DUAL-MODE PC CAMERA CONTROLLER

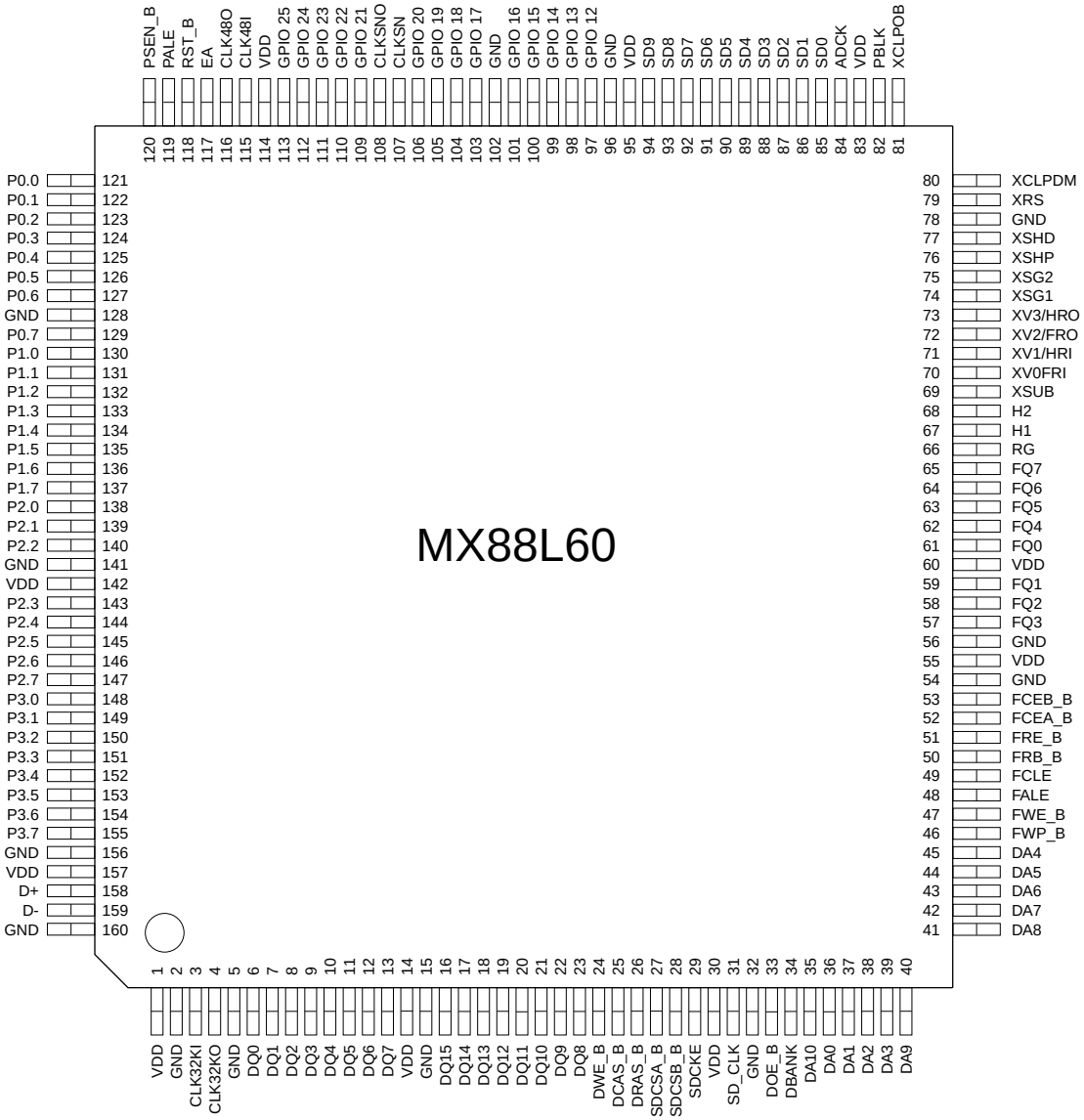
FEATURES

- **Power**
  - 3.3V with power saving control
- **Image Sensor Interface**
  - 8-bit to 10-bit resolution for digital image raw data input
  - Support imager with resolution up to SVGA (800x592)with windowing mode or random-access control
  - Support universal serial interface for various CCD and CMOS sensors
    * CCD sensor: Sony , Sharp , and Panasonic
    * CMOS sensor: Hyundai, HP, VLSI Vision (VVL), Photobit, Biomorphic, TASC, etc.
- **Image Processing Unit**
  - Complete image processing functions:
    * RGB Bayer CFA color interpolation
    * Black reference
    * Defect concealment
    * Flare and black level correction
    * Brightness and contrast control
    * Edge enhancement
    * Color correction
    * Gamma correction
    * RGB to YUV color space conversion
    * Color saturation control
    * False color suppression
    * Image sub-sampling
  - Programmable 5(H) x 5(V) zones with programmable size for image statistical calculation to facilitate automatic exposure control and automatic white balance
  - Support focus-assisting signaling control (with Melody IC interface)
- **Video Compression Unit**
  - High quality and high performance proprietary compression algorithm for live video capture and transferring
    * 30 fps for CIF (352x288)
    * 10~15 fps for VGA (640x480)
- **Memory Control Interface**
  - Support both EDO DRAM (256Kx16) x1 or SDRAM (1Mx16) x1 or x2
  - Support NAND-type Flash memory (8Mb,16Mb,32Mb,64Mb) x1 or x2
  - Support serial Flash memory (MX25L4004, 4Mb) x1, x2,x3 or x4
  - Support Compact Flash card and Smart Media card.
  - Support NDR-type Flash memory (16Mb,32Mb,64Mb)
  - Support EEPROM for sensor information
  - Support Flash memory format function, controlled by PC software
- **PC Interface**
  - High speed USB interface with embedded transceiver
  - UART interface with external transceiver, for best backward compatibility
- **Portable Mode Additional Features**
  - Embedded 8051 micro-controller
  - Support external ROM code storage at Flash memory or EPROM
  - Embedded real-time-clock (RTC) for time stamp
    * Adjusted by PC software
    * On-System programming capability at portable mode
  - Support monochrome TN LCD for information display. The logos include:
    * Date
    * Time
    * Number of pictures left: 2 or 3 digits
    * Flash light status: ON/OFF/AUTO
    * Self Timer: On, Off, and Flash when push the snap shot button
    * Battery status: High, low, and empty
    * Continuous shots: On and Off
    * Quality (compression rate): Best, Better, Good (total 8 classes actually)
    * Image size: Full, 1/2
  - Support self timer function
  - Support melody IC for singling control when
    * Initialization
    * Self timer
    * Snap shot
    * Low battery
    * Failure shot
  - Support flashlight charge control
- **Miscellaneous**
  - 48 MHz system clock operation
  - Dedicated sensor clock input(optional)
  - Built in 27 general-purpose I/O pins
  - 160 pin LQFP

GENERAL DESCRIPTION

The MX88L60 is a general-purpose controller for dual-mode (tethered and portable) PC cameras and toy cameras. The MX88L60 contains all the necessary hardware supports, like image sensor control and interface, image capture and processing, proprietary video compression, memory control, USB and UART interface, embedded micro-controller and general-purpose I/Os. With the intensive hardware and associated software supports, it is an ideal solution for a tethered digital video camera, which can capture real-time live video for entertainment or videoconference applications. For still image capture, the MX88L60 can also function as a controller for low-cost digital still camera (DSC) or toy camera. With Flash memory interface support and power-saving control, it can make the system work on battery power for portable purpose.

PIN CONFIGURATION



Pin Numbers in Numerical Sequence

Name	Pin #	Type	Definition
VDD	1		3.3V
GND	2		
CLKRTCI	3	I	RTC crystal oscillator input, 32KHz
CLKRTCO	4	O	RTC crystal output
GND	5		
DQ0	6	I/O	DRAM data bit 0, pull high/low, mapping to register DRAM_TYPE[0]
DQ1	7	I/O	DRAM data bit 1, pull high/low, mapping to register DRAM_TYPE[1]
DQ2	8	I/O	DRAM data bit 2, pull high/low, mapping to register DCK[0]
DQ3	9	I/O	DRAM data bit 3, pull high/low, mapping to register DCK[1]
DQ4	10	I/O	DRAM data bit 4, , pull high/low, mapping to register DCK[2]
DQ5	11	I/O	DRAM data bit 5, pull high/low, mapping to register DCK[3]
DQ6	12	I/O	DRAM data bit 6, pull high/low, mapping to register TEST[0]
DQ7	13	I/O	DRAM data bit 7, pull high/low, mapping to register TEST[1]
VDD	14		3.3V
GND	15		
DQ15	16	I/O	DRAM data bit 15, pull high/low, mapping to register TEST[9]
DQ14	17	I/O	DRAM data bit 14, pull high/low, mapping to register TEST[8]
DQ13	18	I/O	DRAM data bit 13, pull high/low, mapping to register TEST[7]
DQ12	19	I/O	DRAM data bit 12, pull high/low, mapping to register TEST[6]
DQ11	20	I/O	DRAM data bit 11, pull high/low, mapping to register TEST[5]
DQ10	21	I/O	DRAM data bit 10, pull high/low, mapping to register TEST[4]
DQ9	22	I/O	DRAM data bit 9, pull high/low, mapping to register TEST[3]
DQ8	23	I/O	DRAM data bit 8, pull high/low, mapping to register TEST[2]
DWE_B	24	O	DRAM write enable
DCAS_B	25	O	DRAM Column address strobe
DRAS_B	26	O	DRAM Row address strobe
SDCSA_B	27	O	SDRAM #0 chip select
SDCSB_B	28	O	SDRAM #1 chip select
SDCKE	29	O	SDRAM clock enable
VDD	30		3.3V
SDCLKO	31	O	SDRAM clock output
GND	32		
DOE_B	33	O	SDRAM, ldqm, udqm, EDORAM output enable
DBANK	34	O	SDRAM bank select
DA10	35	O	SDRAM address bit 10
DA0	36	O	DRAM address bit 0
DA1	37	O	DRAM address bit 1
DA2	38	O	DRAM address bit 2

Name	Pin #	Type	Definition
DA3	39	O	DRAM address bit 3
DA9	40	O	SDRAM address bit 9
DA8	41	O	DRAM address bit 8
DA7	42	O	DRAM address bit 7
DA6	43	O	DRAM address bit 6
DA5	44	O	DRAM address bit 5
DA4	45	O	DRAM address bit 4
FWP_B	46	O	Flash memory write protect
FWE_B	47	O	NAND type flash memory write enable Serial flash data output
FALE	48	O	NAND type flash memory address latch enable Serial flash memory #3 chip select
FCLE	49	O	NAND type flash memory command latch enable Serial flash memory #2 chip select
FRB_B	50	I	NAND type flash memory read/busy input Serial flash data input
FRE_B	51	O	NAND type flash memory read enable Serial flash clock output
FCEA_B	52	O	Flash memory #0 chip select
FCEB_B	53	O	Flash memory #1 chip select
GND	54		
VDD	55		3.3V
GND	56		
FQ3	57	I/O	NAND type flash memory data bit 3, pull high/low, mapping to register GP_CFG[0]
FQ2	58	I/O	NAND type flash memory data bit 2, pull high/low, mapping to register FLASH_TYPE[2]
FQ1	59	I/O	NAND type flash memory data bit 1, pull high/low, mapping to register FLASH_TYPE[1]
VDD	60		3.3V
FQ0	61	I/O	NAND type flash memory data bit 0, pull high/low, mapping to register FLASH_TYPE[0]
FQ4	62	I/O	NAND type flash memory data bit 4, pull high/low, mapping to register GP_CFG[1]
FQ5	63	I/O	NAND type flash memory data bit 5, pull high/low, mapping to register GP_CFG[2]
FQ6	64	I/O	NAND type flash memory data bit 6, pull high/low, mapping to register GP_CFG[3]
FQ7	65	I/O	NAND type flash memory data bit 7, pull high/low, mapping to register GP_CFG[4]
RG	66	O	Reset gate pulse output for CCD image sensor
H1	67	O	Horizontal transfer pulse output 1 for CCD image sensor
H2	68	O	Horizontal transfer pulse output 2 for CCD image sensor
XSUB	69	O	Pulse output for electronic shutter
XV0/ FRI	70	I/O	Vertical transfer-pulse 0 for CCD image sensor; also can be programmed to vertical sync signal input.
XV1/ HRI	71	I/O	Vertical transfer-pulse 1 for CCD image sensor; also can be programmed to horizontal sync signal input.

Name	Pin #	Type	Definition
XV2/ FRO	72	O	Vertical transfer pulse 2 for CCD image sensor; also can be programmed to vertical sync signal output
XV3/ HRO	73	O	Vertical transfer pulse 3 for CCD image sensor; also can be programmed to horizontal sync signal output
XSG1	74	O	Readout pulse 1 for CCD image sensor
XSG2	75	O	Readout pulse 2 for CCD image sensor
XSHP	76	O	Pre-charge level sample-and-hold pulse
XSHD	77	O	Data level sample-and-hold pulse
GND	78		
XRS	79	O	Sample-and-hold pulse output for analog/digital conversion IC
XCLPDM	80	O	Dummy bit block clamp pulse output
XCLPOB	81	O	Optical black bit block clamp pulse output
PBLK	82	O	Pre-blanking pulse that corresponds to the cease period of horizontal transfer pulse for CCD image sensor.
VDD	83		3.3V
ADCK	84	O	Clock output for analog/digital conversion IC or CMOS image sensor.
SD0	85	I	Sensor input data bit 0 (LSB)
SD1	86	I	Sensor input data bit 1
SD2	87	I	Sensor input data bit 2
SD3	88	I	Sensor input data bit 3
SD4	89	I	Sensor input data bit 4
SD5	90	I	Sensor input data bit 5
SD6	91	I	Sensor input data bit 6
SD7	92	I	Sensor input data bit 7
SD8	93	I	Sensor input data bit 8
SD9	94	I	Sensor input data bit 9(MSB)
VDD	95		3.3V
GND	96		
GPIO 12	97	I/O	GPIO bit 12
GPIO 13	98	I/O	GPIO bit 13
GPIO 14	99	I/O	GPIO bit 14
GPIO 15	100	I/O	GPIO bit 15
GPIO 16	101	I/O	GPIO bit 16
GND	102		
GPIO 17	103	I/O	GPIO bit 17
GPIO 18	104	I/O	GPIO bit 18
GPIO 19	105	I/O	GPIO bit 19
GPIO 20	106	I/O	GPIO bit 20, 8051 clock off output
CLKSNI	107	I	Sensor clock crystal oscillator input
CLKSNO	108	O	Sensor clock crystal output

Name	Pin #	Type	Definition
GPIO 21	109	I/O	GPIO bit 21, flash light strobe output
GPIO 22	110	I/O	GPIO bit 22
GPIO 23	111	I/O	GPIO bit 23
GPIO 24	112	I/O	GPIO bit 24
GPIO 25	113	I/O	GPIO bit 25
VDD	114		3.3V
CLK48I	115	I	System clock crystal oscillator input, 48MHz
CLK48O	116	O	System clock crystal output
EA	117	I	External ROM enable
RST_B	118	I	Hardware reset
PALE	119	I/O	Address latch enable
PSEN_B	120	I/O	Program strobe enable
P0.0	121	I/O	8051 port 0 bit 0, external address/data bus bit 0
P0.1	122	I/O	8051 port 0 bit 1, external address/data bus bit 1
P0.2	123	I/O	8051 port 0 bit 2, external address/data bus bit 2
P0.3	124	I/O	8051 port 0 bit 3, external address/data bus bit 3
P0.4	125	I/O	8051 port 0 bit 4, external address/data bus bit 4
P0.5	126	I/O	8051 port 0 bit 5, external address/data bus bit 5
P0.6	127	I/O	8051 port 0 bit 6, external address/data bus bit 6
GND	128		
P0.7	129	I/O	8051 Port 0 bit 7, external address/data bus bit 7
P1.0	130	I/O	8051 port 1 bit 0, GPIO bit 0,
P1.1	131	I/O	8051 port 1 bit 1, GPIO bit 1,
P1.2	132	I/O	8051 port 1 bit 2, GPIO bit 2,
P1.3	133	I/O	8051 port 1 bit 3, GPIO bit 3
P1.4	134	I/O	8051 port 1 bit 4, GPIO bit 4
P1.5	135	I/O	8051 port 1 bit 5, GPIO bit 5
P1.6	136	I/O	8051 port 1 bit 6, GPIO bit 6, SCL
P1.7	137	I/O	8051 Port 1 bit 7, GPIO bit 7, SDA
P2.0	138	I/O	8051 port 2 bit 0, external address bus bit 8
P2.1	139	I/O	8051 port 2 bit 1, external address bus bit 9
P2.2	140	I/O	8051 port 2 bit 2, external address bus bit 10
GND	141		
VDD	142		3.3V
P2.3	143	I/O	8051 port 2 bit 3, external address bus bit 11
P2.4	144	I/O	8051 port 2 bit 4, external address bus bit 12
P2.5	145	I/O	8051 port 2 bit 5, external address bus bit 13
P2.6	146	I/O	8051 port 2 bit 6, external address bus bit 14
P2.7	147	I/O	8051 Port 2 bit 7, external address bus bit 15
P3.0	148	I/O	8051 port 3 bit 0, GPIO bit 8, RXD
P3.1	149	I/O	8051 port 3 bit 1, GPIO bit 9, TXD

Name	Pin #	Type	Definition
P3.2	150	I/O	8051 port 3 bit 2, interrupt 0,
P3.3	151	I/O	8051 port 3 bit 3, interrupt 1,
P3.4	152	I/O	8051 port 3 bit 4, GPIO bit 10
P3.5	153	I/O	8051 port 3 bit 5, GPIO bit 11
P3.6	154	I/O	8051 port 3 bit 6, external SRAM write strobe, GPIO26
P3.7	155	I/O	8051 Port 3 bit 7, external SRAM read strobe, GPIO27
GND	156		
UVDD	157		3.3V
D+	158	I/O	Data+, USB data bus
D-	159	I/O	Data-, USB data bus
UGND	160		

Pin Numbers/Definition by Function

Power Supply

Name	Pin #	Type	Definition
VDD	1		3.3V
VDD	14		3.3V
VDD	30		3.3V
VDD	55		3.3V
VDD	60		3.3V
VDD	83		3.3V
VDD	95		3.3V
VDD	114		3.3V
VDD	142		3.3V
UVDD	61		3.3V
GND	2		
GND	5		
GND	15		
GND	32		
GND	54		
GND	56		
GND	78		
GND	96		
GND	102		
GND	128		
GND	141		
GND	156		
UGND	62		

Sensor Interface

Name	Pin #	Type	Definition
RG	66	O	Reset gate pulse output for CCD image sensor
H1	67	O	Horizontal transfer pulse output 1 for CCD image sensor
H2	68	O	Horizontal transfer pulse output 2 for CCD image sensor
XSUB	69	O	Pulse output for electronic shutter
XV0/ FRI	70	I/O	Vertical transfer-pulse 0 for CCD image sensor; also can be programmed to vertical sync signal input.
XV1/ HRI	71	I/O	Vertical transfer-pulse 1 for CCD image sensor; also can be programmed to horizontal sync signal input.
XV2/ FRO	72	O	Vertical transfer pulse 2 for CCD image sensor; also can be programmed to vertical sync signal input
XV3/ HRO	73	O	Vertical transfer pulse 3 for CCD image sensor; also can be programmed to horizontal sync signal input
XSG1	74	O	Readout pulse 1 for CCD image sensor
XSG2	75	O	Readout pulse 2 for CCD image sensor
XSHP	76	O	Pre-charge level sample-and-hold pulse
XSHD	77	O	Data level sample-and-hold pulse
XRS	79	O	Sample-and-hold pulse output for analog/digital conversion IC
XCLPDM	80	O	Dummy bit block clamp pulse output
XCLPOB	81	O	Optical black bit block clamp pulse output
PBLK	82	O	Pre-blanking pulse that corresponds to the cease period of horizontal transfer pulse for CCD image sensor.
ADCK	84	O	Clock output for analog/digital conversion IC or CMOS image sensor. Phase adjustment in 90^{O} units.
SD0	85	I	Sensor input data bit 0 (LSB)
SD1	86	I	Sensor input data bit 1
SD2	87	I	Sensor input data bit 2
SD3	88	I	Sensor input data bit 3
SD4	89	I	Sensor input data bit 4
SD5	90	I	Sensor input data bit 5
SD6	91	I	Sensor input data bit 6
SD7	92	I	Sensor input data bit 7
SD8	93	I	Sensor input data bit 8
SD9	94	I	Sensor input data bit 9(MSB)

DRAM Interface

Name	Pin #	Type	Definition
DQ0	6	I/O	DRAM data bit 0, pull high/low, mapping to register DRAM_TYPE[0]
DQ1	7	I/O	DRAM data bit 1, pull high/low, mapping to register DRAM_TYPE[1]
DQ2	8	I/O	DRAM data bit 2, pull high/low, mapping to register DCK[0]
DQ3	9	I/O	DRAM data bit 3, pull high/low, mapping to register DCK[1]
DQ4	10	I/O	DRAM data bit 4, pull high/low, mapping to register DCK[2]
DQ5	11	I/O	DRAM data bit 5, pull high/low, mapping to register DCK[3],
DQ6	12	I/O	DRAM data bit 6, pull high/low, mapping to register TEST[0]
DQ7	13	I/O	DRAM data bit 7, pull high/low, mapping to register TEST[1]
DQ8	23	I/O	DRAM data bit 8, pull high/low, mapping to register TEST[2]
DQ9	22	I/O	DRAM data bit 9, pull high/low, mapping to register TEST[3]
DQ10	21	I/O	DRAM data bit 10, pull high/low, mapping to register TEST[4]
DQ11	20	I/O	DRAM data bit 11, pull high/low, mapping to register TEST[5]
DQ12	19	I/O	DRAM data bit 12, pull high/low, mapping to register TEST[6]
DQ13	18	I/O	DRAM data bit 13, pull high/low, mapping to register TEST[7]
DQ14	17	I/O	DRAM data bit 14, pull high/low, mapping to register TEST[8]
DQ15	16	I/O	DRAM data bit 15, pull high/low, mapping to register TEST[9]
DWE_B	24	O	DRAM write enable
DCAS_B	25	O	DRAM Column address strobe
DRAS_B	26	O	DRAM Row address strobe
SDCSA_B	27	O	SDRAM #0 chip select
SDCSB_B	28	O	SDRAM #1 chip select
SDCKE	29	O	SDRAM clock enable
SDCLKO	31	O	SDRAM clock output
DOE_B	33	O	SDRAM, ldqm, udqm,EDORAM output enable
DA0	36	O	DRAM address bit 0
DA1	37	O	DRAM address bit 1
DA2	38	O	DRAM address bit 2
DA3	39	O	DRAM address bit 3
DA4	45	O	DRAM address bit 4
DA5	44	O	DRAM address bit 5
DA6	43	O	DRAM address bit 6
DA7	42	O	DRAM address bit 7
DA8	41	O	DRAM address bit 8
DA9	40	O	SDRAM address bit 9
DA10	35	O	SDRAM address bit 10
DBANK	34	O	SDRAM bank select

Flash Memory Interface

Name	Pin #	Type	Definition
FCLE	49	O	NAND type flash memory command latch enable Serial flash memory #2 chip select
FALE	48	O	NAND type flash memory address latch enable Serial flash memory #3 chip select
FWE_B	47	O	NAND type flash memory write enable Serial flash memory data output
FWP_B	46	O	Flash memory write protect
FRB_B	50	I	NAND type flash memory read/busy input Serial flash memory data input
FRE_B	51	O	NAND type flash memory read enable Serial flash memory clock output
FCEA_B	52	O	Flash memory #0 chip select
FCEB_B	53	O	Flash memory #1 chip select
FQ0	61	I/O	NAND type flash memory data bit 0, pull high/low, mapping to register FLASH_TYPE[0]
FQ1	59	I/O	NAND type flash memory data bit 1, pull high/low, mapping to register FLASH_TYPE[1]
FQ2	58	I/O	NAND type flash memory data bit 2, pull high/low, mapping to register FLASH_TYPE[2]
FQ3	57	I/O	NAND type flash memory data bit 3, pull high/low, mapping to register GP_CFG[0]
FQ4	62	I/O	NAND type flash memory data bit 4, pull high/low, mapping to register GP_CFG[1]
FQ5	63	I/O	NAND type flash memory data bit 5, pull high/low, mapping to register GP_CFG[2]
FQ6	64	I/O	NAND type flash memory data bit 6, pull high/low, mapping to register GP_CFG[3]
FQ7	65	I/O	NAND type flash memory data bit 7, pull high/low, mapping to register GP_CFG[4]

USB Interface

Name	Pin #	Type	Definition
D+	158	I/O	Data+, USB data bus
D-	159	I/O	Data-, USB data bus

Micro-Controller Interface

Name	Pin #	Type	Definition
P0.0	121	I/O	8051 port 0 bit 0, external address/data bus bit 0
P0.1	122	I/O	8051 port 0 bit 1, external address/data bus bit 1
P0.2	123	I/O	8051 port 0 bit 2, external address/data bus bit 2
P0.3	124	I/O	8051 port 0 bit 3, external address/data bus bit 3
P0.4	125	I/O	8051 port 0 bit 4, external address/data bus bit 4
P0.5	126	I/O	8051 port 0 bit 5, external address/data bus bit 5
P0.6	127	I/O	8051 port 0 bit 6, external address/data bus bit 6
P0.7	129	I/O	8051 Port 0 bit 7, external address/data bus bit 7
P1.0	130	I/O	8051 port 1 bit 0, GPIO bit 0,
P1.1	131	I/O	8051 port 1 bit 1, GPIO bit 1,
P1.2	132	I/O	8051 port 1 bit 2, GPIO bit 2,
P1.3	133	I/O	8051 port 1 bit 3, GPIO bit 3

P1.4	134	I/O	8051 port 1 bit 4, GPIO bit 4
P1.5	135	I/O	8051 port 1 bit 5, GPIO bit 5
P1.6	136	I/O	8051 port 1 bit 6, GPIO bit 6, SCL
P1.7	137	I/O	8051 Port 1 bit 7, GPIO bit 7, SDA
P2.0	138	I/O	8051 port 2 bit 0, external address bus bit 8
P2.1	139	I/O	8051 port 2 bit 1, external address bus bit 9
P2.2	140	I/O	8051 port 2 bit 2, external address bus bit 10
P2.3	143	I/O	8051 port 2 bit 3, external address bus bit 11
P2.4	144	I/O	8051 port 2 bit 4, external address bus bit 12
P2.5	145	I/O	8051 port 2 bit 5, external address bus bit 13
P2.6	146	I/O	8051 port 2 bit 6, external address bus bit 14
P2.7	147	I/O	8051 Port 2 bit 7, external address bus bit 15
P3.0	148	I/O	8051 port 3 bit 0, GPIO bit 8, RXD
P3.1	149	I/O	8051 port 3 bit 1, GPIO bit 9, TXD
P3.2	150	I/O	8051 port 3 bit 2, interrupt 0,
P3.3	151	I/O	8051 port 3 bit 3, interrupt 1,
P3.4	152	I/O	8051 port 3 bit 4, GPIO bit 10
P3.5	153	I/O	8051 port 3 bit 5, GPIO bit 11
P3.6	154	I/O	8051 port 3 bit 6, external SRAM write strobe, GPIO26
P3.7	155	I/O	8051 Port 3 bit 7, external SRAM read strobe, GPIO27
EA	117	I	External ROM enable
PALE	119	I/O	Address latch enable
PSEN_B	120	I/O	Program strobe enable

Miscellaneous

Name	Pin #	Type	Definition
GPIO12	97	I/O	GPIO bit 12, sel_sram_b
GPIO 13	98	I/O	GPIO bit 13, usb_dpluso
GPIO 14	99	I/O	GPIO bit 14, usb_dminuso
GPIO 15	100	I/O	GPIO bit 15, usb_data_en_b
GPIO 16	101	I/O	GPIO bit 16, usb_suspendo
GPIO 17	103	I/O	GPIO bit 17, usb_dplusi
GPIO 18	104	I/O	GPIO bit 18, usb_dmiusi
GPIO 19	105	I/O	GPIO bit 19, usb_datai
GPIO 20	106	I/O	GPIO bit 20, 8032 clock off output
GPIO 21	109	I/O	GPIO bit 21, flash light strobe output
GPIO 22	110	I/O	GPIO bit 22
GPIO 23	111	I/O	GPIO bit 23
GPIO 24	112	I/O	GPIO bit 24

Absolute Maximum Ratings

RATING	VALUE
DC Supply Voltage(VCC)	3.0V to 3.6V
DC Input/Output Voltage(Vin/Vout)	-0.5V to VCC+0.5V
Ambient Temperature(TA)	0 to 70Celsius
Storage Temperature(TSTG)	-40 to 125Celsius
ESD rating(Rzap=1.5K,Czap=100pF)	2000V
Power Dissipation(PD)	0.7mW
Power Dissipation(Normal)	0.4W

DC Characteristics

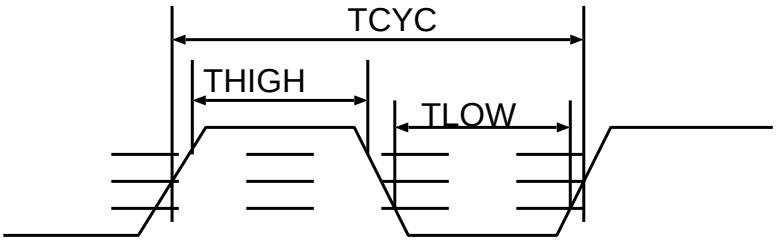
SYMBOL	Description	MIN	MAX	Test Conditions	Unit
VIL	Input Low Voltage	-	0.8		Volt
VIH	Input High Voltage	2.0	-		Volt
VOL	Output Low Voltage	-	0.4	I=4ma	Volt
VOH	Output Low Voltage	0.8VCC	-	I=4ma	Volt
ICC	Power Supply Current	-	130	VCC=3.3V 640x480x10Hz	ma
IIL	Input Low Current	-1	1	VCC=3.5V, Vin=0V	ua
IIH	Input High Current	-	1	Vin=VCC	ua
Rpullup	Pull Up Resistance	20	60		K ohm
IDD	Static IDD Current	-			ma
Cin	Input Capacitance	3	10		pf
Cout	Output Capacitance		45		pf

AC Characteristics

RESET Timing AC Characteristics

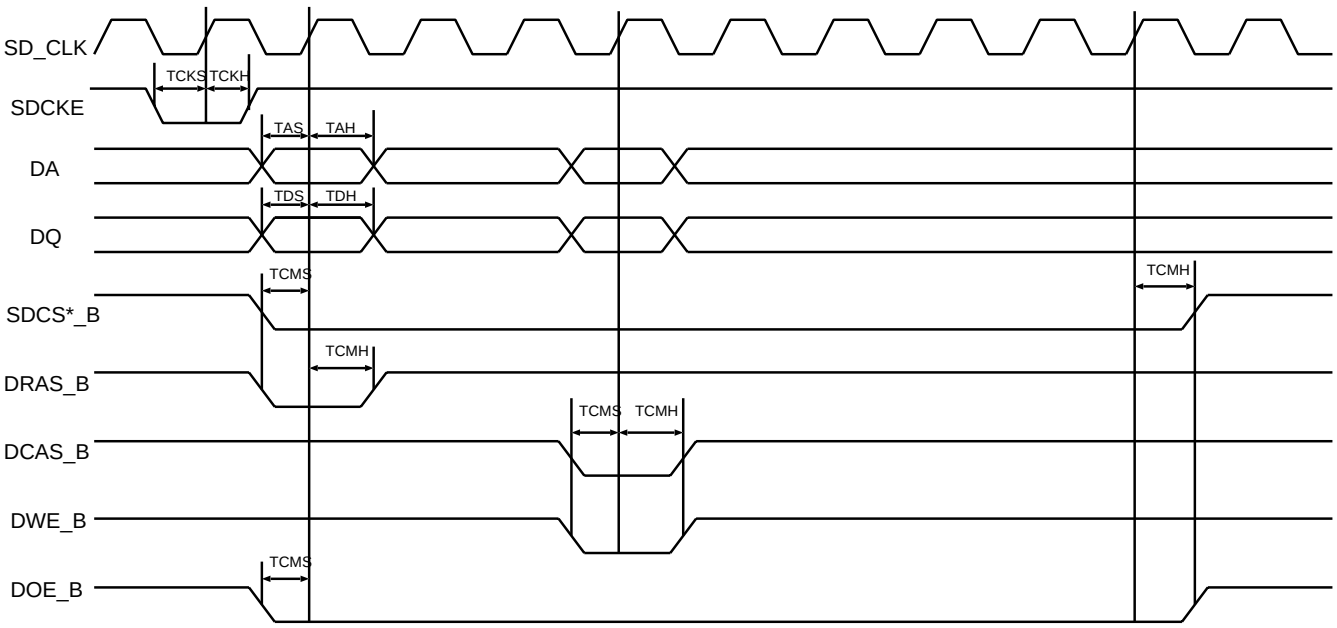
SYMBOL	Description	MIN	MAX	Test Conditions	Unit
TRST	Reset Pulse Width	250			ns

Clock AC Characteristics



SYMBOL	PARAMETER	MIN	TYP	MAX	Unit
1/TCYC	CLK48I		48		Mhz
	CLK32KI		32.768		Khz
	SD_CLK		48		Mhz
THIGH	CLK48I		10.4		ns
	CLK32KI		15.2		ms
	SD_CLK		10.4		ns
TLOW	CLK48I		10.4		ns
	CLK32KI		15.2		ms
	SD_CLK		10.4		ns

SDRAM Interface Timings

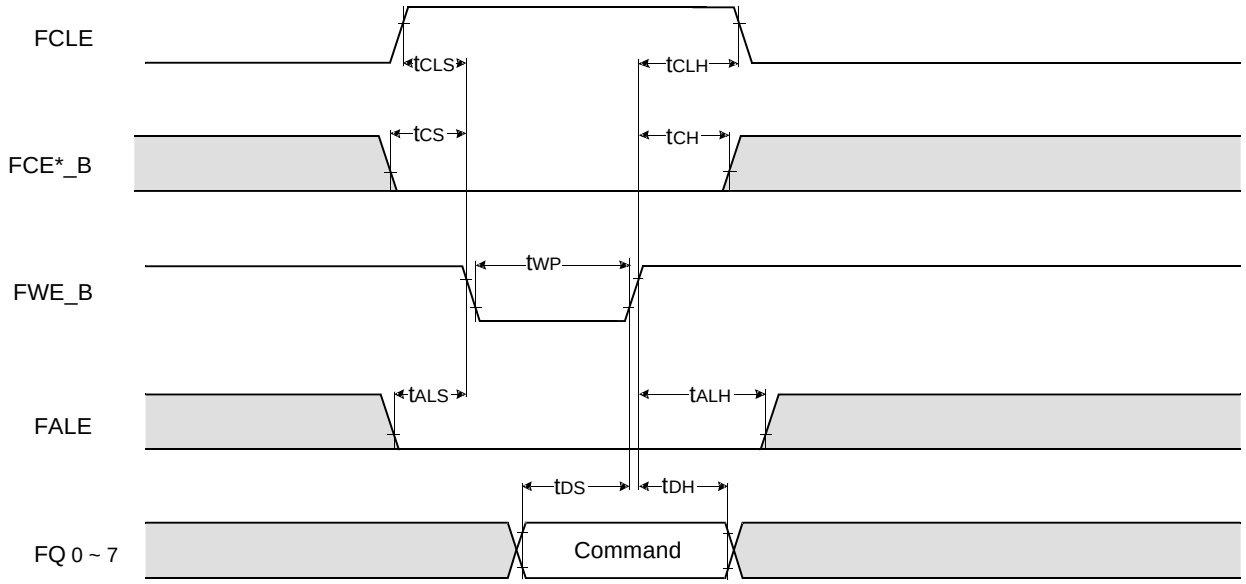


Parameter	SYMBOL	MIN	TYP	MAX	Unit
Address setup time	TAS	3	–	–	ns
Address hold time	TAH	1.5	–	–	ns
Data-in setup time	TDS	3	–	–	ns
Data-in hold time	TDH	1.5	–	–	ns
CKE setup time	TCKS	3	–	–	ns
CKE hold time	TCKH	1.5	–	–	ns
Command setup time	TCMS	3	–	–	ns
Command hold time	TCMH	1.5	–	–	ns

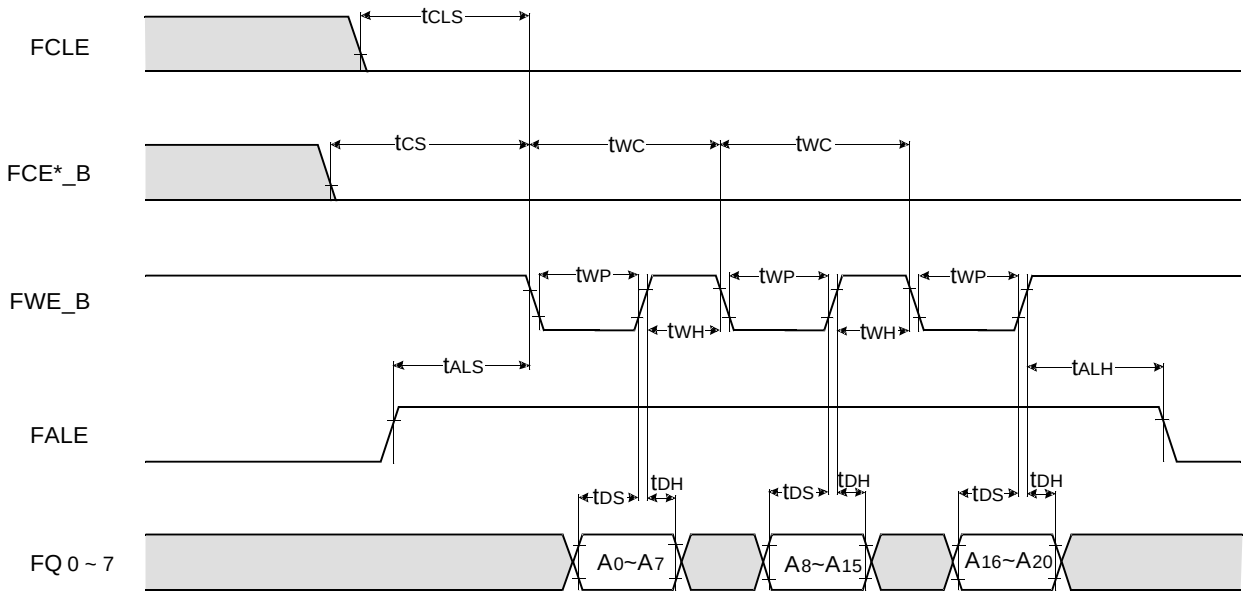
Note : SDRAM Interface Timing is adjustable in the step of about 2ns

NANDFLASH Interface Timings

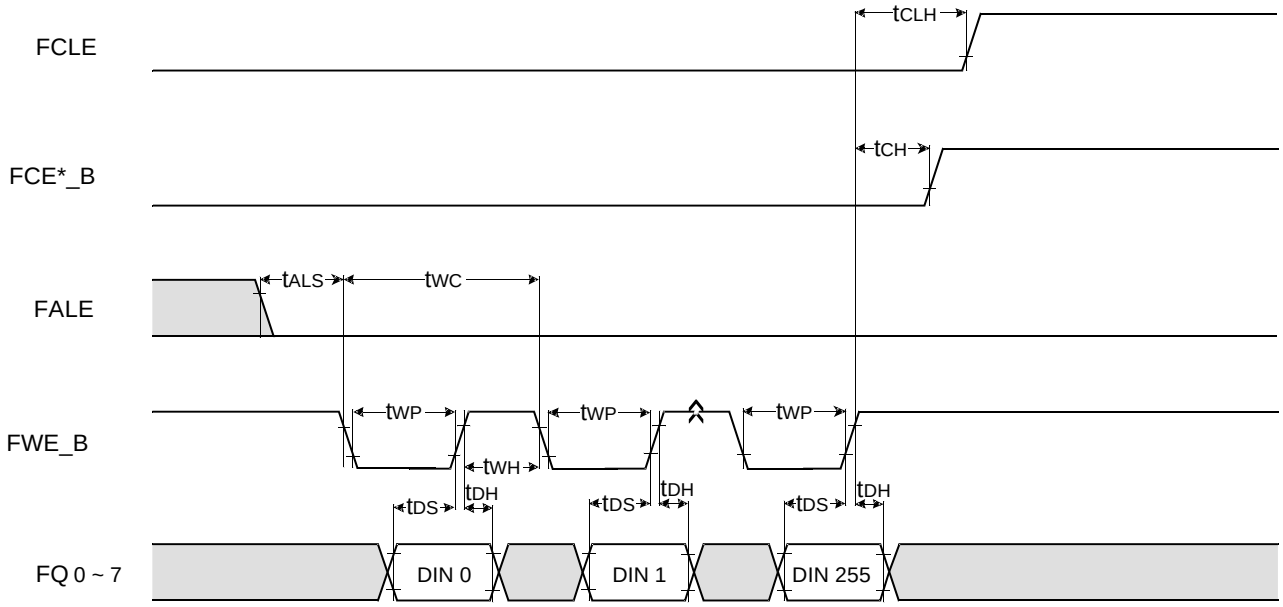
* Command Latch Cycle



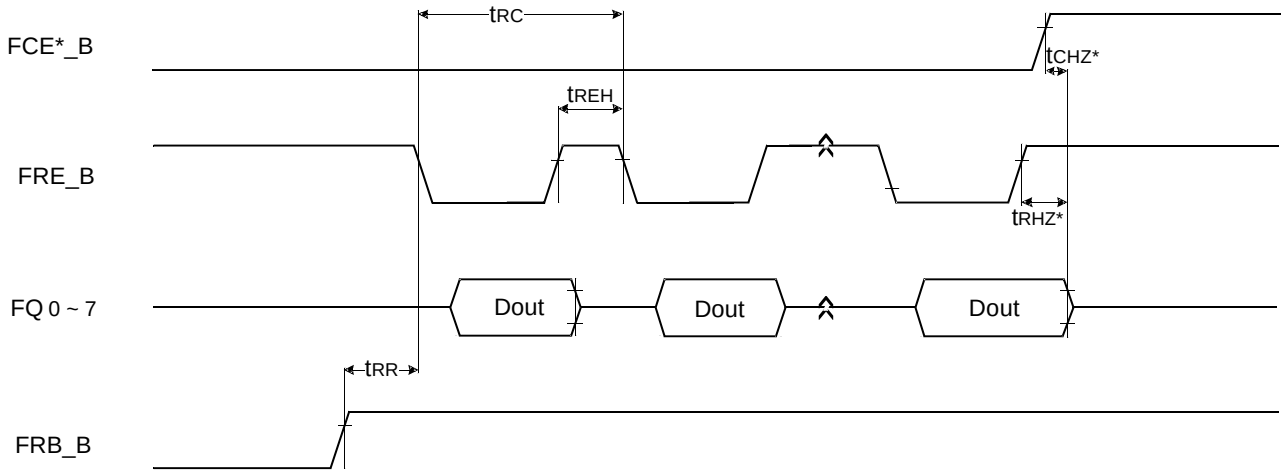
* Address Latch Cycle



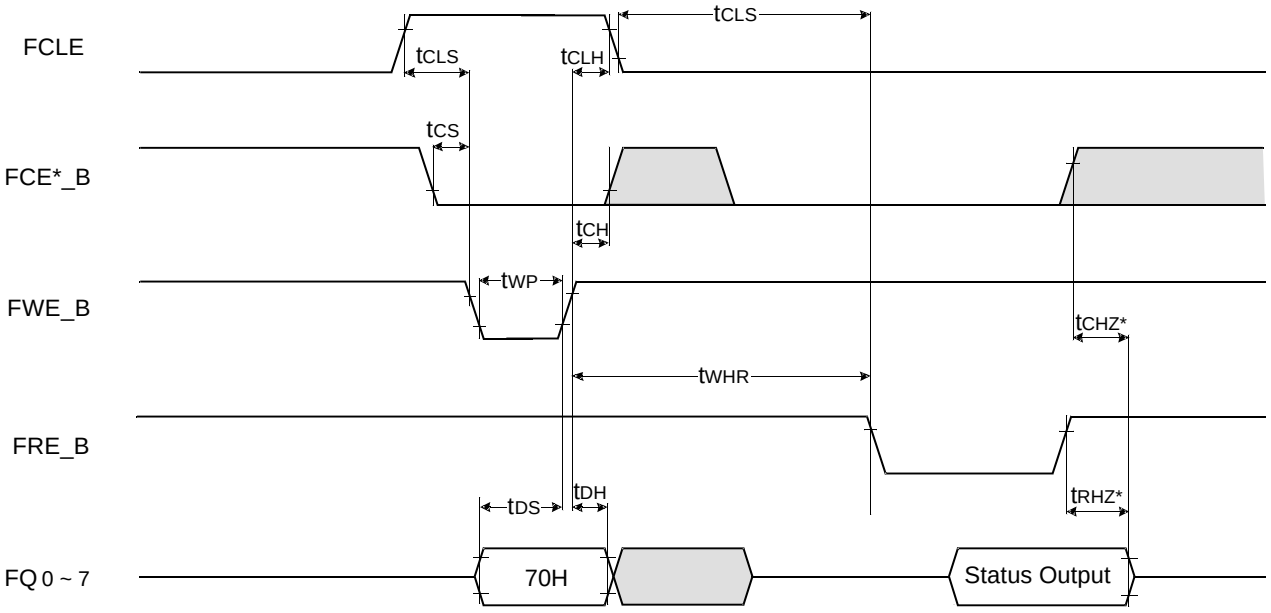
* Input Data Latch Cycle



* Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



* Status Read Cycle



AC Timing Characteristics for Command / Address / Data Input

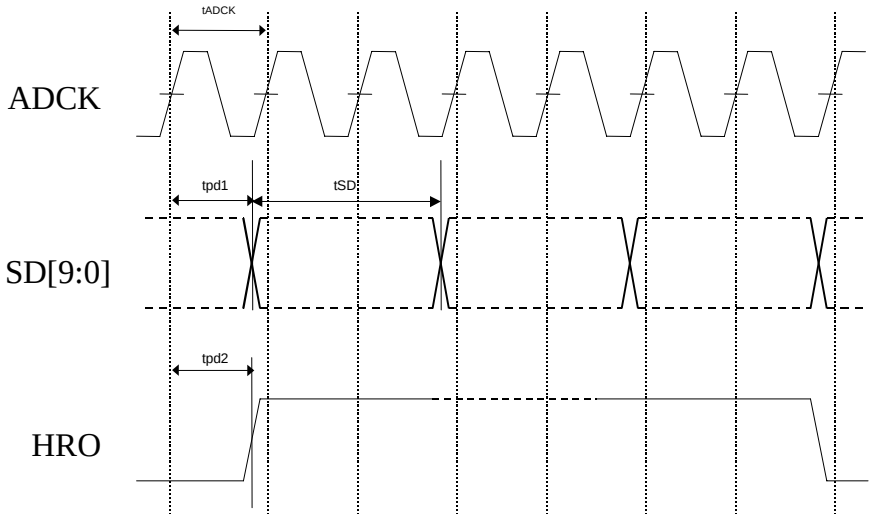
Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	tCLS	1		CLK *
CLE Hold Time	tCLH	2		CLK
$\overline{CE}$ Setup Time	tCS	2		CLK
$\overline{CE}$ Hold Time	tCH	8		CLK
$\overline{WE}$ Pulse Width	tWP	2		CLK
ALE Setup Time	tALS	1		CLK
ALE Hold Time	tALH	2		CLK
Data Setup Time	tDS	2		CLK
Data Hold Time	tDH	2		CLK
Write Cycle Time	tWC	4		CLK
$\overline{WE}$ High Hold Time	tWH	2		CLK

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Ready to RE Low	tRR	6		CLK
Read Cycle Time	tRC	4		CLK
$\overline{RE}$ High to Output Hi-Z	tRHZ	0		
$\overline{CE}$ High to Output Hi-Z	tCHZ	0		
$\overline{RE}$ High Hold Time	tREH	1		CLK
$\overline{WE}$ High to RE Low	tWHR	3		CLK

* 1 CLK = one CLK48I cycle time

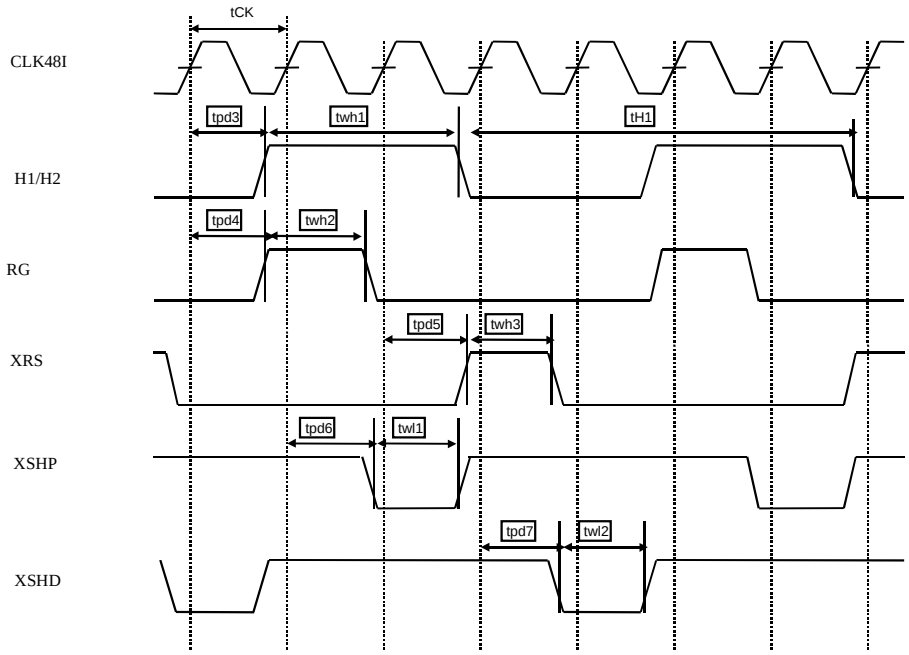
SENSOR Interface Timings



Symbol	Definition	Min.	Typ.	Max.	Unit
tADCK	ADCK cycle time	20.8	-	-	ns
tSD	sensor data cycle time	1	-	6	TADCK
tpd1	sensor data input delay	0	-	6	TADCK
tpd2	HRO rising delay	0	-	-	ns

* 1 TADCK = one ADCK cycle time

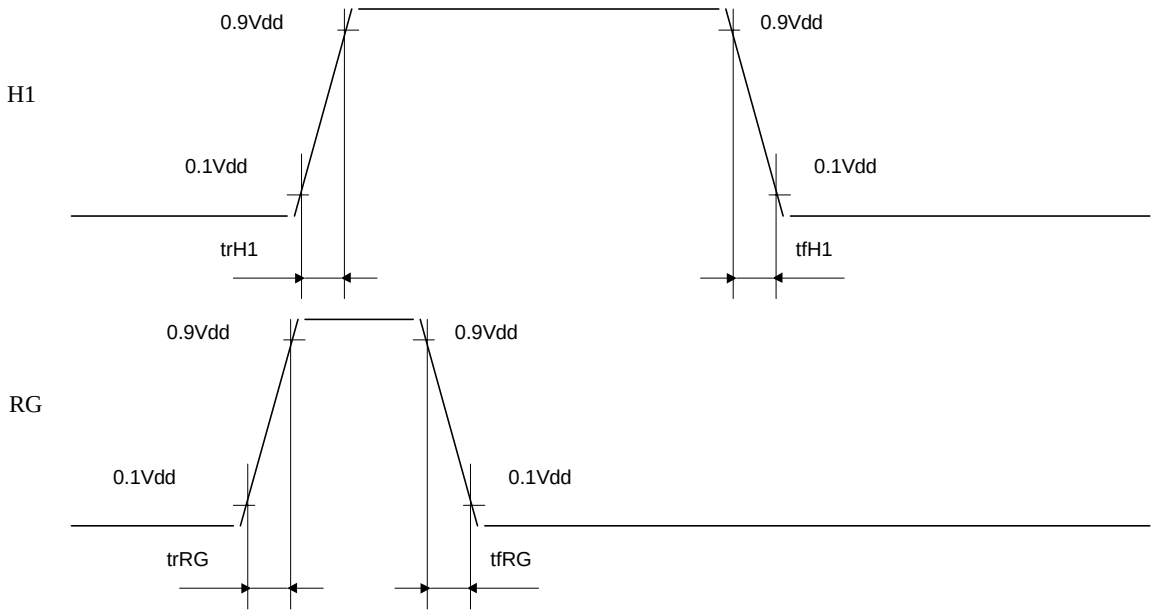
CCD sensor interface timings



CLoad : 35pF, 25^{O}C

Symbol	Definition	Min.	Typ.	Max.	Unit
tH1	H1/H2 cycle time	4	-	-	SCLK*
tpd3	H1/H2 rising delay, activated by the rising edge of CLK48I	1.2	-	-	ns**
tpd4	RG rising delay, activated by the rising edge of CLK48I	3.0	-	-	ns**
tpd5	XRS rising delay, activated by the rising edge of CLK48I	3.0	-	-	ns**
tpd6	XSHP falling delay, activated by the rising edge of CLK48I	3.0	-	-	ns**
tpd7	XSHD falling delay, activated by the rising edge of CLK48I	2.6	-	-	ns**
twh1	H1/H2 high level width		2	-	SCLK
twh2	Pulse width of RG		1		SCLK
twh3	Pulse width of XRS		1		SCLK
twl1	Pulse width of XSHP		1	-	SCLK
twl2	Pulse width of XSHD		1		SCLK

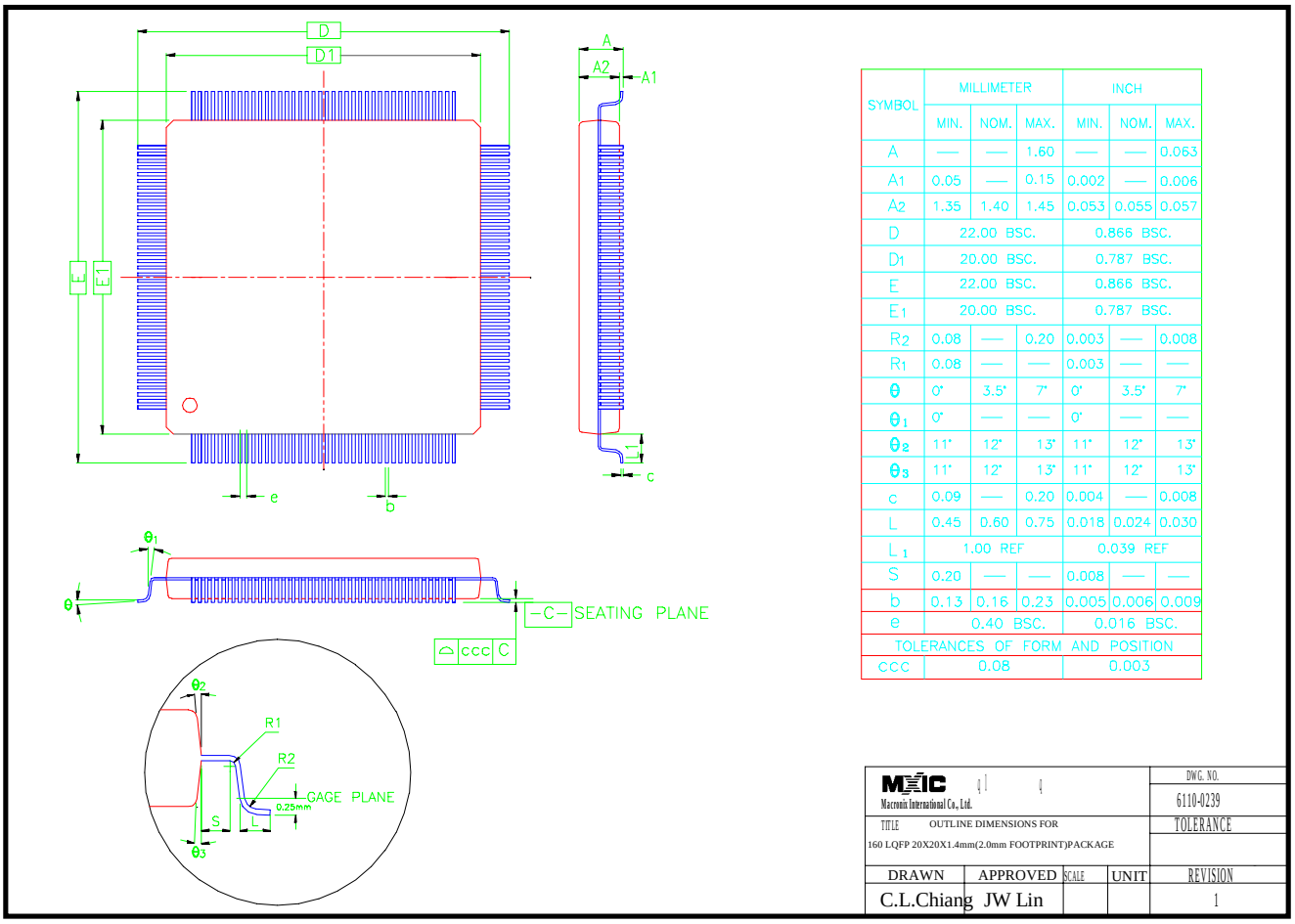
* 1 SCLK = one cycle of CLK48I or SD.CLK
** adjustable by registry settings



CLoad : 30pF, 25^{O}C

Symbol	Definition	Min.	Typ.	Max.	Unit
trH1	H1 rise time		2.1		ns
tfH1	H1 fall time		1.8		ns
trRG	RG rise time		2.1		ns
tfRG	RG fall time		1.8		ns

PACKAGE INFORMATION



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	22.00 BSC.			0.866 BSC.		
E1	20.00 BSC.			0.787 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
TOLERANCES OF FORM AND POSITION						
ccc	0.08			0.003		

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TITLE: OUTLINE DIMENSIONS FOR 160 LQFP 20X20X1.4mm(2.0mm FOOTPRINT)PACKAGE					TOLERANCE
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