MX88V44

Analog LCD Panel Controller
Datasheet

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General Description

MX88V44 is the low cost high performance solution for subsized LCD panel display. It accepts digital video input in 8-bit CCIR656 or CCIR601 format with 4:3 aspect ratio. A flexible Timing controller (TCON) is embedded to supports variety analog LCD panel. Three display modes can be selected: Full, Normal or Cinema. It also includes programmable brightness, sharpness, contrast, saturation, hue , gamma and sharpness control for LCD display adjustment. Embedded ADC and TV decoder for TV input, embedded RGB DAC for low cost panel drive.

Application

- Portable DVD player with analog LCD panel (AUO, CPT, Sharp, Panasonic, LG, Samsung, Sanyo Ö).
- Portable DTV
- Car Entertainment System
- Rear Seat Display System

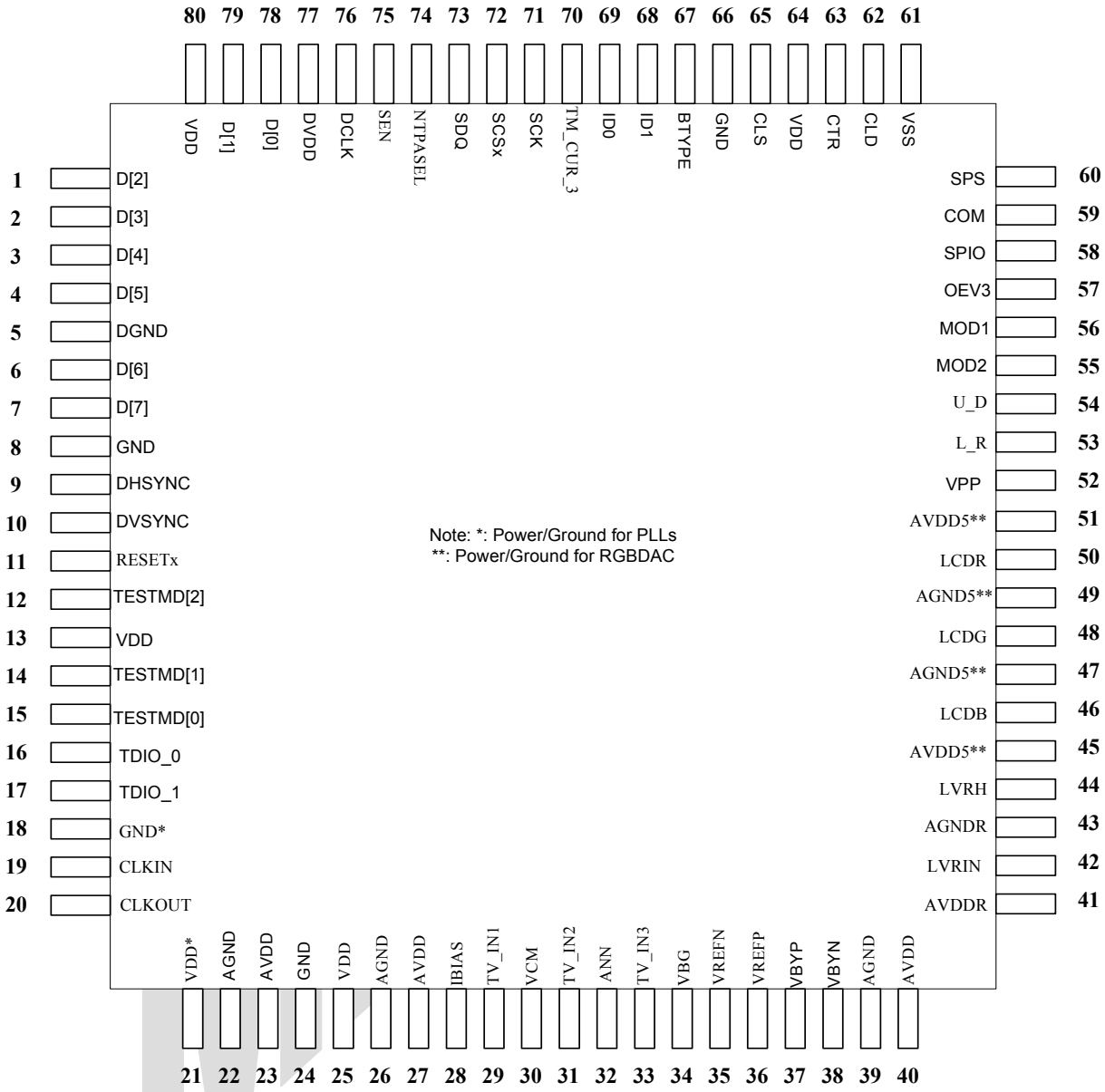
Main Feature

- **Video Input**
  - Support DVD VCD and more decoded CCIR656/601 standard 8-bit YCbCr input.
  - Support video input source in 4:3 aspect ratio.
- **LCD Display Interface**
  - Fix coefficient CSC (Color Space Conversion)
  - Programmable Brightness, Contrast, Saturation and Hue adjustment.
  - 256-segment piecewise-linear RGB Gamma adjustment.
  - Built-in sharpness enhancement.
  - Built-in Timing Controller to drive the Analog LCD panel directly.
  - Support LCD modules in 400x234, 480x234, 320x234. (Programmable)
  - Support 3 display modes: Full, Normal and Cinema. (Sharp Panel)
  - Support 64 built-in and 64 user define fonts OSD with color change, border control, transparent and scaling control.
- **TV input interface**
  - Embedded TV decoder for CVBS input (NTSC/PAL/SECAM).
  - Embedded 10-bit ADC with AGC and clamp.
- **CPU Interface**

- Support 2-wire and 3-wire serial interface to communicate with external micro-controller.

- **Other**
  - Advanced power saving control.
  - Power supply: 5V for LCD DAC, Tcon pad output, and 3.3V for others pad, core 2.5V

Pin configuration



Package: LQFP80

Pin Name	Pin Number	Pin description
DVDD	77	Power for 3.3V pad
DGND	5	3.3V Ground
AVDD	27,40	2.5V ADC power
AVDD	23	3.3V ADC power

AGND	22,26,39	ADC Ground
AVDD5	45, 51	5V RGBDAC power
AGND5	47, 49	RGBDAC Power
AVDDR	41	5V DAC trace power
AGNDR	43	DAC trace ground
VPP	52	5V Digital I/O power
VSS	61	Ground for 5V I/O pin
VDD	13,21,25,64,80	2.5V digital Core Power & PLL power
GND	8,18,24,66	Digital Core ground & PLL ground

Pin List (80pin include power pin)

Pin Name	Pin No.	In/Out	Type	Pad Name	Description
1. Digital Video Interface					
DCLK	76	I	cmos	PDIS0C	Digital Video Input Clock
DHSYNC	9	I	cmos	PDIC0C	Digital Video Input Hsync
DVSYNC	10	I	cmos	PDIC0C	Digital Video Input Vsync
DI[7:0]	7,6,4,3,2, 1,79,78	I	cmos	PDIC0C	8-bit Digital Video data input Itís alternating between Y and Cb or Cr cycle by cycle compliant to the ITU-BT.656/601 standard
2. Serial MIC Interface					
SCK	71	I	2mA	PDIS0C	Serial Clock
SCSx	72	I	2mA	PDIS0C	Serial Interface Chip Select Active low. When 0, means a valid serial transfer cycle
SDQ	73	IO	2mA	PDB0MC0C	Serial Data Input/Output
BTYPE	67	I		PDIC0C	3-wire or 2wire select 0: 2-wire 1: 3-wire
3. LCD TCON Interface (5V compatible PAD to support Sharp panel)					
CLD/CPH*	62	O	4mA	PHT2M	Clock Signal for source driver
CTR/OEV2*	63	O	4mA	PHT2M	Control Signal for source driver
CLS/CPV*	65	O	4mA	PHT2M	Clock Signal for gate driver
SPS/STV*	60	O	4mA	PHT2M	Start signal for gate driver
SPIO/STH*	58	O	4mA	PHT2M	Start signal for source driver
OEV3	57	O	4mA	PHT2M	Panasonic panel gate driver enable 3
MOD1/OEH*	56	O	4mA	PHT2M	

<table>
<tr><td>MOD2/OEV1*</td><td>55</td><td>O</td><td>4mA</td><td>PHT2M</td><td>MOD1 and MOD2 control the line write mode for gate driver
<table>
<tr><td>MOD2</td><td>MOD1</td><td>Output Mode</td></tr>
<tr><td>0</td><td>0</td><td>No output</td></tr>
<tr><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>2 lines writing at the same time</td></tr>
<tr><td>1</td><td>1</td><td>1 line writing</td></tr>
</table></td></tr>
<tr><td>COM/VCOM*</td><td>59</td><td>O</td><td>4mA</td><td>PHT2M</td><td>COM electrode driving signal, which can be used to control the LCD brightness</td></tr>
<tr><td>L_R</td><td>53</td><td>O</td><td>2mA</td><td>PHT1M</td><td>Left and Right mirror control</td></tr>
<tr><td>U_D</td><td>54</td><td>O</td><td>2mA</td><td>PHT1M</td><td>Up and Down convert control</td></tr>
<tr><td colspan="6">4. LCD DAC Interface (5V pad)</td></tr>
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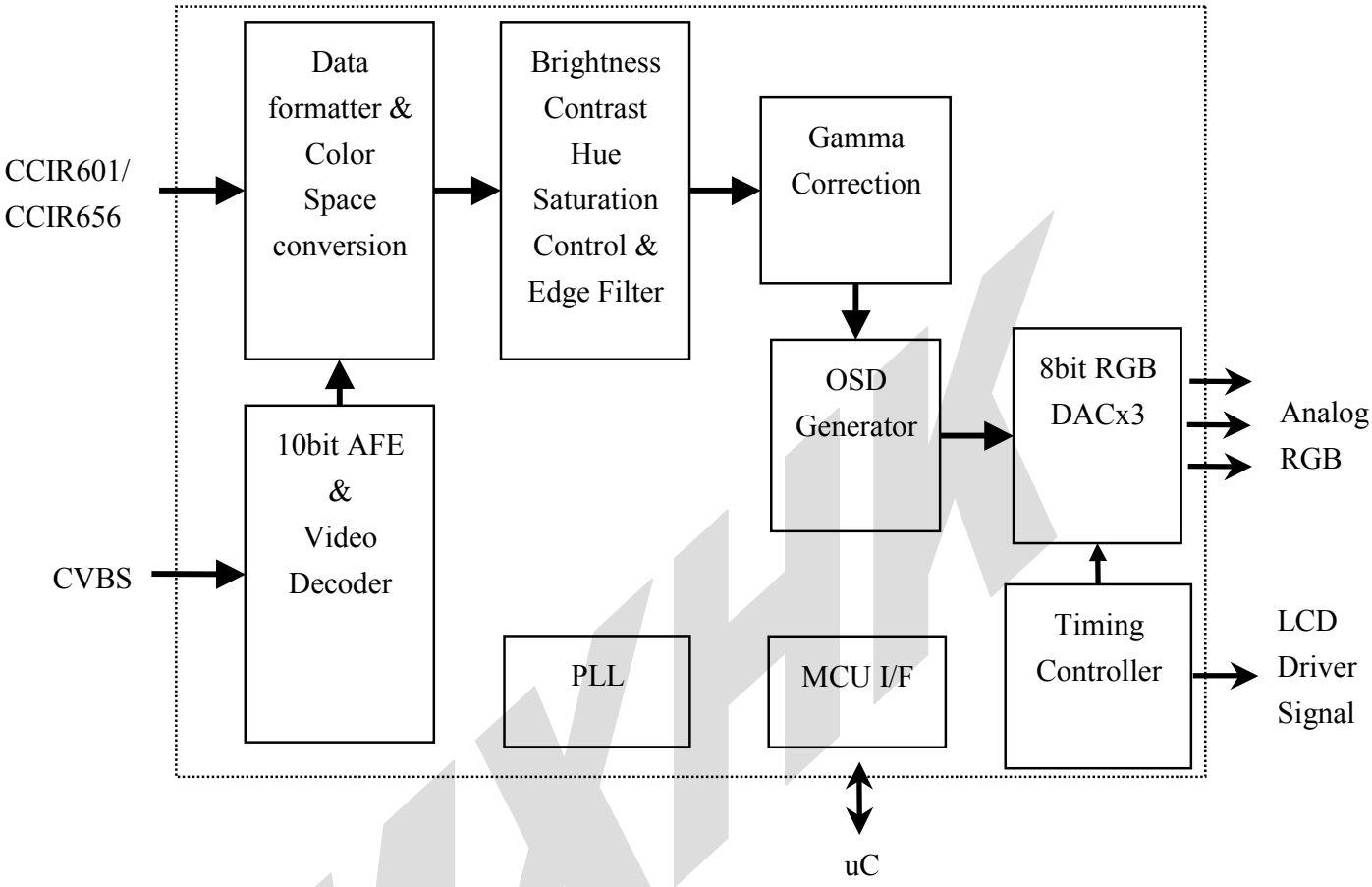
<tr><td>LCDG</td><td>48</td><td>A</td><td></td><td>PHDWNR</td><td>G component output</td></tr>
<tr><td>LCDB</td><td>46</td><td>A</td><td></td><td>PHDWNR</td><td>B component output</td></tr>
<tr><td>LVRIN</td><td>42</td><td>A</td><td></td><td>PHDWNR</td><td>Compensation signal for the LCD DACs</td></tr>
<tr><td>LVRH</td><td>44</td><td>A</td><td></td><td>PHDWNR</td><td>Capacitor complement for the LCD DACs</td></tr>
<tr><td colspan="6">5. TV input interface</td></tr>
<tr><td>TV_IN1</td><td>29</td><td>A</td><td></td><td>PADWNR</td><td>Analog Composite video input 1</td></tr>
<tr><td>TV_IN2</td><td>31</td><td>A</td><td></td><td>PADWNR</td><td>Analog Composite video input 2</td></tr>
<tr><td>TV_IN3</td><td>33</td><td>A</td><td></td><td>PADWNR</td><td>Analog Composite video input 3</td></tr>
<tr><td>ANN</td><td>32</td><td>A</td><td></td><td>PADWNR</td><td>Video input reference with 1uf capacitor to ground</td></tr>
<tr><td>VREFP</td><td>36</td><td>A</td><td></td><td>PADWNR</td><td>Internal ref voltage with 100nf capacitor to ground</td></tr>
<tr><td>VREFN</td><td>35</td><td>A</td><td></td><td>PADWNR</td><td>Internal ref voltage with 100nf capacitor to ground, parallel 100nf with 10uf capacitors between VREFP &VREFN</td></tr>
<tr><td>VCM</td><td>30</td><td>A</td><td></td><td>PADWNR</td><td>Common mode voltage with 2.2uf capacitor to ground</td></tr>
<tr><td>VBG</td><td>34</td><td>A</td><td></td><td>PADWNR</td><td>Bandgap voltage with 2.2uf capacitor to ground</td></tr>
<tr><td>IBIAS</td><td>28</td><td>A</td><td></td><td>PADWNR</td><td>Output for monitoring or input for bypass of Internal Bias Current</td></tr>
<tr><td>VBYP</td><td>37</td><td>A</td><td></td><td>PADWNR</td><td>Positive bypass PGA input voltage with 100nf</td></tr>
</table>

					capacitor to ground
VBYN	38	A		PADWNR	Negative bypass PGA input voltage with 100nf capacitor to ground
6. System Interface					
CLKIN	19	I		PDX3	**13.5 MHZ Oscillator input** (for Tcon & Tvdecoder PLL)
CLKOUT	20	O		PDX3	Oscillator output
ID0	69	I		PDIC0C	For 2-wire ID selection.
ID1	68	I		PDIC0C	For 2-wire ID selection. (MSB)
NTPALSEL	74	I		PDIC0C	0: NTSC 1: PAL
TM_CUR_3	70	I		PDIC0C	PLL test mode input ***Connect to Ground in normal operation***
SEN	75	I		PDIC0C	Scan chain enable 0: disable 1:enable ***Connect to Ground in normal operation***
RESETx	11	I		PDIS0C	Master reset signal. Active low.
TESTMD[2:0]	12,14,15	I		PDIC0C	Test Mode Select ***Connect to Ground in normal operation***
TDIO_1 TDIO_0	17,16	IO	2mA	PDB0MC0C	Test Data Input/Output ***Connect to Ground in normal operation***
7. Power/Ground					
DVDD	77		3.3V	VPPPADP1	Digital Power for 3.3V pad
DGND	5			GNDPADA	3.3V Digital Ground
AVDD	27,40		2.5V	VDDPADA 1	2.5V ADC power
AVDD	23		3.3V	VDDPADA 1	3.3V ADC Power
AGND	22,26,39			GNDPADA	ADC ground
AVDD5	45, 51		5V	V5VPPPAD A1	5V RGBDAC power
AGND5	47, 49			V5GNDPA DA	RGBDAC ground
AVDDR	41		5V	V5VPPPAD A1	5V DAC trace power

AGNDR	43			V5GNDPADA	5V DAC trace ground
VPP	52		5V	V5VPPPADP1	5V Digital I/O power
VSS	61			V5GNDPADA	Ground for 5V I/O pin
VDD	13,21,25,64,80		2.5V	VDDPADA1	2.5V core power & PLL power
GND	8,18,24,66		2.5V	GNDPADA	Digital core ground & PLL ground

Block Diagram



Register Definition

Video input formatter and Y to RGB conversion

Base address: 0x00

Address	Bit	Name	Function Description
0x00	D7	mode_sel	D7: Input data mode selection 0: CCIR_601 (default) 1: CCIR_656
	D6	clk27_inv	D6: Input Clock inversion selection 0: No inv 1: Inv clock (default)
	D5	dly	D5: Video stream delay selection (only for CCIR_601) 0: no delay (default) 1: delay 1 clock with hsync signal
	D4	vsync_pol	D4: Input vsync polarity selection 0: active low (default) 1: active high
	D3	hsync_pol	D3: Input hsync polarity selection 0: active low (default) 1: active high
	D2-1		Reserved
	D0	tv_sel	0: CCIR input (default) 1:tvdecoder input
0x01	PDNCTRL (Power Down Control)		
	D7	ntpal_control	0: ntsc_pal control from pin (default from pin) 1: ntsc_pal control from register 0x01:D6
	D6	ntpal_sel	0: ntsc (default) 1: Pal
	D5	TV_PLL_EN	Tvdecoder PLL Enable 1: Enable (default) 0: Disable when disabled CLKIN will used as tv clock

	D4	TVdecoder_EN	TV Decoder Enable 1: Enable (default) 0: Disable. When disabled, the clock input of the TV Decoder will be masked off. (tvdecoderís pll will be masked)
	D3		Reserved
	D2	LCD_EN	LCD Enable 1: Enable (default) 0: Disable. When disabled, the clock input to the LCD data path TCON and RGB DAC will be masked off.
	D1	PLL_EN	Tcon PLL Enable 1: Enable (default) 0: Disable. When disabled, the CLKIN will be selected as the PLL_CLK.
	D0	osc_en	OSC Enable 1: Enable oscillator circuit (default) 0: Disable oscillator circuit by putting the OSC pad into power down.
0x02	PLLCFGL (PLL Configuration M value) (0x02,0x03 for Tcon pll)		
	D7-0	pll_m	M value of the PLL (default value is 0x01)
0x03	PLLCFGH (PLL Configuration N value)		
	D7-0	pll_n	N value of the PLL (default value is 0x0d)
0x04	D7-0	hrst_val [7:0]	HRST_CNT count down value LOW Byte Hrst_val [7:0] of 9 bit (default value is 0x1b) hrst_cnt counter will be count down from the value of hrst_val to zero when EAV data format is detected
0x05	D7-3		Reserved
	D2-0	hrst_val [10:8]	HRST_CNT count down value HIGH Byte Hrst_val[10:8] of 11 bit (default is 0)
0x06	D7-0	hds601[7:0]	CCIR601 horizontal start low byte (default 0)

0x07	D2-0	hds601[10:8]	CCIR601 horizontal start high byte (default 0)
0x08	D7-0	hvalid_str[7:0]	Horizontal valid start point low byte (default 0)
0x09	D7		Reserved
	D6-5	tcon_vcorange	00: vco range 16.7~125 (default) 01: vco range 12.5~100 10: vco range 7.7~142.85 11: vco range 4.76~33.3
	D4	tcon_pwrdnb1	0: pll power down 1: pll power on (default)
	D3	tcon_div	0: don't divide frequency (default) 1: tcon_pll divided by 2
	D2-0	hvalid_str[10:8]	Horizontal valid start point high byte (default 0)
0x0A	D7-0	hvalid_dur[7:0]	Horizontal valid duration low byte (default 0)
0x0B	D7		Reserved
	D6-5	tv_vcorange	00: vco range 16.7~125 (default) 01: vco range 12.5~100 10: vco range 7.7~142.85 11: vco range 4.76~33.3
	D4	tv_pwrdnb1	0: pll power down 1: pll power on (default)
	D3	tv_div	0: don't divide frequency (default) 1: tv_pll divided by 2
	D2-0	hvalid_dur [10:8]	Horizontal valid duration high byte (default 0)
0x0C	D7-0	tv_pll_m	M value of the tvdecoder pll(default 0x01)
0x0D	D7-0	tv_pll_n	N value of the tvdecoder pll (default 0x03)
0x0E	D7-4	tv_current	Default 0
	D3-1	tv_si	Default 0
	D0		Reserved
0x0F	D7-4	tcon_current	Default 0
	D3-1	tcon_si	Default 0
	D0		Reserved

BIU & Output effect control (contrast, brightness, saturation, hue, Gamma, and OSD blending)

Base address: 0x10

Address	Bit	Name	Function Description
0x10	D7	burst_en	Serial bus address auto increase function 0: Enable (burst mode) 1: Disable (default)
	D6-0		Reserved
0x11	D7	contrast_en	Contrast Adjustment Enable 1: Enable 0: Disable (default)
	D6	brightness_en	Brightness Adjustment Enable 1: Enable 0: Disable (default)
	D5	saturation_en	Saturation Adjustment Enable 1: Enable 0: Disable (default)
	D4	hue_en	Hue Adjustment Enable 1: Enable 0: Disable (default)
	D3	gamma_en	GAMMA Correction Enable 1: Enable 0: Disable (default)
	D2	gamma_accen	Gammma Table set access enable 1: Enable 0: Disable (default)
	D1	sharp_en	Edge filter adjustment enable 1: Enable 0: Disable (default)
	D0		Reserved
0x12	D7-0	Coeff_C_R	Contrast Coefficient-Red, Active when Contrast_EN = 1 D7-0 = 00h ~ FFh (Power on default = 80h)

0x13	D7-0	Coeff_C_G	Contrast Coefficient-Green, Active when Contrast_EN = 1 D7-0 = 00h ~ FFh (Power on default = 80h)
0x14	D7-0	Coeff_C_B	Contrast Coefficient-Blue, Active when Contrast_EN = 1 D7-0 = 00h ~ FFh (Power on default = 80h)
0x15	D7-0	Coeff_B_R	Brightness Coefficient-Red, Active when Brightness_EN = 1 D7-0 = -128(00h) ~ 127(FFh) (Power on default = 80h)
0x16	D7-0	Coeff_B_G	Brightness Coefficient-Green, Active when Brightness_EN = 1 D7-0 = -128(00h) ~ 127(FFh) (Power on default = 80h)
0x17	D7-0	Coeff_B_B	Brightness Coefficient-Blue, Active when Brightness_EN = 1 D7-0 = -128(00h) ~ 127(FFh) (Power on default = 80h)
0x18	D7-0	Coeff_Sat	Saturation Coefficient, Active when Saturation_EN = 1 D7-0 = 00h ~ FFh(Power on default = 80h)
0x19	D7-0	Coeff_H	Hue Coefficient, active when Hue_EN = 1 D7-0 = 00h ~ FFh (power on default = 00h) 1 step means 360/256 degree
0x1A	D7-0		Reserved
0x1B	D7-0	Gamma_Dport	GAMMA Coefficient data port register
0x1C	D7	OSD_EN	OSD Enable bit 1: OSD enable 0: OSD disable (default)

	D6-5	Color_Logic	Color key alpha blending selection 00: disable color key alpha blending (default) 01: enable color key alpha blending 10: enable NOT color key alpha blending 11: not defined, reserved
	D4	Foreground_EN	OSD foreground alpha blending 0: disable (default) 1: enable
	D3	Background_EN	OSD background alpha blending 0: disable (default) 1: enable
	D2-0	Blending	OSD alpha blending mode 000: 00.0% transparency (default) 001: 12.5% transparency 010: 25.0% transparency 011: 37.5% transparency 100: 50.0% transparency 101: 62.5% transparency 110: 75.0% transparency 111: 87.5% transparency
0x1D	D7-0	ColorKey_R	Color key Red color for alpha blending (Power on default = 00h)
0x1E	D7-0	ColorKey_G	Color key Green color for alpha blending (Power on default = 00h)
0x1F	D7-0	ColorKey_B	Color key Blue color for alpha blending (Power on default = 00h)
0x20	D7	Screen_Off	Screen-Off Enable (output data set to 0) 0: Disable (Screen-On) (default) 1: Enable (Screen-Off)
	D6	Data_SEL	Output pixel data source select 0: Generate by internal frame window color set (when no signal input use) 1: Generated by input data (default)

	D5	Frame_EN	Frame window color 1: ON 0: OFF (default)
	D4-0		Reserved
0x21	D7-0	FrameCol_R	Frame window color-Red, Active when Frame_EN = 1 D7-0 = 00h ~ FFh(Power on default = 00h)
0x22	D7-0	FrameCol_G	Frame window color-Green, Active when Frame_EN = 1 D7-0 = 00h ~ FFh(Power on default = 00h)
0x23	D7-0	FrameCol_B	Frame window color-Blue, Active when Frame_EN = 1 D7-0 = 00h ~ FFh(Power on default = 00h)
0x24	D7-0	Edge filter Coefficient A	Edge filter coefficient A (default 0xE0) The most significant bit is sign bit (2ís complement) 0: positive 1: negative D6~D0: fraction part range: 0(0H) ~ 0.9921875 (7FH) -0.0078125 (FFH) ~ -1(80H)
0x25	D7-0	Edge filter Coefficient B	Edge filter coefficient B (default 0x60) D7~D6: integer part, D5~0: fraction part range: 0 (0H) ~3.984375 (FFH)
0x26	D7-0	Edge filter Coefficient C	Edge filter coefficient C (default 0xE0) The most significant bit is sign bit (2ís complement) 0: positive 1: negative D6~D0: fraction part range: 0(0H) ~ 0.9921875 (7FH) -0.0078125 (FFH) ~ -1(80H)

TCON

Base address: 0x30

Address	Bit	Name	Function Description
0x30	D7	up/down	Flip function(default 1)
	D6	left/right	Mirror function(default 1)
	D5-4	panel_sel	select the panel type 01:sharp 10:Panasonic and invert SPS 00,11: Panasonic (default)
	D3	Initial_State_Sel	Set Initial level-state of driver signals, this bit is applied to CTR/COM driver signals and FPRV signal 1: FPRV/CTR=í1í, COM =í0í 0: FPRV/CTR=í0í, COM =í1í (default)
	D2	Reg_Read_EN	Register read enable (apply to the double-register structure) 1: Enable 0: Disable(default) The data of first lever register is applied to second level register when Reg_Read_EN = 1 and TCON_VCNT_RST = 1
	D1-0	DSP_MSEL	LCD display mode selection 00: Full mode(default) 01: Normal mode 10: Cinema mode 11: Reserved
0x31	D7-0	THRST_VAL [7:0]	THRST_VAL LOW byte(default 0x0A) THRST_VAL [7:0] of 9 bits THRST_CNT counter will be count down from the value of THRST_VAL to zero when HSYNC active.
0x32	D7-1		Reserved

	D0	THRST_VAL [8]	THRST_VAL HIGH byte(default 0) THRST_VAL [8] of 9 bits
0x33	D7-0	CLS_HP_STR [7:0]	CLS_HP_STR LOW byte(default 0x09) CLS_HP_STR [7:0] of 11 bits CLS signal go to high level when TCON_HCNT is equal to CLS_HP_STR.
0x34	D7-3		Reserved
	D2-0	CLS_HP_STR [10:8]	CLS_HP_STR HIGH byte(default 0) CLS_HP_STR [10:8] of 11 bits
0x35	D7-0	CLS_HP_END [7:0]	CLS_HP_END LOW byte(default 0x1C) CLS_HP_END [7:0] of 11 bits CLS signal go to low level when TCON_HCNT is equal to CLS_HP_END.
0x36	D7-3		Reserved
		CLS_HP_END [10:8]	CLS_HP_END HIGH byte(default 0) CLS_HP_END [10:8] of 11 bits
0x37	D7-0	CLS_LP_VSTR [7:0]	CLS_LP_VSTR LOW byte(default 0x04) CLS_LP_VSTR [7:0] of 9 bits CLS_LP_VSTR is valid when CLS_MASK_EN = 1 CLS signal is masked (low level output) when **CLS_LP_VSTR > CLS_CNT > CLS_LP_VEND**
0x38	D7-1		Reserved
	D0	CLS_LP_VSTR [8]	CLS_LP_VSTR HIGH byte(default 0) CLS_LP_VSTR [8] of 9 bits
0x39	D7-0	CLS_LP_VEND [7:0]	CLS_LP_VEND LOW byte(default 0x08) CLS_LP_VEND [7:0] of 9 bits
0x3A	D7-1		Reserved
	D0	CLS_LP_VEND [8]	CLS_LP_VEND HIGH byte(default 0) CLS_LP_VEND [8] of 9 bits

0x3B	D7-0	MASK_MPLCND [7:0]	MASK_MPLCND LOW byte(default 0x0E) MASK_MPLCND [7:0] of 9 bits MASK_MPLCND is valid when CLS_MASK_EN = 1 The multiplicand of mask-CLS-formula.
0x3C	D7-1		Reserved
	D0	MASK_MPLCND [8]	MASK_MPLCND HIGH byte(default 0) MASK_MPLCND[8] of 9 bits
0x3D	D7-0	MASK_SUMAD1 [7:0]	MASK_SUMAD1 LOW byte(default 0x0C) MASK_SUMAD1 [7:0] of 9 bits MASK_SUMAD1 is valid when CLS_MASK_EN = 1 The summand of mask-CLS-formula is applied to first field.
0x3E	D7-1		Reserved
	D0	MASK_SUMAD1 [8]	MASK_SUMAD1 HIGH byte(default 0) MASK_SUMAD1[8] of 9 bits
0x3F	D7-0	MASK_SUMAD2 [7:0]	MASK_SUMAD2 LOW byte(default 0x14) MASK_SUMAD2 [7:0] of 9 bits MASK_SUMAD2 is valid when CLS_MASK_EN = 1 The summand of mask-CLS-formula is applied to first field.
0x40	D7-1		Reserved
	D0	MASK_SUMAD2 [8]	MASK_SUMAD2 HIGH byte(default 0) MASK_SUMAD2 [8] of 9 bits

0x41	D7-0	MASK_SUMAD3 [7:0]	MASK_SUMAD3 LOW byte(default 0x11) MASK_SUMAD3 [7:0] of 9 bits MASK_SUMAD3 is valid when CLS_MASK_EN = 1 The summand of mask-CLS-formula is applied to second field.
0x42	D7-1		Reserved
	D0	MASK_SUMAD3 [8]	MASK_SUMAD3 HIGH byte(default 0) MASK_SUMAD3 [8] of 9 bits
0x43	D7-0	MASK_SUMAD4 [7:0]	MASK_SUMAD4 LOW byte(default 0x17) MASK_SUMAD4 [7:0] of 9 bits MASK_SUMAD4 is valid when CLS_MASK_EN = 1 The summand of mask-CLS-formula is applied to second field.
0x44	D7-1		Reserved
	D0	MASK_SUMAD4 [8]	MASK_SUMAD4 HIGH byte(default 0) MASK_SUMAD4 [8] of 9 bits
0x45	D7-0	SPIO_HP_STR [7:0]	SPIO_HP_STR LOW byte(default 0x99) SPIO_HP_STR [7:0] of 11 bits SPIO signal go to high level when TCON_HCNT is equal to SPIO_HP_STR.
0x46	D7-3		Reserved
	D2-0	SPIO_HP_STR [10:8]	SPIO_HP_STR HIGH byte(default 0) SPIO_HP_STR [10:8] of 11 bits
0x47	D7-0	SPIO_HP_END [7:0]	SPIO_HP_END LOW byte(default 0x9E) SPIO_HP_END [7:0] of 11 bits SPIO signal go to low level when TCON_HCNT is equal to SPIO_HP_END.
0x48	D7-3		Reserved
	D2-0	SPIO_HP_END [10:8]	SPIO_HP_END HIGH byte(default 0) SPIO_HP_END [10:8] of 11 bits

0x49	D7-0	CTR_TG_STR [7:0]	CTR_TG_STR LOW byte(default 0x06) CTR_TG_STR [7:0] of 11 bits CTR signal is inverted when TCON_HCNT is equal to CTR_TG_STR.
0x4A	D7-3		Reserved
	D2-0	CTR_TG_STR [10:8]	CTR_TG_STR HIGH byte(default 0) CTR_TG_STR [10:8] of 11 bits
0x4B	D7-0	COM_TG_STR [7:0]	COM_TG_STR LOW byte(default 0) COM_TG_STR [7:0] of 11 bits COM signal is inverted when TCON_HCNT is equal to COM_TG_STR.COM signal will keep prior level when CLS_MASK_EN = 1
0x4C	D7-3		Reserved
	D2-0	COM_TG_STR [10:8]	COM_TG_STR HIGH byte(default 0) COM_TG_STR [10:8] of 11 bits
0x4D	D7-0	FPRV_TG_STR [7:0]	FPRV_TG_STR LOW byte(default 0) FPRV_TG_STR [7:0] of 11 bits FPRV (internal signal) is inverted when TCON_HCNT is equal to FPRV_TG_STR. FPRV = 0, R/G/B output is inverted FPRV = 1, R/G/B output is not inverted FPRV signal will keep prior level when CLS_MASK_EN=1
0x4E	D7-3		Reserved
	D2-0	FPRV_TG_STR [10:8]	FPRV_TG_STR HIGH byte(default 0) FPRV_TG_STR [10:8] of 11 bits
0x4F		SPS_LP_HSTR [7:0]	SPS_LP_HSTR LOW byte(default 0x06) SPS_LP_HSTR [7:0] of 11 bits SPS signal is go to low level when TCON_HCNT is equal to SPS_LP_HSTR and CLS_CNT is equal to SPS_LP_VSTR

0x50	D7-3		Reserved
	D2-0	SPS_LP_HSTR [10:8]	SPS_LP_HSTR HIGH byte(default 0) SPS_LP_HSTR [10:8] of 11 bits
0x51		SPS_LP_HEND [7:0]	SPS_LP_HEND LOW byte(default 0x2F) SPS_LP_HEND [7:0] of 11 bits SPS signal is go to high level when TCON_HCNT is equal to SPS_LP_HEND and CLS_CNT is equal to SPS_LP_VEND
0x52	D7-3		Reserved
	D2-0	SPS_LP_HEND [10:8]	SPS_LP_HEND HIGH byte(default 0) SPS_LP_HEND [10:8] of 11 bits
0x53	D7-0	SPS_LP_FVSTR [7:0]	SPS_LP_FVSTR LOW byte(default 0x12) SPS_LP_FVSTR [7:0] of 9 bits SPS_LP_FVSTR is valid for first field period. SPS signal is go to low level when TCON_HCNT is equal to SPS_LP_HSTR and CLS_CNT is equal to SPS_LP_FVSTR.
0x54	D7-1		Reserved
	D0	SPS_LP_FVSTR [8]	SPS_LP_FVSTR HIGH byte(default 0) SPS_LP_FVSTR [8] of 9 bits
0x55	D7-0	SPS_LP_FVEND [7:0]	SPS_LP_FVEND LOW byte(default 0x1F) SPS_LP_FVEND [7:0] of 9 bits SPS_LP_FVEND is valid for first field period. SPS signal is go to high level when TCON_HCNT is equal to SPS_LP_HEND and CLS_CNT is equal to SPS_LP_FVEND.
0x56	D7-1		Reserved
	D0	SPS_LP_FVEND [8]	SPS_LP_FVEND HIGH byte(default 0) SPS_LP_FVEND [8] of 9 bits

0x57	D7-0	SPS_LP_SVSTR [7:0]	SPS_LP_SVSTR LOW byte(default 0x12) SPS_LP_SVSTR [7:0] of 9 bits SPS_LP_SVSTR is valid for second field period. SPS signal is go to low level when TCON_HCNT is equal to SPS_LP_HSTR and CLS_CNT is equal to SPS_LP_SVSTR
0x58	D7-1		Reserved
	D0	SPS_LP_SVSTR [8]	SPS_LP_SVSTR HIGH byte (default 0) SPS_LP_SVSTR [8] of 9 bits
0x59	D7-0	SPS_LP_SVEND [7:0]	SPS_LP_SVEND LOW byte(default 0x1F) SPS_LP_SVEND [7:0] of 9 bits SPS_LP_SVEND is valid for second field period. SPS signal is go to high level when TCON_HCNT is equal to SPS_LP_HEND and CLS_CNT is equal to SPS_LP_SVEND.
0x5A	D7-1		Reserved
	D0	SPS_LP_SVEND [8]	SPS_LP_SVEND HIGH byte (default 0) SPS_LP_SVEND [8] of 9 bits
0x5B	D7-0	MOD1_LEN_FSTR [7:0]	MOD1_LEN_FSTR LOW byte(default 0x01) MOD1_LEN_FSTR [7:0] of 9 bits MOD1_LEN_FSTR is valid when NTSC_PAL = 0 and DSP_MSEL = 2íb10, If (MOD1_LEN_FSTR > CLS_CNT >MOD1_LEN_FEND) MOD1-Low-Enable is active in first field period
0x5C	D7-1		Reserved

	D0	MOD1_LEN_FSTR [8]	MOD1_LEN_FSTR HIGH byte(default 0) MOD1_LEN_FSTR [8] of 9 bits
0x5D	D7-0	MOD1_LEN_FEND [7:0]	MOD1_LEN_FEND LOW byte (default 0x32) MOD1_LEN_FEND [7:0] of 9 bits MOD1_LEN_FEND is valid when NTSC_PAL = 0 and DSP_MSEL = 2íb10, If (MOD1_LEN_FSTR > CLS_CNT >MOD1_LEN_FEND) MOD1-Low-Enable is active in first field period
0x5E	D7-1		Reserved
	D0	MOD1_LEN_FEND [8]	MOD1_LEN_FEND HIGH byte(default 0) MOD1_LEN_FEND [8] of 9 bits
0x5F	D7-0	MOD1_LEN_SSTR [7:0]	MOD1_LEN_SSTR LOW byte (default 0x01) MOD1_LEN_SSTR [7:0] of 9 bits MOD1_LEN_SSTR is valid when NTSC_PAL = 0 and DSP_MSEL = 2íb10, If (MOD1_LEN_SSTR > CLS_CNT>MOD1_LEN_SEND) MOD1-Low-Enable is active in second field period
0x60	D7-1		Reserved
	D0	MOD1_LEN_SSTR [8]	MOD1_LEN_SSTR HIGH(default 0) MOD1_LEN_SSTR [8] of 9 bits

0x61	D7-0	MOD1_LEN_SEND [7:0]	MOD1_LEN_SEND LOW byte (default 0xB0) MOD1_LEN_SEND [7:0] of 9 bits MOD1_LEN_SEND is valid when NTSC_PAL = 0 and DSP_MSEL = 2íb10 If (MOD1_LEN_STR > CLS_CNT > MOD1_LEN_SEND) MOD1-Low-Enable is active in second field period
0x62	D7-1		Reserved
	D0	MOD1_LEN_SEND [8]	MOD1_LEN_SEND HIGH(default 0) MOD1_LEN_SEND [8] of 9 bits
0x63	D7-0	MOD2_LP_STR [7:0]	MOD2_LP_STR LOW byte(default 0x0F) MOD2_LP_STR [7:0] of 11 bits MOD2_LP_STR is valid in the next Hor. line period of 2 lines same time writing mode. If (MOD2_LP_STR > TCON_HCNT > MOD2_LP_END) MOD2 signal will keep in low level
0x64	D7-3		Reserved
	D2-0	MOD2_LP_STR [10:8]	MOD2_LP_STR HIGH byte(default 0) MOD2_LP_STR [10:8] of 11 bits

0x65	D7-0	MOD2_LP_END [7:0]	MOD2_LP_END LOW byte(default 0x31) MOD2_LP_END [7:0] of 11 bits MOD2_LP_END is valid in the next Hor. line period of 2 lines same time writing mode. If (MOD2_LP_STR > TCON_HCNT > MOD2_LP_END) MOD2 signal will keep in low level
0x66	D7-3		Reserved
	D2-0	MOD2_LP_END [10:8]	MOD2_LP_END HIGH byte(default 0) MOD2_LP_END [10:8] of 11 bits
0x67	D7-4		Reserved
	D3-0	MOD_EN_STR	MOD1/MOD2 signals are enabling when Field-COUNTER value greater than MOD_EN_STR. (default 0x01)
0x68	D7	Meth_sel	0:99M div(default) 1: 27M clock div freq.
	D6	Oeh_mask_en	0: donít mask oeh (default) 1: mask oeh
	D5	Spio_mask_en	0: donít mask spio 1: mask spio (default)
	D4	CLD_SEL	D7=1(0: old cld, 1: new cld) D7=0(0:2div 1: 1div) (default)
	D3	CLK_SEL	CLK_SEL 0:19.95M (default) 1:27M as tcon_clock
	D2	CLS_MASK_EN	CLS mask enable 1: enable(default) 0: disable
	D1	fCLD_SEL23_EN	fCLD_SEL2/fCLD_SEL3 register enable 1: enable(default) 0: disable
	D0	fCLD_SEL14_EN	fCLD_SEL1/fCLD_SEL4 register enable 1: enable(default) 0: disable

0x69		fCLD_SEL1 [7:0]	fCLD_SEL1 LOW byte(default 0x20) fCLD_SEL1 [7:0] of 11 bits CLD signal changed clock frequency from fCLD1 into fCLD2 when TCON_HCNT is equal to fCLD_SEL1. (fCLD_SEL1 is valid when fCLD_SEL14_EN = 1)
0x6A	D7-3		Reserved
	D2-0	fCLD_SEL1 [10:8]	fCLD_SEL1 HIGH byte(default 0) fCLD_SEL1 [10:8] of 11 bits
0x6B	D7-0	fCLD_SEL2 [7:0]	fCLD_SEL2 LOW byte(default 0x60) fCLD_SEL2 [7:0] of 11 bits CLD signal changed clock frequency from fCLD2 into fCLD3 when TCON_HCNT is equal to fCLD_SEL2. (fCLD_SEL2 is valid when fCLD_SEL23_EN = 1)
0x6C	D7-3		Reserved
	D2-0	fCLD_SEL2 [10:8]	fCLD_SEL2 HIGH byte(default 0) fCLD_SEL2 [10:8] of 11 bits
0x6D	D7-0	fCLD_SEL3 [7:0]	fCLD_SEL3 LOW byte(default 0xA0) fCLD_SEL3 [7:0] of 11 bits CLD signal changed clock frequency from fCLD3 into fCLD2 when TCON_HCNT is equal to fCLD_SEL3. (fCLD_SEL3 is valid when fCLD_SEL23_EN = 1)
0x6E	D7-3		Reserved
	D2-0	fCLD_SEL3 [10:8]	fCLD_SEL3 HIGH byte(default 0) fCLD_SEL3 [10:8] of 11 bits
0x6F	D7-0	fCLD_SEL4 [7:0]	fCLD_SEL4 LOW byte(default 0xF0) fCLD_SEL4 [7:0] of 11 bits CLD signal changed clock frequency from fCLD2 into fCLD1 when TCON_HCNT is equal to fCLD_SEL4 (fCLD_SEL4 is valid when fCLD_SEL14_EN = 1)

0x70	D7-3		Reserved
	D2-0	fCLD_SEL4 [10:8]	fCLD_SEL4 HIGH byte(default 0) fCLD_SEL4 [10:8] of 11 bits
0x71			
	D7-0	fCLD_DIV1	fCLD1 clock rate is PLL-clock rate divided by fCLD_DIV1(default 0x17)
0x72			
	D7-0	fCLD_DIV2	fCLD_DIV2 is valid when fCLD_SEL14_EN or fCLD_SEL23_EN is active fCLD2 clock rate is PLL-clock rate divided by fCLD_DIV2. (default 0x09)
0x73			
	D7-0	fCLD_DIV3	fCLD_DIV3 is valid when fCLD_SEL14_EN and fCLD_SEL23_EN are active. FCLD3 clock rate is PLL-clock rate divided by fCLD_DIV3. (default 0x0B)
0x74	D7-0	OEH_HSTR[7:0]	OEH_HSTR LOW byte(default 0x0F) OEH_HSTR[7:0] of 11 bit OEH_HSTR is the horizontal start point of OEH signal for Panasonic
0x75	D7-3		Reserved
	D2-0	OEH_HSTR [10:8]	OEH_HSTR HIGH byte(default 0) OEH_HSTR [10:8] of 11 bits
0x76	D7-0	OEH_HEND[7:0]	OEH_HEND LOW byte(default 0x1F) OEH_HEND [7:0] of 11 bit OEH_HEND is the horizontal end point of OEH signal for Panasonic
0x77	D7-3		Reserved
	D2-0	OEH_HEND [10:8]	OEH_HEND HIGH byte(default 0) OEH_HEND [10:8] of 11 bits

0x78	D7-0	OEV_HSTR[7:0]	OEV_HSTR LOW byte(default 0x02) OEV_HSTR[7:0] of 11 bit OEV_HSTR is the horizontal start point of OEV signal for Panasonic
0x79	D7-3		Reserved
	D2-0	OEV_HSTR [10:8]	OEV_HSTR HIGH byte(default 0) OEV_HSTR [10:8] of 11 bits
0x7A	D7-0	OEV_HEND[7:0]	OEV_HEND LOW byte(default 0xAE) OEV_HEND [7:0] of 11 bit OEV_HEND is the horizontal end point of OEV signal for Panasonic
0x7B	D7-3		Reserved
	D2-0	OEV_HEND [10:8]	OEV_HEND HIGH byte(default 0x03) OEV_HEND [10:8] of 11 bits
0x7C	D7-0		Reserved
0x7D	D7	OEV1_mask_enable	Oev1 mask enable enable 1:enable 0:disable (default 0x01)
	D6	OEV1_OUT_INV	oev1 output select1:invert 0: donít invert (default 0)
	D5-D3		Reserved
	D2	OEH_INV_SEL	OEH output invert select 0:donít invert 1:invert (default 0)
0x7E	D7-0		Reserved
0x7F	D7	OEV2_mask_enable	oev2 mask enable 1:enable 0: disable (default 1)
	D6	OEV2_OUT_INV	oev2 output select 1:invert 0: donít invert (default 0)
	D5-0		Reserved
0x80	D7-0		Reserved
0x81	D7:	OEV3_mask_enable	oev3 mask enable 1:enable 0:disable (default 0)

	D6	OEV3_OUT_INV	oev3 mask select 1:invert 0:donít invert (default 0)
	D5-0		Reserved
0x82	D7-0		Reserved
0x83	D7-0		Reserved
0x84	D7-0		Reserved
0x85	D7-0		Reserved
0x86	D7-3		Reserved
	D2-0	CLD_MASK_STR [10:8]	CLD_MASK_STR high bits(default 0)
0x87	D7-0	CLD_MASK_STR [7:0]	CLD_MASK_STR low bits(default 0)
0x88	D7-3		Reserved
	D2-0	CLD_MASK_END [10:8]	CLD_MASK_END high bits (default 0)
0x89	D7-0	CLD_MASK_END [7:0]	CLD_MASK_END low bits(default 0)
0x8a	D7-0	DIV1_high byte	Div1 high byte when meth_sel = 0(0x68:D7) (default 0x17)
0x8b	D7-0	DIV2_high byte	Div2 high byte when meth_sel = 0(0x68:D7) (default 0x09)
0x8c	D7-0	DIV3_high byte	Div3 high byte when meth_sel = 0(0x68:D7) (default 0x0B)
0x8d	D7-1		Reserved
	D0	CLS_MASK_SEL	0: fix drop line (default) 1:round robin drop line

TV Decoder registers

Base address: 0x90

Address	Bit	Name	Function Description
0x90	TV decoder Address port (from 0x00-0x91)		
	D7-0	TV_Addrport	Used to send tvdecoder registers address

0x91	TV Decoder Data port		
	D7-0	TV_Dataport	Used to access tvdecoder registers data

TV Decoder internal registers

CVD1 Control Registers

Address	Bit	Name	Function Description
0x00	CVD1 CONTROL0		
	D7	hv_delay	This bit emulates the HV-delay mode found Sony studio monitors 0: disabled (default) 1: enabled
	D6-5	hpixel	These bits select the output display format. Standard pixels/line 00: NTSC, PAL(M) (default) 858 01: PAL(B, D, G, H, I, N, CN), SECAM 864 10: NTSC Square Pixel, PAL(M) Square Pixel 780 11: PAL(B, D, G, H, I, N) Square Pixel 944
	D4	vline_625	This bit selects the number of scan lines per frame. 0: 525 (default) 1: 625
	D3-1	colour_mode	These bits select video colour standard. 000 = NTSC (default) 001 = PAL (I, B, G, H, D, N) 010 = PAL (M) 011 = PAL (CN) 100 = SECAM
	D0	yc_src	This bit selects input video format. 0 = composite (default) 1 = S-Video (separated Y/C)
0x01	CVD1 CONTROL1		

	D7	cv_inv	This bit inverts the select signal for the analog input multiplexer during component video mode. 0 = not inverted (default) 1 = inverted
	D6	cv_src	This bit enables the component video input format. 0 = Disable the component video input (default) 1 = Component-Video (Y,Pb,Pr)
	D5-4	luma_notcha_bw	These bits select luma notch width 00 = none (default) 01 = narrow 10 = medium 11 = wide
	D3-2	chroma_bw_lo	This bit set the chroma low pass filter to wide or narrow 0 = narrow (default) 1 = wide 2 = extra wide
	D1	Chroma _burst5or10	This bit selects the burst gate width 0 = 5 subcarrier clock cycles (default) 1 = 10 subcarrier clock cycles
	D0	ped	This bit enables black level correction for 7.5 blank-to-black setup (pedestal). 0 = no pedestal subtraction 1 = pedestal subtraction (default)
0x02	CVD1 CONTROL2		
	D7	hagc_field	* 0 = off (default) 1 = on
	D6	mv_hagc	This bit, when set, automatically reduces the gain (set in register 4) by 25% when macro-vision encoded signals are detected 0 = off 1 = on (default)

	D5-4	dc_clamp_ mode	This bit sets the mode for the analog front end DC clamping 00 = auto (default) 01 = backporch only 10 = synctip only 11 = off
	D3	dagc_en	This bit, when set, enables the digital AGC. The digital AGC is used in series with the analog gain. 0 = off 1 = on (default)
	D2	agc_half_en	This bit, when set, enables the half gain mode, when unlocked, for the analog front end. 0 = off 1 = on (default)
	D1	cagc_en	This bit when set enables the chroma AGC. If disabled, then the AGC target is used to drive directly the AGC gain. 0 = off 1 = on (default)
	D0	hagc_en	** 0 = off 1 = on (default)

*When this bit is ì0î (the default), then the gain is updated once per line, after DC clamping. When this bit is set, then the gain is only updated once per field, at the start of vertical blank.

** This bit when set enables the luma/composite AGC. If disabled, then the AGC target (register 04h) is used to drive directly the AGC gain.

YC-Separation Control Registers

Address	Bit	Name	Function Description
0x03	YC_SEPARATION CONTROL		
	D7-4	Reserved	

	D3	colour_trap	This bit enables the notch-filter at the luma path after the comb filter. This filter can be turned on or off irrespective of the adaptive mode setting. 0 = Disabled (default) 1 = Enabled
	D2-0	adaptive_mode	These bits select modes for the composite signalís luma (Y) and chroma (C) separation before colour demodulation. 000 = fully adaptive comb (2-D adaptive comb) (default) 001 = vertical adaptive comb (1-D adaptive comb, vertical comb only) 010 = 5-tap adaptive comb filter (PAL mode only) 011 = basic luma notch filter mode (for very noisy and unstable pictures) 100 = simple 2-tap comb 101 = simple 3-tap comb 110 = 5-tap hybrid adaptive comb filter (PAL mode only)

Horizontal Acquisition Registers

Address	Bit	Name	Function Description
0x04	LUMA AGC VALUE		
	D7-0	hagc	* Standard — Programming Value NTSC M — DDh (221d) (default) NTSC J — CDh (205d) PAL B,D,G,H,I, COMB N, SECAM — DCh (220d) PAL M,N — DDh (221d) NTSC M (MACROVISIOIN) — A6h (166d) PAL B,D,G,H,I, COMB N (MACROVISION) — AEh (174d) If ìhagc_enî (register 02.0h) is ì0î, then ìhagcî is used to directly drive the analog gain. In this case, a value of 64 represents a unity gain, 32 represents a one-half gain, and 128 denotes a double gain.
0x05	NOISE_THRESHOLD		
	D7-0	noise_thresh	**Default = 50
0x06	AGC_GATE_THRESHOLD and ADC_SWAP		
	D7	adc_updn_swap	This bit swaps the DC clamp up/down controls to the analog front-end. 0 = Disabled (default) 1 = Enabled
	D6	adc_input_swap	This bit swaps the MSBs and LSBs from the analog front-endís ADC 0 = Disabled (default) 1 = Enabled

	D5	adc_cbcr_pump_swap	This bit swaps the Pb/Pr charge pump pairs to the analog front-end 0 = Disabled (default) 1 = Enabled
	D4-0	agc_gate_thresh	This specifies the threshold at which the rough gate generator creates a sync gate. Default = 10.

* These bits specify the luma AGC target value. The gain of the AGC is modified until the horizontal sync height is equal to this value. Note that if a MacroVision signal is detected and ìmv_hagc_modeî (02.6h) is set, then this value is automatically reduced by 25%.

** This value sets the noise value at which the circuit considers a signal noisy. The detected noise value may be read back through register 7Fh (ìstatus_noiseî). If the detected noise value is greater than ìnoise_threshî, then register bit 3C.3h (ìnoisyî) is set. Larger values of ìstatus_noiseî indicate noisier signals, so larger values of ìnoise_threshî decreases the likelihood of ìnoisyî being set while smaller values of ìnoise_threshî increases the likelihood of ìnoisyî being set.

Output Control Registers

Address	Bit	Name	Function Description
0x07	OUTPUT CONTROL		
	D7	reserved	
	D6	cbcr_swap	This bit swaps Cb/Cr outputs. 0 = donít swap Cb/Cr (default) 1 = swap Cb/Cr
	D5-4	blue_mode	This bit controls the blue screen mode. 00 = Disabled 01 = Enabled 10 = Auto (Default) 11 = reserved
	D3-0	yc_delay	* The range is [-5,7]. Default = 0

*This 2ís complement number controls the output delay between luma and chroma. Negative values shift luma outputs to the left while positive values shift luma values to the right. Luma Adjustment Registers

Address	Bit	Name	Function Description
0x08	LUMA CONTRAST ADJUSTMENT		
	D7-0	contrast	These bits control the adjustable gain to the luma output path Default = 128
0x09	LUMA BRIGHTNESS ADJUSTMENT		
	D7-0	brightness	*These bits control the adjustable brightness level to the luma output path. Default = 32

*This value is offset by -32, i.e., a value of 32 (the default) implies a brightness level of 0, and a value

of 0 implies a brightness level of -32.Chroma Adjustment Registers

Address	Bit	Name	Function Description
0x0A	CHROMA SATURATION ADJUSTMENT		
	D7-0	saturation	These bits adjust the colour saturation Default = 128
0x0B	CHROMA HUE PHASE ADJUSTMENT		
	D7-0	hue	This 2ís complement number adjusts the hue phase offset. Default = 0
0x0C	CHROMA AGC		
	D7-0	cagc	These bits set the chroma AGC target. Default = 138
0x0D	CHROMA KILL		

	D7-6	user_ckill _mode	Mode 0 uses auto hardware chroma kill, Mode 1 forces chroma kill on and Mode 2 forces chroma kill off. Default = 0
	D5	vbi_ckill	When set, chroma is killed during VBI. Default = 0
	D4	hlock_ckill	When set, chroma is killed whenever horizontal lock is lost. Default = 0
	D3-0	chroma_kill	These bits set the chroma kill level. Default = 7
0x0F	CHROMA AUTOPOSITION		
	D7-6	reserved	
	D5	fixed_burstgate	*The manual burstgate window position is defined by the burst_gate_start(0x2c) and burst_gate_end(0x2d) register. Default = 1
	D4-0	cautopos	These bits set the chroma burst gate position relative to the auto centre position Default = 12

* When set, this bit disables the burst gate autoposition.

Front End Control

Address	Bit	Name	Function Description
0x10	AGC PEAK NOMINAL		
	D7	reserved	
	D6-0	agc_peak _nominal	These bits set the luma peak white detectionís AGC nominal peak white value. This value is added to 128 and then the result is multiplied by 4 Default = 10
0x11	AGC PEAK AND GATE CONTROLS		

	D7	agc_gate_vsync _coarse	This bit forces coarse sync-tip and backporch gates to be used during vsync when VCRs are detected. Default = 1
	D6	agc_gate_vsync _stip	This bit forces sync-tip clamping during vsync. Default = 0
	D5-4	agc_gate_kill_ mode	These bits determine the method that sync-tip and backporch gates are suppressed: 00 = off 01 = enabled ñ if sync-tip gate is killed, kill backporch gate(default) 10 = enabled ñ if sync-tip gate is killed, kill backporch gate, except during vsync 11 = enabled ñ if sync-tip gate is killed, do not kill backporch gate
	D3	agc_peak_en	This bit enables the AGC peak white detector. Default = 1
	D2-0	agc_peak_cntl	These bits set the time constant for the AGC peak white detector. Default = 1
0x12	AGC GATE START (agc_gate_start[10:8])		
	D7-3	reserved	
	D2-0	agc_gate_start [10:8]	These high-order bits set the delay from the detected hsync for the rough gate generator
0x13	AGC GATE START		
	D7-0	agc_gate_start [7:0]	These low-order bits set the delay from the detected hsync for the rough gate generator Default = 1666
0x14	AGC GATE WIDTH		
	D7	reserved	
	D6-0	agc_gate_width	These bits set the width of the rough gates Default = 64
0x15	AGC BP DELAY		

	D7-0	agc_bp_delay	These bits set the time delay from the sync tip gate to the backporch gate for the rough gate generator. Default = 100

HPLL Control

Address	Bit	Name	Function Description
0x16	LOCK COUNT		
	D7-4	locked_count _noisy_max	These bits set the max value of the hlock sensor for noisy signals. 8 is added to this Default = 7
	D3-0	locked_count _clean_max	These bits set the max value of the hlock sensor for clean signals. 8 is added to this value. Default = 4
0x17	AGC PEAK AND GATE CONTROLS		
	D7-6	hlock_vsync _mode	These bits control hsync locking during vsync: 00 = disabled 01 = enabled 10 = enabled except for noisy signals 11 = enabled only for VCR signals (default)
	D5	hstate_fixed	This bit when set forces the state machine to remain in the state set in ìhstate_maxî Default = 0
	D4	disable_hfine	This bit, when set, disables the fine mode of the HPLL phase comparator. Default = 0
	D3	hstate_unlocked	This bit sets the state when unlocked. Default = 1
	D2-0	hstate_max	*If ìhstate_fixedî is set, then this register is used to force the state. Default = 3

* These bits set the maximum state for the horizontal PLL state machine. The range of this register is 0 to 5, inclusive. Higher states have a finer PLL control. Values of ì0î and ì1î should not programmed into this register.

Chroma DTO Registers

Address	Bit	Name	Function Description
0x18	CHROMA DTO INCREMENT		
	D7	cdto_fixed	This bit, when set, fixes the chroma DTO at its center frequency. Default = 0
	D6	reserved	
	D5-0	cdto_inc[29:24]	These bits contain bits 29:24 of the 30-bit-wide chroma DTO increment. Default = 0x21
0x19	CHROMA DTO INCREMENT		
	D7-0	cdto_inc[23:16]	These bits contain bits 23:16 of the 30-bit-wide chroma DTO increment. Default = 0xF0
0x1A	CHROMA DTO INCREMENT		
	D7-0	cdto_inc[15:8]	These bits contain bits 15:8 of the 30-bit-wide chroma DTO increment. Default = 0x7C
0x1B	CHROMA DTO INCREMENT		
	D7-0	cdto_inc[7:0]	These bits contain bits 7:0 of the 30-bit-wide chroma DTO increment. Default = 0x1F

Horizontal Sync DTO Registers

Address	Bit	Name	Function Description
0x1C	HORIZONTAL SYNC DTO INCREMENT		
	D7	hdto_fixed	This bit, when set, fixes the horizontal sync DTO at its center frequency. Default = 0
	D6	reserved	

	D5-0	hdto_inc[29:24]	These bits contain bits 29:24 of the 30-bit-wide horizontal sync DTO increment. Default = 0x20
0x1D	HORIZONTAL SYNC DTO INCREMENT		
	D7-0	hdto_inc[23:16]	These bits contain bits 23:16 of the 30-bit-wide horizontal sync DTO increment. Default = 00
0x1E	HORIZONTAL SYNC DTO INCREMENT		
	D7-0	hdto_inc[15:8]	These bits contain bits 15:8 of the 30-bit-wide horizontal sync DTO increment. Default = 00
0x1F	HORIZONTAL SYNC DTO INCREMENT		
	D7-0	hdto_inc[7:0]	These bits contain bits 7:0 of the 30-bit-wide horizontal sync DTO increment. Default = 00

Horizontal Sync Detection Registers

Address	Bit	Name	Function Description
0x20	HORIZONTAL SYNC RISING-EDGE OCCURRENCE TIME		
	D7-0	hsync_rising	*These bits set the position of the expected hsync rising edge Default = 62
0x21	HORIZONTAL SYNC PHASE OFFSET		
	D7-0	hsync_phase_offset	**This register sets the offset value between the coarse hsync detector and the fine hsync detector. Default = 62
0x22	HORIZONTAL SYNC DETECT WINDOW START TIME		
	D7-0	hsync_gate_start	These bits control the PLL horizontal sync detect window for coarse sync detection. This specifies the beginning of the window. Default = 0
0x23	HORIZONTAL SYNC DETECT WINDOW END TIME		

	D7-0	hsync_gate_end	These bits control the PLL horizontal sync detect window for coarse sync detection. This specifies the end of the window. Default = 128
0x24	HORIZONTAL SYNC TIP DETECT WINDOW START TIME		
	D7-0	hsync_tip_start	These bits control the PLL horizontal sync tip detect window used for AGC control. This specifies the beginning of the window. Default = -23
0x25	HORIZONTAL SYNC TIP DETECT WINDOW END TIME		
	D7-0	hsync_tip_end	These bits control the PLL horizontal sync tip detect window used for AGC control. This specifies the end of the window. Default = 15
0x26	HORIZONTAL SYNC RISING-EDGE DETECT WINDOW START TIME		
	D7-0	hsync_rising _start	These bits provide a programmable start time of the window that looks for the rising edge of the hsync. This is used by the coarse hsync detector. Default = 45
0x27	HORIZONTAL SYNC RISING-EDGE DETECT WINDOW END TIME		
	D7-0	hsync_rising _end	These bits provide a programmable end time for the window which spans across the rising-edge of the horizontal sync pulse. Default = 80
0x28	BACKPORCH INTERVAL START TIME		
	D7-0	backporch_start	These bits control the backporch detect window. This specifies the beginning of the window. Default = 34
0x29	BACKPORCH INTERVAL END TIME		
	D7-0	backporch_end	These bits control the backporch detect window. This specifies the end of the window Default = 78

0x2A	HSYNC FILTER GATE START TIME		
	D7-0	hblank_start	These bits specify the beginning of the horizontal-blank-interval window. Default = -42
0x2B	HSYNC FILTER GATE END TIME		
	D7-0	hblank_end	These bits specify the end of the horizontal-blank-interval window. Default = 78
0x2C	CHROMA BURST GATE START TIME		
	D7-0	burst_gate _start	***This specifies the beginning of the burst gate window. Default = 50
0x2D	CHROMA BURST GATE END TIME		
	D7-0	burst_gate_end	These bits specifies the end of the burst gate window Default = 70
0x2E	ACTIVE VIDEO HORIZONTAL START TIME		
	D7-0	hactive_start	****This specifies the beginning of active line. Default = 130
0x2F	ACTIVE VIDEO HORIZONTAL WIDTH		
	D7-0	hactive_width	*****These bits control the active video line time interval. Default = 80

*It is used by the fine hsync detector. The fine detector uses this time position to sample the video signal for the rising edge of the hsync.
**Nominally set to 62. The course detector actually finds the middle of the hsync so we need to subtract the nominal hsync width to find the beginning of the hsync.
***Note that this window is set to be bigger than the burst. The automatic burst position tracker finds the burst within this window.
**** These bits control the active video line time interval. This register is used to centre the horizontal position, and should not be used to crop the image to a smaller size.
*****This register specifies the width of the active line, and should not be used to crop the image to a smaller size. The value 640 is added to this register.

Vertical Sync and Field Detection Registers

Address	Bit	Name	Function Description
0x30	ACTIVE VIDEO VERTICAL START		
	D7-0	vactive_start	These bits control the first active video line in a field. This specifies the number of halflines from the start of a field. Default = 34.
0x31	ACTIVE VIDEO VERTICAL HIGHT		
	D7-0	vactive_height	These bits control the active video height. This specifies the height by the number of half lines. The value 384 is added to this register. Default = 97
0x32	VSYNC H LOCKOUT START		
	D7-0	vsync_h_min	*This register defines the number of half-lines before the vsync that the hsync detector circuit is disabled. Default = -16
0x33	VSYNC H LOCKOUT END		
	D7-0	vsync_h_max	This register defines the number of half-lines after the vsync that the hsync detector circuit is re-enabled. Default = 14
0x34	VSYNC AGC LOCKOUT START		
	D7-0	vsync_agc_min	This register defines the number of half-lines before the vsync that the AGC, SYNCTIP, and BACKPORCH gates are disabled. Default = -20
0x35	VSYNC AGC LOCKOUT END		
	D7-6	vsync_agc _mode	These bits control DC clamping during the vertical blanking interval. 00 = disabled 01 = enabled 10 = enabled except for noisy signals (default) 11 = enabled except for noisy signals and VCRs

	D5-0	vsync_agc_max	This register defines the number of half-lines after the vsync that the AGC, SYNCTIP, and BACKPORCH gates are re-enabled. Default = 16
0x36	VSYNC VBI LOCKOUT START		
	D7-0	vsync_vbi_min	This register defines the number of half-lines before the VSYNC that VBI data is valid. Default = -16
0x37	VSYNC VBI LOCKOUT END		
	D7-0	vsync_vbi_max	This register defines the number of half-lines after the VSYNC that VBI data is valid. Default = 14

*This is to make sure that the HPLL is not confused by the equalization pulses and the broad pulses. Also in VCR trick modes the VSYNC is just one 3 line wide pulse with no hsync structure so it must be ignored.

VSYNC PLL Control

Address	Bit	Name	Function Description
0x38	VSYNC_CNTL		
	D7-6	vsync_cntl	These bits set the vsync output mode 00 = output the vertical PLL vsync when the signal is noisy; otherwise use directly derived vsync (default) 01 = output the directly detected vsync 10 = output the vertical PLL derived vsync 11 = output the PLL vsync in alternate mode
	D5-0	vsync_threshold	This register specifies a relative threshold to add to the slice level for the purpose of vsync detection. Default = 0 (2ís complement value)
0x39	VSYNC TIME CONSTANT		

	D7	field_polarity	This bit sets the output field polarity. 0 ⇒ field=1 for odd fields, field=0 for even fields (default) 1 ⇒ field=0 for odd fields, field=1 for even fields
	D6	flip_field	This bit flips even/odd fields Default = 0
	D5	veven_delayed	This bit delays detection of even fields by 1 vertical line. Default = 0
	D4	vodd_delayed	This bit delays detection of odd fields by 1 vertical line. Default = 0
	D3-2	field_detect_mode	These bits control the field detection logic. Default = 2
	D1-0	vloop_tc	These bits set the vertical PLL time constant 0 = fast. Only useful if the vloop_cntl register is not 11. Internal values are 2 and 1. 1 = moderate. Internal values are 1 and º . 2 = slow. Internal values are Ω and 1/16 (default) 3 = very slow. Most useful for noisy signals. Internal values are º and Ω

Status Registers

Address	Bit	Name	Function Description
0x3A	CVD1 STATUS REGISERT 1		
	D7-5	mv _colourstripes	Macrovision colour stripes detected. The number indicates the number of colour stripe lines in each group
	D4	mv_vbi _detected	MacroVision VBI pseudo-sync pulses detection 1 = Detected 0 = Undetected

	D3	chromalock	Chroma PLL locked to colour burst 1 = Locked 0 = Unlocked
	D2	vlock	Vertical lock 1 = Locked 0 = Unlocked
	D1	hlock	Horizontal line locked 1 = Locked 0 = Unlocked
	D0	no_signal	No signal detection 1 = No Signal Detected 0 = Signal Detected
0x3B	CVD1 STATUS REGISERT 2		
	D7-1	reserved	
	D0	proscan _detected	Progressive Scan Detected
0x3C	CVD1 STATUS REGISERT 3		
	D7	vcr_rew	VCR Rewind Detected
	D6	vcr_ff	VCR Fast-Forward Detected
	D5	vcr_trick	VCR Trick-Mode Detected
	D4	vcr	VCR Detected
	D3	noisy	Noisy Signal Detected. This bit is set when the detected noise value (status register 7Fh) is greater than the value programmed into the ìnoise_threshî register (05h).
	D2	625lines _detected	625 Scan Lines Detected
	D1	SECAM _detected	SECAM Colour Mode Detected
	D0	PAL_detected	PAL Colour Mode Detected
0x70	HORIZONTAL SYNC DTO INCREMENT STATUS		
	D7-6	reserved	
	D5-0	status_hdto_inc [29:24]	These bits contain status bits 29:24 of the 30-bit-wide horizontal sync DTO increment.

0x71	HORIZONTAL SYNC DTO INCREMENT STATUS		
	D7-0	status_hdto_inc [23:16]	These bits contain status bits 23:16 of the 30-bit-wide horizontal sync DTO increment.
0x72	HORIZONTAL SYNC DTO INCREMENT STATUS		
	D7-0	status_hdto_inc [15:8]	These bits contain status bits 15:8 of the 30-bit-wide horizontal sync DTO increment.
0x73	HORIZONTAL SYNC DTO INCREMENT STATUS		
	D7-0	status_hdto_inc [7:0]	These bits contain status bits 7:0 of the 30-bit-wide horizontal sync DTO increment.
0x74	CHROMA SYNC DTO INCREMENT STATUS		
	D7-6	reserved	
	D5-0	status_cdto_inc [29:24]	These bits contain status bits 29:24 of the 30-bit-wide chroma sync DTO increment.
0x75	CHROMA SYNC DTO INCREMENT STATUS		
	D7-0	status_cdto_inc [23:16]	These bits contain status bits 23:16 of the 30-bit-wide chroma sync DTO increment.
0x76	CHROMA SYNC DTO INCREMENT STATUS		
	D7-0	status_cdto_inc [15:8]	These bits contain status bits 15:8 of the 30-bit-wide chroma sync DTO increment.
0x77	CHROMA SYNC DTO INCREMENT STATUS		
	D7-0	status_cdto_inc [7:0]	These bits contain status bits 7:0 of the 30-bit-wide chroma sync DTO increment.
0x78	AGC ANALOG GAIN STATUS		
	D7-0	agc_again	These bits contain the analog AGC gain value.
0x79	AGC DIGITAL GAIN STATUS		
	D7-0	agc_dgain	These bits contain the digital AGC gain value.
0x7A	CHROMA MAGNITUDE STATUS		
	D7-0	status_cmag	These bits contain the chroma magnitude.
0x7B	CHROMA GAIN STATUS		
	D7-6	reserved	
	D5-0	status_cgain [13:8]	These bits contain the high order of the chroma gain.
0x7C	CHROMA GAIN STATUS		

	D7-0	status_cgain [7:0]	These bits contain the low order of the chroma gain.
0x7D	CORDIC FREQUENCY STATUS		
	D7-0	status_cordiq _frerq	These bits contain the SECAM cordic frequency.
0x7F	CVD1 STATUS		
	D7-0	status _noise	This registers indicates how noisy the signal is. Larger values indicate noisier signals. This register is used in conjunction with programmable register 05h, ì noise_threshî and status bit 3C.3h, ì noisyî .

Luma Peaking Registers

Address	Bit	Name	Function Description
0x80	LUMA PEAKING		
	D7-6	Reserved	
	D5-4	peak_range	These bits set the range of peak_gain. Setting peak_range value 00 1 (default) 01 2 10 4 11 8 Ypeak = Y + YH *(peak_gain/peak_range) where Y is the luma and YH is the high frequency luma only
	D3-1	peak_gain	These bits set the gain for the luma horizontal peaking control. This allows adjustable gain to the luma around the colour subcarrier frequency. Default = 2
	D0	peak_en	This bit enables the luma horizontal peaking control around the colour subcarrier frequency 0 = Disabled (default) 1 = Enabled

Comb Filter Configuration Registers

Address	Bit	Name	Function Description
0x82	CVD1 COMB FILTER CONFIG		
	D7	reserved	
	D6	pal_perr	This bit is used to reduce phase-error artifacts in the comb filterís luma-path. It should be set for VCR signals. Default = 1
	D5	pal_perr _auto_en	When set, this will turn on the pal_perr when VCR signals is detected. Default = 0
	D4	comb_wide _band	This bit is used to select the bandpass filter used in the comb-filter. This should be set to 1 for PAL mode. Default=0
	D3-2	reserved	
	D1-0	palsw_level	This bit is used to determine how many incorrect lines are used for the pal switch circuit before switching. Use a higher level for noisy signals. Default = 2

Chroma-Lock Configuration Registers

Address	Bit	Name	Function Description
0x83	CVD1 CHROMA_LOCK CONFIG		
	D7-4	lose_chromaloc k_count	This register is used to tune the chromakill, higher values are more sensitive to losing lock. Default = 6
	D3-1	lose_chromaloc k_level	Set the level for chromakill. Default = 7

	D0	lose_chromalock_ckill	When set, chroma is killed whenever chromlock is lost. Default = 1

Comb Filter Threshold Registers

Address	Bit	Name	Function Description
0x84	CVD1 COMB FILTER THRESHOLD1		
	D7-0	noise_ntsc_c	These register bits are used to tune the noise_threshold used by the comb filter for NTSC. Default = 7.
0x85	CVD1 COMB FILTER THRESHOLD2		
	D7-0	noise_pal_c	These register bits are used to tune the noise_threshold used by the comb filter for PAL. Default = 32
0x86	CVD1 COMB FILTER THRESHOLD3		
	D7-0	noise_phase_c	These register bits are used to tune the noise_threshold used by the chroma comb filter. Default = 3
0x87	CVD1 COMB FILTER THRESHOLD4		
	D7-0	noise_phase_y	These register bits are used to tune the noise_threshold used by the luma comb filter. Default = 16
0x8A	CVD1 CHROMA LOOPFIL STATE		
	D7-4	reserved	
	D3-1	cstate	This register sets the chroma loopfilter bandwidth state, larger state has a slower response. Default = 5
	D0	fixed_state	This register fixes the state of chroma loopfilter to cstate. Default=0

Hresampler Control Registers

0x8B	CVD1 CHROMA HRESAMPLER CONTROL		
	D7-1	reserved	
	D0	hresampler_2up	Upsample the chroma by 2 before going into the hresampler. Default=1

Charge-Pump Delay Registers

0x8D	**CVD1 CHARGE PUMP DELAY CONTROL**		
	D7-2	cpump_adjust_delay	Delay, relative to charge-pump pulses, before adjustment, used to compensate for possible visible artefacts caused by charge-pump pulses, is applied. Default = 10.
	D1	cpump_adjust_polarity	Polarity of adjustment used to compensate for possible visible artefacts caused by charge-pump pulses. Default = 0 (normal polarity).
	D0	cpump_delay_en	Enable delay of charge-pump up/down pulses. Default = 0 (disabled)
0x8E	**CVD1 CHARGE PUMP ADJUSTMENT**		
	D7-0	cpump_adjust	Value used to compensate for possible visible artefacts caused by charge-pump pulses. Default = 200.
0x8F	CVD1 CHARGE PUMP DELAY		
	D7-0	cpump_delay	If ì cpump_delay_en == 1î, then the charge pump up/down pulses are delayed by ì4Ý cpump_delayî output pixels. Default = 185 ➔ 740 output pixel delay.

Reset Register

Address	Bit	Name	Function Description
0x3F	CVD1 RESET REGISTER		
	D7-1	reserved	
	D0	soft_rst	Soft Reset

ADC Control Register

Address	Bit	Name	Function Description
0x90	ADC CONTROL 1		
	D7-6	ansel1..ansel0	Multiplexer Channel Input selector 00: an0(Input to channel) (Default) 01: an1 10: an2 11: reserve
	D5-3	Pga2..pga0	PGA Input Gain settings PGA[2:0] Gain Setting 000 0.75 (Default) 001 1.25 010 1.5 011 2 100 2.5 101 3 110 3.5 111 4
	D2-1	da1..da0	Channel DAC Clamp Current Setting Da1 da0 Charge(mA) Discharge(mA) 0 0 0.5 0.5 (Default) 0 1 1 1 1 0 2 2 1 1 4 4
	D0	swann	External Analog input Reference select Default = 0
0x91	ADC CONTROL 2		

	D7-6	reserved	
	D5	ench	Channel Power Down Default = 1 *1
	D4	envbg	Power On for Bandgap Generator Default = 1 *1
	D3	enref	Power On for Reference Generator Default = 1 *1
	D2	envcm	Power On for Reference Generator Default = 1 *1
	D1	swib	External Current Reference selector Default = 0 *1
	D0	bypass	Bypass PGA for testing purpose only Default = 0 *1

*1

Mode	***Objective***	***ench***	***envbg***	***enref***	***envcm***	***swib***	***bypass***
0	Complete Power Down	0	0	0	0	0	X
1	Normal operating mode with the three channels active	1	1	1	1	0	0
2	Normal operation with bypass of internal bandgap	1	0	1	1	0	0
3	Normal operation with bypass of internal vcm buffer	1	1	1	0	0	0
4	Normal operation with bypass of internal vrefn and vrefp	1	1	0	1	0	0
5	Normal operation with external bias current generation	1	1	1	1	1	0
6	Bypass of Luma PGA-S/H (testing purposes only)	1	x	x	x	x	1

OSD External registers

Base address: 0xA0

Address	Bit	Name	Function Description
0xA0	AddrLSBSel (LSB bit of internal OSD address) The meaning of this register depends of Reg. 0xA4[1:0] (default = 0)		
	bit	0xA4[1:0]	Reg. 0xA0 description
	D7-0	00	Starting address of Internal OSD control register
	D5-0	01	Starting char code of internal OSD font table RAM
	D5-0	10	Starting address of Internal OSD display code buffer
	D5-0	11	Starting address of Internal OSD display attribute buffer
0xA1	AddrMSBSel (MSB bit of internal OSD address) The meaning of this register depends of reg. 0xA4[1:0](default = 0)		
	bit	0xA4[1:0]	Reg. 0xA1 description
		00	Not used
	D4-0	01	Starting char scan line of internal OSD font table RAM
		10	Not used
		11	Not used
0xA2	DataLSBSel (LSB bit of internal OSD data port) The meaning of this register depends of reg. 0xA4[1:0](default = 0)		
	bit	0xA4[1:0]	Reg. 0xA2 description
	D7-0	00	Internal OSD control register data port
	D7-0	01	Internal OSD font table RAM LSB 8 bit data port
	D7-0	10	Internal OSD display code buffer data port
	D7-0	11	Internal OSD display attribute buffer data port
0xA3	DataMSBSel (MSB bit of internal OSD data port) The meaning of this register depends of reg. 0xA4[1:0](default = 0)		
	bit	0xA4[1:0]	Reg. 0xA3 description
		00	Not used
	D3-0	01	Internal OSD font table RAM MSB 4 bit data port
		10	Not used
		11	Not used
0xA4	ORWCtrl (OSD Read/Write control) (default = 8íb0)		

	D7	burstmode	Internal OSD read/write mode select 0: single mode (default) 1: burst mode enable
	D6	clrpulse (Write Only)	Internal OSD clear buffer bit 0: normal (default) 1: clear code buffer with 0x3e clear attribute buffer with 0x00
	D5	rwmode	Indicates read/write mode, ì1î is read mode, ì0î is write mode.
	D4-3		Reserved
	D2	accosd	Internal OSD Read/Write enable 0: enable accessing internal OSD registers and buffer (default) 1: disable
	D1-0	accsel	Internal OSD accessing select 00: internal OSD control register (default) 01: internal OSD RAM font buffer 10: internal OSD display code buffer 11: internal OSD display attribute buffer

OSD internal control register:

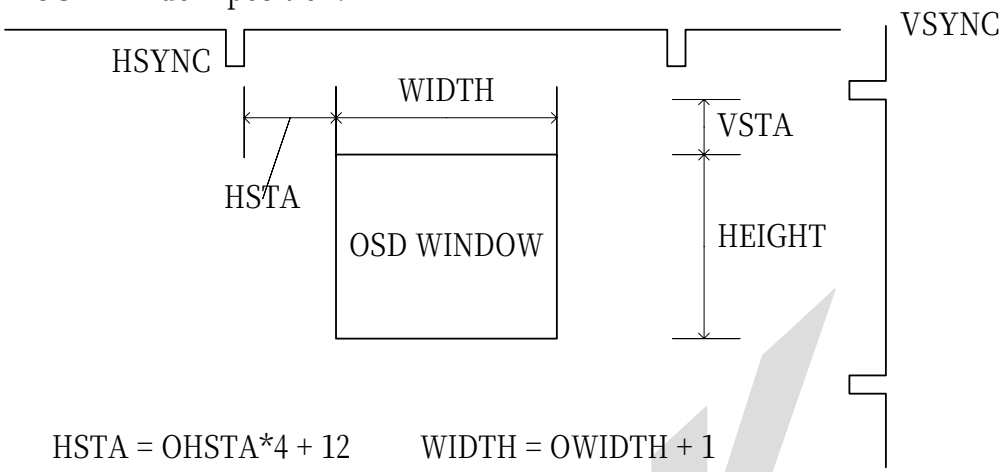
INDEX	R/W	DESCRIPTION
0x00	R/W	OHSTA (OSD window horizontal start position) (default value is 0x50) Start position = 4*OHSTA +12(pixel)
0x01	R/W	OVSTA (OSD window vertical start position) (default value is 0x10) Start position = 4*OVSTA+1 (line)
0x02	R/W	D5-0: OWIDTH (OSD window horizontal width) (default value is 0x07) Display width = OWIDTH+1(char)
0x03	R/W	(default value is 0x07) D7-4: OVSTP (OSD vertical space start position)(unit: char) D3-0: OHEIGHT (OSD window vertical height) Display height = OHEIGHT+1(char)
0x04	R/W	D5-0: OHSTP (OSD horizontal space start position) (unit: char)

INDEX	R/W	DESCRIPTION
		(default value is 0x00)
0x05	R/W	OSPW (OSD space width) (default value is 0x00) Space width = 8*OSPW (pixel)
0x06	R/W	OSPH (OSD space height) (default value is 0x00) Space height = 8*OSPH (line)
0x07	R/W	OSD control register (default value is 0x22) D7-6: OVS (vertical scaling) 00: vertical enlarged x1 by repeated pixels(default) 01: vertical enlarged x2 by repeated pixels 10: vertical enlarged x3 by repeated pixels 11: vertical enlarged x4 by repeated pixels D5-4: OHS (horizontal scaling) 00: horizontal enlarged x1 by repeated pixels 01: horizontal enlarged x2 by repeated pixels 10: horizontal enlarged x3 by repeated pixels(default) 11: horizontal enlarged x4 by repeated pixels D3-2: Reserved D1: Type of character border 0: all direction font boundary 1: bottom-right font boundary(default) D0: OSD window display 0: Main OSD window OFF(default) 1: Main OSD window ON
0x08	R/W	OSD misc. control D7-D5: Reserved D4: Border width control if font scale up 0: one pixel width for all scale 1: scale with OVS and OHS(default) D3-D0: Reserved
0x09	R/W	D7: code buffer offset selector (default value is 0x00) 0: code buffer offset is equal to OWIDTH (IREG 0x02) (default) 1: code buffer offset is equal to OOFFSET [5:0] D6: Reserved

INDEX	R/W	DESCRIPTION
		D5-0: OOFFSET, code buffer offset value(default 0)
0x0A	R/W	D5-0:OSD code base (default value is 0x00)
0x0B	R/W	OSD blink period (default value is 0x20)
0x0C	R/W	OSD red color 0 (default value is 0x90)
0x0D	R/W	OSD green color 0(default value is 0xf0)
0x0E	R/W	OSD blue color 0 (default value is 0x0a)
0x0F	R/W	OSD red color 1 (default value is 0xff)
0x10	R/W	OSD green color 1(default value is 0x00)
0x11	R/W	OSD blue color 1 (default value is 0x00)
0x12	R/W	OSD red color 2 (default value is 0x00)
0x13	R/W	OSD green color 2(default value is 0xff)
0x14	R/W	OSD blue color 2 (default value is 0x00)
0x15	R/W	OSD red color 3 (default value is 0x00)
0x16	R/W	OSD green color 3(default value is 0x00)
0x17	R/W	OSD blue color 3 (default value is 0xff)
0x18	R/W	OSD red color 4 (default value is 0xff)
0x19	R/W	OSD green color 4(default value is 0xff)
0x1A	R/W	OSD blue color 4 (default value is 0x00)
0x1B	R/W	OSD red color 5 (default value is 0x00)
0x1C	R/W	OSD green color 5(default value is 0xff)
0x1D	R/W	OSD blue color 5 (default value is 0xff)
0x1E	R/W	OSD red color 6 (default value is 0xff)
0x1F	R/W	OSD green color 6(default value is 0x00)
0x20	R/W	OSD blue color 6 (default value is 0xff)
0x21	R/W	OSD red color 7 (default value is 0x00)
0x22	R/W	OSD green color 7(default value is 0x00)
0x23	R/W	OSD blue color 7 (default value is 0x00)
0x24	R/W	OSD border red color (default value is 0x80)
0x25	R/W	OSD border green color (default value is 0xa0)
0x26	R/W	OSD border blue color (default value is 0x60)

OSD window and register define

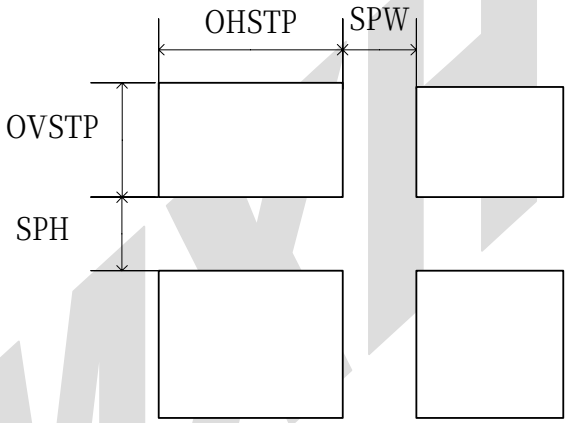
OSD window position:



HSTA = OHSTA*4 + 12　　WIDTH = OWIDTH + 1

VSTA = OVSTA*4 + 1　　HEIGHT = OHEIGHT + 1

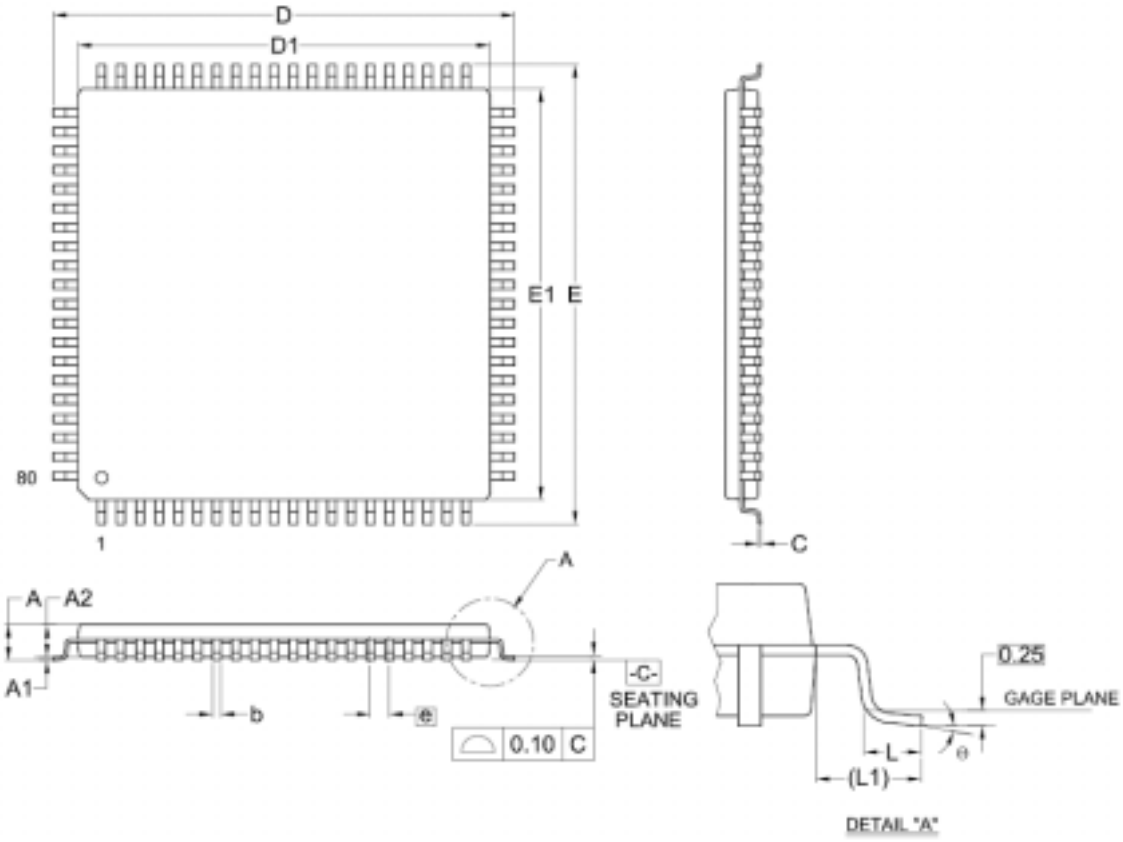
SPACE:



SPW = OSPW * 8

SPH = OSPH *8

Package outline:



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	E1	e	L	L1	Θ
mm	Min.	---	0.05	1.35	0.13	0.09	11.80	9.90	11.80	9.90		0.45	0.85	0
	Nom.	---	0.10	1.40	0.16	0.13	12.00	10.00	12.00	10.00	0.40	0.60	1.00	3.5
	Max.	1.60	0.15	1.45	0.23	0.20	12.20	10.10	12.20	10.10		0.75	1.15	7
Inch	Min.	---	0.002	0.053	0.005	0.004	0.465	0.390	0.465	0.390		0.018	0.033	0
	Nom.	---	0.004	0.055	0.006	0.005	0.472	0.394	0.472	0.394	0.016	0.024	0.039	3.5
	Max.	0.063	0.006	0.057	0.009	0.008	0.480	0.398	0.480	0.398		0.030	0.045	7