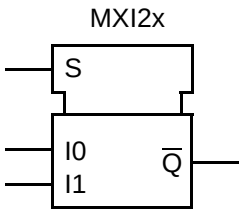
Description

MXI2x is a family of inverting two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

HDL Syntax

Verilog ..... MXI2x *inst_name* (QN, I0, I1, S);

VHDL..... *inst_name*: MXI2x port map (QN, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MXI21	MXI22	MXI24	MXI26
I0	1.0	1.0	1.0	1.0
I1	1.0	1.0	1.0	1.0
S	2.2	2.2	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MXI21	4.0	TBD	7.2
MXI22	4.0	TBD	9.0
MXI24	7.0	TBD	13.1
MXI26	8.0	TBD	19.3

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
MXI21	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.47 0.45	0.56 0.56	0.68 0.68	0.82 0.83	0.93 0.95
	From: S To: QN	t_{PLH} t_{PHL}	0.59 0.52	0.68 0.62	0.80 0.73	0.93 0.88	1.03 1.00
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
MXI22	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.50 0.49	0.62 0.61	0.72 0.72	0.81 0.82	0.92 0.93
	From: S To: QN	t_{PLH} t_{PHL}	0.60 0.55	0.71 0.66	0.82 0.77	0.92 0.87	1.03 0.99
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
MXI24	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.48 0.48	0.62 0.62	0.72 0.74	0.81 0.85	0.90 0.95
	From: S To: QN	t_{PLH} t_{PHL}	0.58 0.56	0.71 0.67	0.84 0.79	0.94 0.91	1.02 1.03
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
MXI26	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.52 0.51	0.65 0.64	0.75 0.73	0.87 0.83	1.01 0.95
	From: S To: QN	t_{PLH} t_{PHL}	0.64 0.56	0.76 0.69	0.87 0.80	0.99 0.90	1.11 1.00

Delay will vary with input conditions. See page 2-17 for interconnect estimates.