Data Sheet

MxL214C

Full-Spectrum Capture™ Cable Receiver SoC with Wideband IF Output and Four Transport Stream Outputs

General Description

The MxL214C is a gateway front-end System on a Chip (SoC) that supports four downstream DOCSIS channels and four video channels. The MxL214C targets DOCSIS 2.0/3.0 Video Gateway designs.

The MxL214C IC captures the full 1GHz cable bandwidth, and can tune to any eight channels in the cable spectrum. The IC provides up to four MPEG Transport Streams (TSs), and up to four more channels at its wideband IF output.

With its high integration and low-power consumption, the MxL214C enables a single-chip DOCSIS 2.0/3.0 and video receiver solution with a compact board design and low Bill-Of-Materials (BOM) costs.

The IC is controlled via one of two I^2C interfaces and operates using 3.3V, 1.8V, and 1.1V supplies. The MxL214C is available in a small, 7mm x 7mm footprint, 48-pin QFN package.

Applications

High-performance receiver for digital cable applications such as:

- DOCSIS 2.0/3.0 and video gateways
- Fast channel change Digital Transport Adapter (DTA)

Features

- Full-Spectrum Capture™ (FSC™) cable receiver capable of receiving Quadrature Amplitude Modulation (QAM) channels from 44MHz to 1002MHz, without external Surface Acoustic Wave (SAW) filters
- Supports up to eight downstream channels:
  - Four serial MPEG TS outputs
  - Four channels in a wideband IF output
- Power consumption of:
  - 1.84W in a four-channel video, plus four-channel IF mode
  - 475mW in single-channel Power Save Mode (PSM)
- Full cable band power spectrum reporting
- Configurable PID filtering to support Autonomous Network Wakeup™
- Dual I^2C-compatible digital control interfaces allow control from two independent hosts

Supported Standards

The MxL214C is compliant to the following standards:

- ITU-T J.83
  - Annex A (DVB-C), Annex C
  - Annex B (US Cable)
- DOCSIS 3.0, 2.0
- EuroDOCSIS 3.0, 2.0

Revision History

Revision No.	Release Date	Change Description
010-214CDSR01	06/11/14	Initial release.

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Introduction

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IC Block Diagram

Figure 1 shows a functional block diagram of the MxL214C. The device has an FSC™ tuner that covers the frequency range of 44MHz to 1002MHz, with four QAM demodulators. The MxL214C can output four independent MPEG TSs, and one wideband IF signal. A narrowband tuner enables the implementation of low power modes.

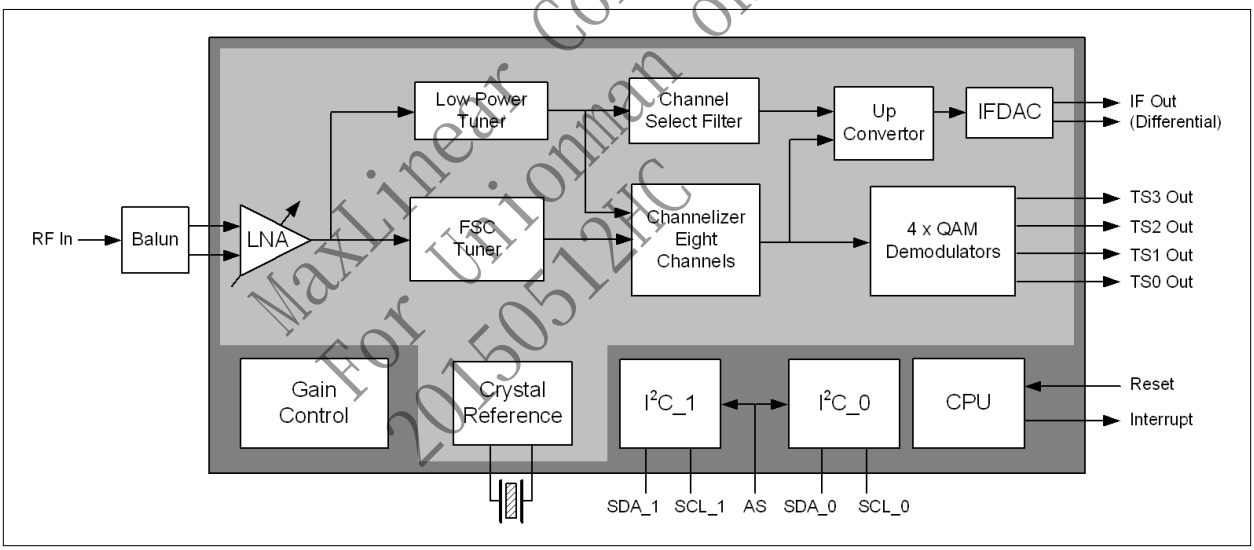


Figure 1: Simplified Block Diagram

Typical Application

The following figure shows a typical application of the MxL214C.

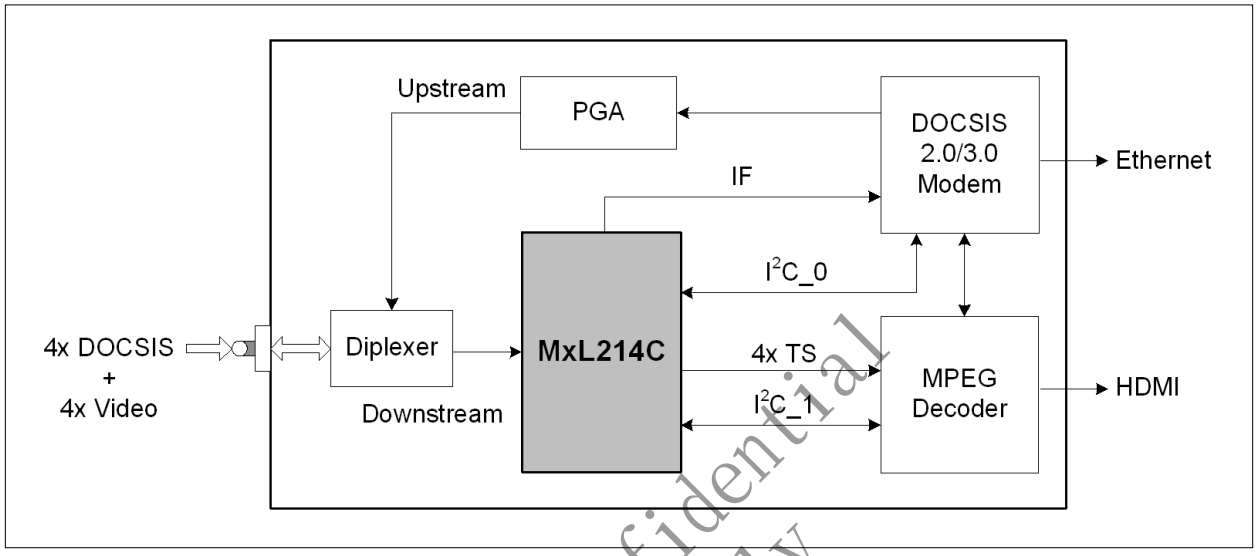


Figure 2: MxL214C Typical Application

Pin Information

Pin Configuration

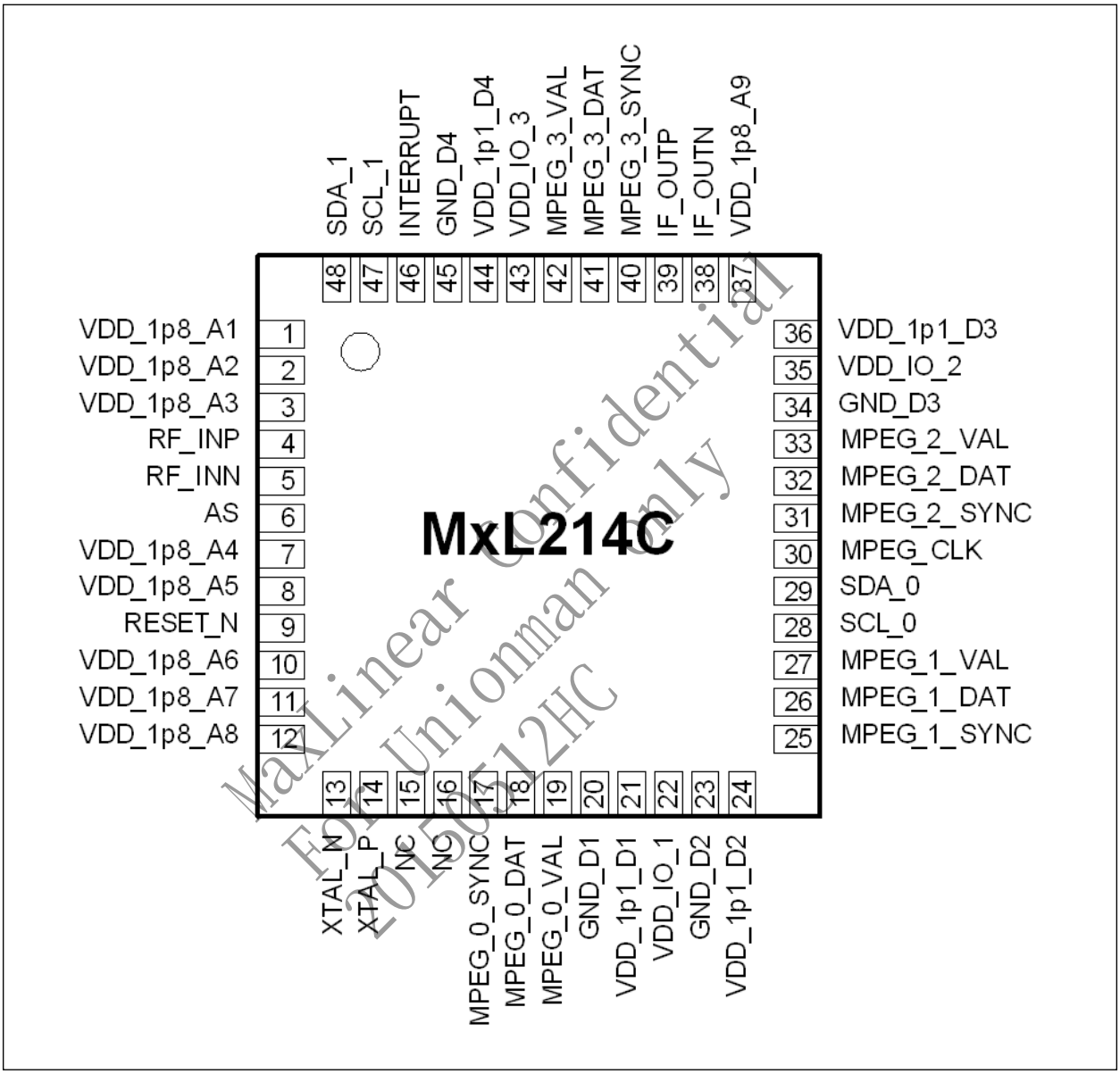


Figure 3: Pin Configuration (Top View)

Pin Description

Pin Names

Table 1: Pin Names

Pin #	Pin Name	Pin #	Pin Name
1	VDD_1p8_A1	25	MPEG_1_SYNC
2	VDD_1p8_A2	26	MPEG_1_DAT
3	VDD_1p8_A3	27	MPEG_1_VAL
4	RF_INP	28	SCL_0
5	RF_INN	29	SDA_0
6	AS	30	MPEG_CLK
7	VDD_1p8_A4	31	MPEG_2_SYNC
8	VDD_1p8_A5	32	MPEG_2_DAT
9	RESET_N	33	MPEG_2_VAL
10	VDD_1p8_A6	34	GND_D3
11	VDD_1p8_A7	35	VDD_IO_2
12	VDD_1p8_A8	36	VDD_1p1_D3
13	XTAL_N	37	VDD_1p8_A9
14	XTAL_P	38	IF_OUTN
15	NC	39	IF_OUTP
16	NC	40	MPEG_3_SYNC
17	MPEG_0_SYNC	41	MPEG_3_DAT
18	MPEG_0_DAT	42	MPEG_3_VAL
19	MPEG_0_VAL	43	VDD_IO_3
20	GND_D1	44	VDD_1p1_D4
21	VDD_1p1_D1	45	GND_D4
22	VDD_IO_1	46	INTERRUPT
23	GND_D2	47	SCL_1
24	VDD_1p1_D2	48	SDA_1

RF Interface

The MxL214C RF interface consists of a differential signal input (RF_IN).

Table 2: RF Interface

Pin Name	Direction	Description
RF_INP RF_INN	Input	LNA differential inputs; 75Ω differential impedance.

IF Interface

The MxL214C IF interface consists of a differential wideband IF output (IF_OUT).

Table 3: IF Interface

Pin Name	Direction	Description
IF_OUTP IF_OUTN	Output	Differential IF outputs; Typical differential load is 4kΩ, 9pF.

MPEG Interface

In the four-wire TS interface, the following four MPEG signals are used to convey information:

- Clock
- Data = A serial bit stream that is clocked by MPEG CLK and organized as 188-byte packets.
- Sync = Asserted concurrent with the first byte (the sync byte) of each packet.
- Valid = A clock-gating signal that is asserted for the entire 188-byte packet, and de-asserted between packets for one or more turnaround clock cycles.

The following figure shows the timing waveforms for the four-wire interface.

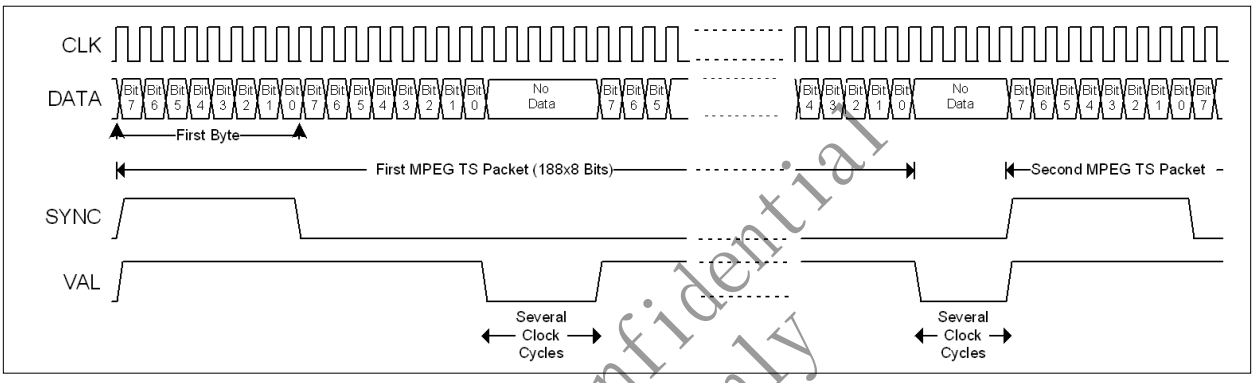


Figure 4: MPEG Serial Four-Wire Interface

The serial interface has the following features:

- MPEG clock frequencies are configurable to:
  - 112.5MHz
  - 84.375MHz
  - 56.25MHz
  - 42.1875MHz

  The configured frequency must be greater than the QAM demodulator data throughput.
- MPEG data output can be programmed as either MSB first or LSB first.
- Data may be clocked by either the rising or falling edge of the clock.
- The polarity of the MPEG Valid and MPEG Sync signals can be inverted.

Table 4: MPEG Serial Four-Wire Interface

Pin Name	Direction	Mode	Description
MPEG_<0-3>_VAL	Output	Serial	MPEG Valid signal for TS<0-3>.
MPEG_<0-3>_SYNC	Output	Serial	MPEG Sync signal for TS<0-3>.
MPEG_<0-3>_DAT	Output	Serial	MPEG Serial Data for TS<0-3>.
MPEG_CLK	Output	Serial	MPEG Clock for TS<0-3>.

I²C Interface

The MxL214C is controlled through one of two I²C interfaces. One of four I²C addresses (0x50–0x53) is assigned by applying a suitable voltage to the Address Select (AS) pin, as specified in Table 25 on page 18 (under "Appendix") and the *MxL214C Reference Design Guide*. Both I²C interfaces are assigned the same I²C address. The SCL_0/1 and SDA_0/1 are open-drain pins and should be pulled-up to VDD_IO using a 4.7kΩ resistor. The MxL214C can be controlled by either of the two I²C interfaces. The SCL_0/SDA_0 is the primary I²C interface, and firmware can only be downloaded using this interface. After the firmware downloads, SCL_1/SDA_1 is enabled. Transactions are handled on a first-come, first-serve basis. This dual I²C facilitates system configurations that involve two hosts (e.g., DOCSIS and video hosts).

Table 5: I²C Interface

Pin Name	Direction	Type	Description
AS	Input	Analog	I²C Address Select (AS).
SCL_0/1	Bi-directional	Digital	I²C clock.
SDA_0/1	Bi-directional	Digital	I²C data.

Supply and Ground

The following table lists the VDD supplies required for normal operation.

Table 6: Supply and Ground

Pin Name	Description
VDD_1p8_A<1-9>	1.8V supply for analog circuits.
VDD_1p1_D<1-4>	1.1V supply for digital circuits.
VDD_IO_<1-3>	Supply for I/O buffers.
GND_D<1-4>	Ground.

Crystal and Clock

Table 7: Crystal Pins

Pin Name	Direction	Description
XTAL_P	Input	Xtal plus.
XTAL_N	Output	Xtal minus.

Interrupt

The MxL214C has one interrupt pin that can be used to alert the host processor of the following six events:

- FEC lock/unlock
- QAM lock/unlock
- MPEG lock/unlock.

Table 8: Interrupt Pin

Pin Name	Direction	Description
Interrupt	Output	Interrupt pin.

Reset

The MxL214C has a single asynchronous active-low reset.

Table 9: Reset Pin

Pin Name	Direction	Description
RESET_N	Input	Global asynchronous reset.

No Connect

Leave pins marked *NC* unconnected.

Table 10: No Connect Pins

Pin Name	Direction	Description
NC	No connect	Do not connect.

MxL214C Specifications

Absolute Maximum Ratings

Important! The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the required operating conditions for extended periods of time may affect device reliability. Solder reflow profile is specified in the IPC/JEDEC J-STD-020C standard.

Table 11: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
All 1.8V Supply	–0.3	1.98	V
All 1.1V Supply	–0.3	1.21	V
VDD_IO	–0.3	3.63	V
Digital IOs	–0.3	3.63	V
Storage Temperature	–55	150	°C
Soldering Temperature	-	260	°C
Junction Temperature T_J	-	150	°C
Input Signal Power	-	10	dBm

Required Operating Conditions

Table 12: Required Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
All 1.8V Supply	VDD_1p8_Ax	1.7	1.8	1.9	V
All 1.1V Supply	VDD_1p1_Dx	1.05	1.1	1.14	V
VDD_IO Supply (3.3V Mode)	VDD_IO_x	3.15	3.3	3.5	V
VDD_IO Supply (1.8V Mode)	VDD_IO_x	1.7	1.8	1.9	V
Reset	RESET_N	0	-	VDD_IO	V
I^2C AS	AS	0	-	1.9	V
Ambient Temperature	T_A	0	25	70	°C
Operating Junction Temperature	T_J	-	-	115	°C

Integrated Receiver Specifications

All specifications apply when using the operating conditions defined in Table 12.

Table 13: Receiver Specifications

Parameter		Symbol	Minimum	Typical	Maximum	Units
Downstream						
Input Return Loss (75Ω, Differential)[1]		S_{11}	-	–10	–8	dB
RF Input Frequency Range		f_{RF}	44	-	1002	MHz
Single-Channel Bandwidth		CHBW	-	6 or 8	-	MHz
Maximum Input Power		P_{max}	-	-	–3	dBm
Spectrum Reporting	Span	-	6	-	1002	MHz
	Resolution Bandwidth	-	20.6	329.6	-	kHz
Input Power Reporting Absolute Accuracy[2]		-	–3	-	3	dB
Power Reporting Accuracy per 1dB Step[2]		-	–0.5	-	0.5	dB
IF Output						
IF Output Center Frequency Range		-	5	-	40	MHz
Maximum Voltage Gain (to IF Output)		-	72	-	-	dB
Gain Range (to IF Output)		-	78	-	-	dB
Maximum IF Output Voltage (Differential)		-	-	1	-	Vp-p, diff
Synthesizer						
Integrated Phase Noise (DSB, 30kHz to 4MHz)		-	-	–45	–43	dBc

1 = Using TDK Balun ATB 2012-75011.

2 = Meets the DOCSIS specifications for power reporting with factory calibration.

Digital I/O Specifications

All specifications apply when using the operating conditions defined in Table 12 on page 8, and when configured for the default I/O drive strength setting of = 2x. Refer to the *MxLWare API for Hercules Family Devices User Guide* (document number 005UGR) for I/O drive strength settings.

Table 14: Digital I/O Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Units
3.3V Configuration (VDD_IO = 3.3V)					
Output Logic Voltage on All Digital I/O Pins	V_{OH} @ 3mA source	VDD_IO–0.2	-	-	V
	V_{OL} @ 3mA sink	-	-	0.2	V
Input Logic Voltage on All Digital I/O Pins	V_{IH}	VDD_IO–0.84	-	-	V
	V_{IL}	-	-	0.9	V
1.8V Configuration (VDD_IO = 1.8V)					
Output Logic Voltage on All Digital I/O Pins	V_{OH} @ 3mA source	VDD_IO–0.33	-	-	V
	V_{OL} @ 3mA sink	-	-	0.2	V
Input Logic Voltage on All Digital I/O Pins	V_{IH}	VDD_IO–0.47	-	-	V
	V_{IL}	-	-	0.4	V

Table 15: RESET_N Input Specification

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Logic Voltage on RESET_N Pin	V_{IH}	1.23	-	-	V
	V_{IL}	-	-	0.4	V

MoCA Rejection

The MxL214C requires external filtering (e.g., from a diplexer or triplexer) to meet SCTE40 and other specifications when MoCA is present either inside or outside the box. The designer must provide an external MoCA rejection filter meeting the performance specifications shown in Table 16.

Example: If a –6dBm MoCA signal is present on the cable outside of the consumer's device, 37dB of filter rejection is required.

Table 16: MoCA Signal Rejection Requirement

MoCA Frequency Band	MoCA Signal Level at IC Input	Units
1125MHz–1675MHz	–43	dBm

Current and Power Consumption

Table 17 shows the current and power consumption for the different modes of operation. The VDD_IO is set to 3.3V for the calculation. The values for:

- Typical = Assume nominal supply voltages and room temperature (25°C).
- Maximum = Assume nominal supply voltages, and the temperature range that is specified under the operating conditions in Table 12 on page 8 and process variations.

Table 17: Current and Power Consumption (MxL214C)

Mode of Operation	Supply Voltage	Current (mA)			Power (mW)		
		Minimum	Typical	Maximum	Minimum	Typical	Maximum
Four-Channel Video Plus Four Channel IF	3.3V	-	7	10	-	23	33
	1.8V	-	772	845	-	1390	1521
	1.1V	-	389	514	-	428	566
	Total	**-**	**-**	**-**	**-**	**1841**	**2120**
Power Save Mode*	3.3V	-	5	7	-	17	23
	1.8V	-	180	193	-	324	348
	1.1V	-	122	178	-	134	196
	Total	**-**	**-**	**-**	**-**	**475**	**567**
Sleep Mode (Xtal On)	3.3V	-	0	0	-	0	0
	1.8V	-	17	22	-	31	40
	1.1V	-	4	27	-	4	30
	Total	**-**	**-**	**-**	**-**	**35**	**70**

* = This mode assumes no IF output; one demodulator is connected to the low-power tuner and one TS output.

Crystal Requirements

The MxL214C uses crystals with a fundamental mode frequency of 27MHz. Two fixed 10pF on-chip crystal loading capacitors are integrated into the MxL214C. Two external load capacitors of about 18pF are required to set the frequency to 27MHz.

The following table lists the requirements of the fundamental mode crystal oscillator.

Table 18: Crystal Requirements

Parameter	Minimum	Typical	Maximum	Units
ESR	-	-	30	Ω
Load Capacitance	15	18	18	pF
Frequency Accuracy (Worst Case Temperature, Tolerance, and Aging)	-	-	±30	ppm
Max Drive Level	150	-	-	uW

ESD Performance

All pins meet the ESD levels listed in the following table.

Table 19: ESD Levels

Specification	Description	Condition	Level Passed
JEDEC JS-001-2012	Human Body Model (HBM)	1500Ω, 100pF	2kV
JEDEC JESD22-C101E	Charged Device Model (CDM)	Field Induced Model	500V

Timing Specifications

Supply Voltage Rules

The MxL214C requires the following three supply voltages to operate:

- VDD_IO (3.3V or 1.8V)
- 1.8V
- 1.1V

These pins can be powered up in any order.

Figure 5 provides ramp-up timing requirement applicable to all VDD pins. Figure 6 shows ramp-down timing requirement for all 1.8V analog supplies (i.e.,VDD_1p8_A<1-9>), while there is no ramp-down restriction on other voltage supplies.

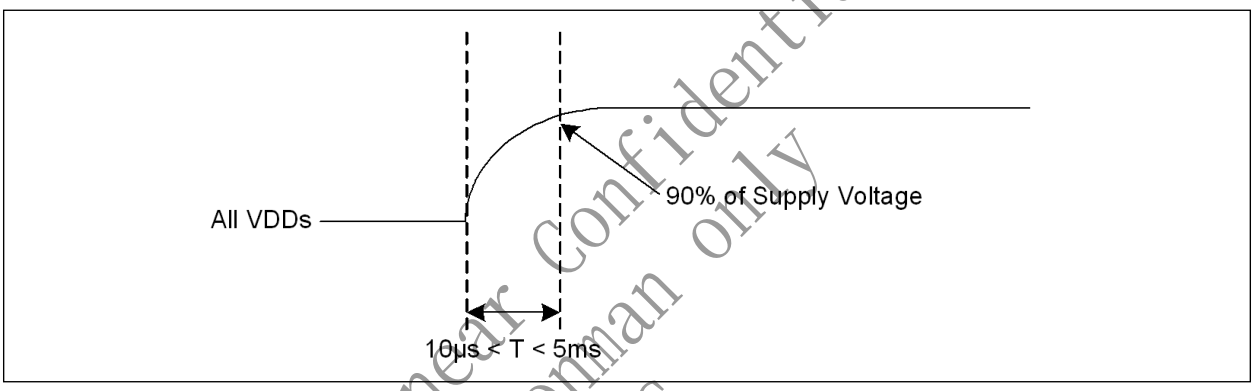


Figure 5: Voltage Supply Ramp-Up Timing

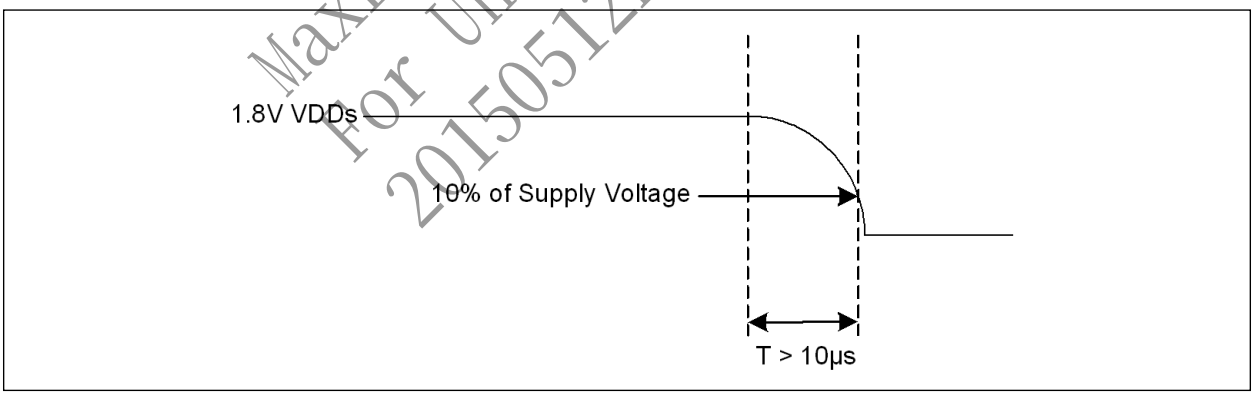


Figure 6: 1.8V Supply Ramp-Down Timing

Serial MPEG TS Timing Specifications

Figure 7 and Figure 8 show the timing diagrams for the MPEG TS output timing specifications. The MPEG_CLK signal can be inverted via configuration of the software, in which case the timing shown in Figure 7 would reference the falling edge of MPEG_CLK.

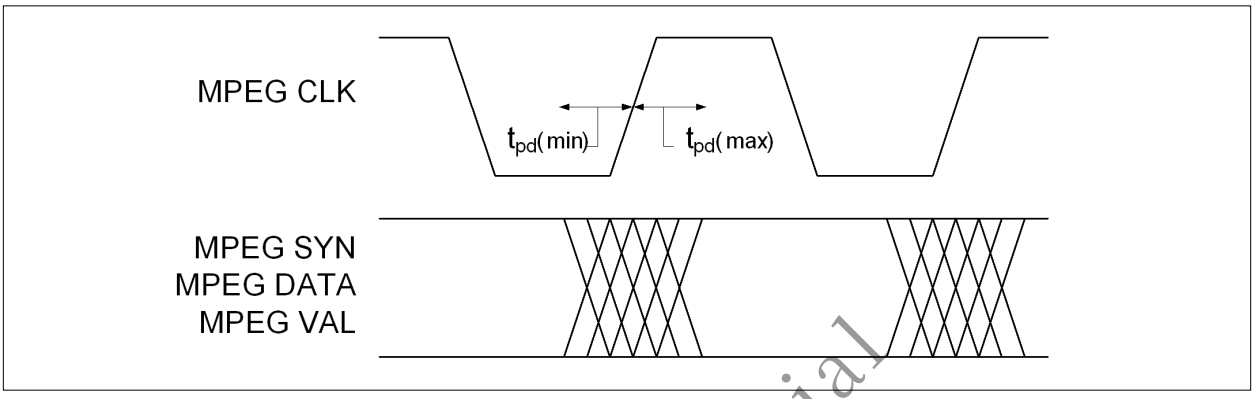


Figure 7: MPEG Serial Output Timing for Four-Wire TS Mode

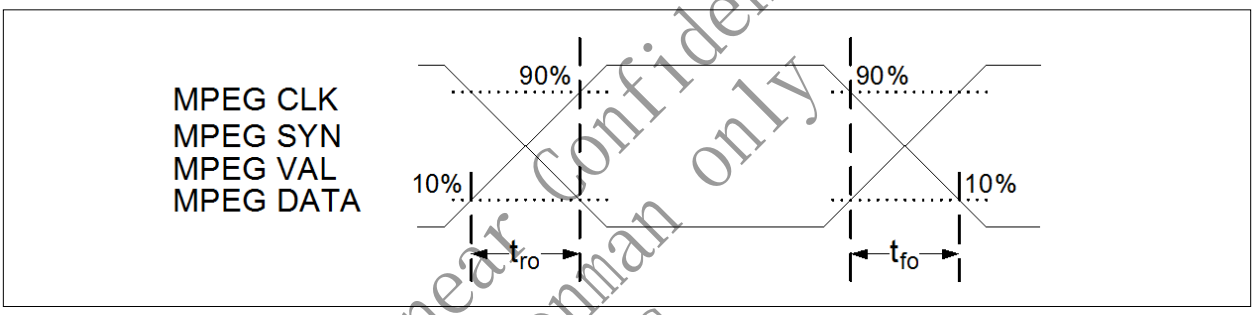


Figure 8: MPEG Output Rise and Fall Time

In the following table, T_A = 25ºC, VDD_IO = 3.3V, unless otherwise specified.

Table 20: Serial MPEG TS Timing Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Units
Propagation Delay[1] (Figure 7) MPEG CLK Frequency ≤ 84.375MHz	t_{pd}	–3	-	3	ns
Propagation Delay[1] (Figure 7) MPEG CLK Frequency = 112.5MHz	t_{pd}	–3	-	2	ns
Rise Time[1, 2] (Figure 8)	t_{ro}	1.1	-	1.6	ns
Fall Time[1, 2] (Figure 8)	t_{fo}	1.1	-	1.5	ns

1 = Measurements with default drive strength.

2 = Capacitive load = 10pF.

I²C Timing Specification

The I²C input and output timing diagrams are shown in Figure 9 and Figure 10, respectively. The corresponding specifications are shown in Table 21.

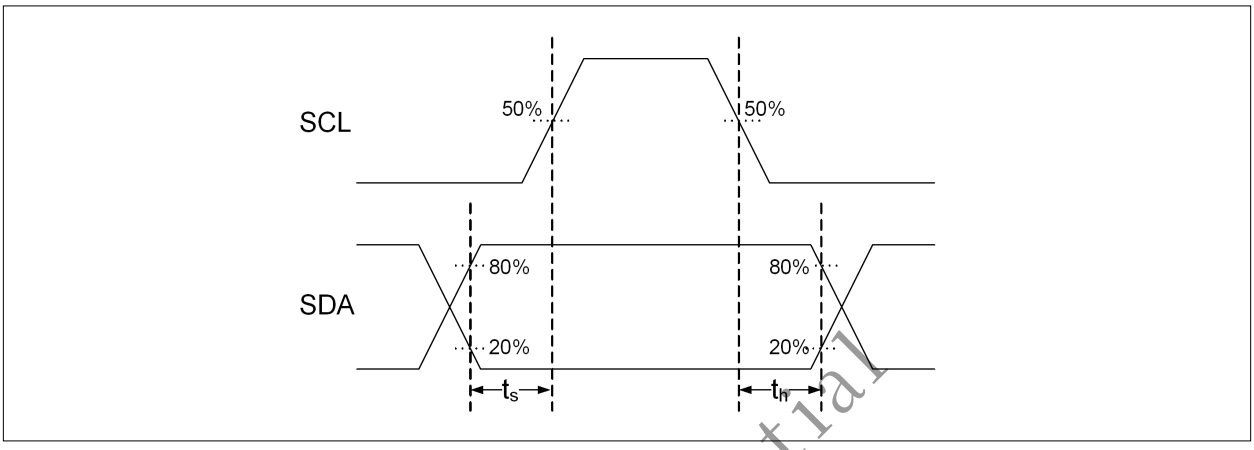


Figure 9: I²C Input Timing

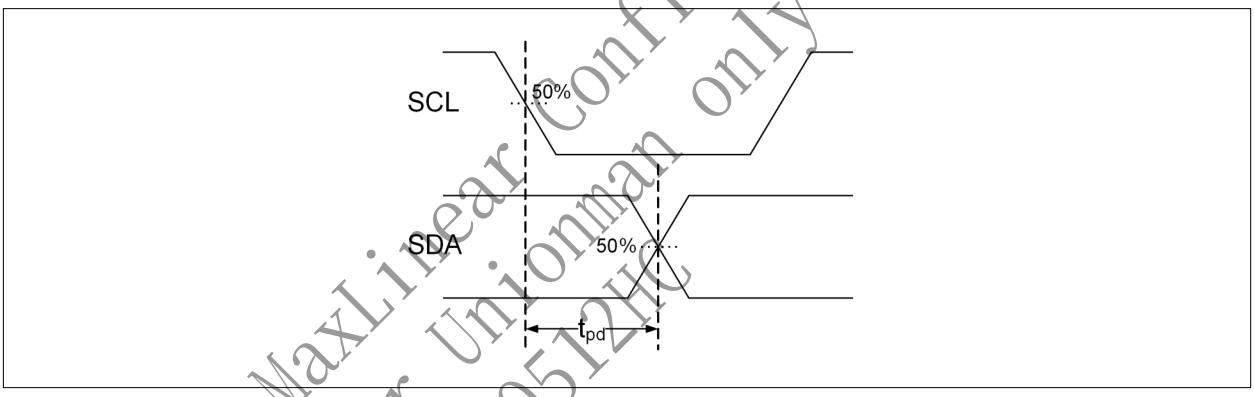


Figure 10: I²C Output Timing

In the following table, T_A = 25°C, VDD_IO = 3.3V, unless otherwise specified.

Table 21: I²C Timing Specification

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup Time (Figure 9)	t_s	-	62	-	ns
Hold Time (Figure 9)	t_h	-	187	-	ns
Propagation Delay (Figure 10)	t_{pd}	-	445	-	ns

Reset Sequence

For the chip to operate normally, the reset sequence and start of I^2C communication must follow the timing specifications shown in Figure 11 and Table 22.

Important! The SCL_0 and SDA_0 I^2C signals *must* be pulled high to VDD_IO during the T_{reset} and T_{ready} times, otherwise the device enters a *test* state.

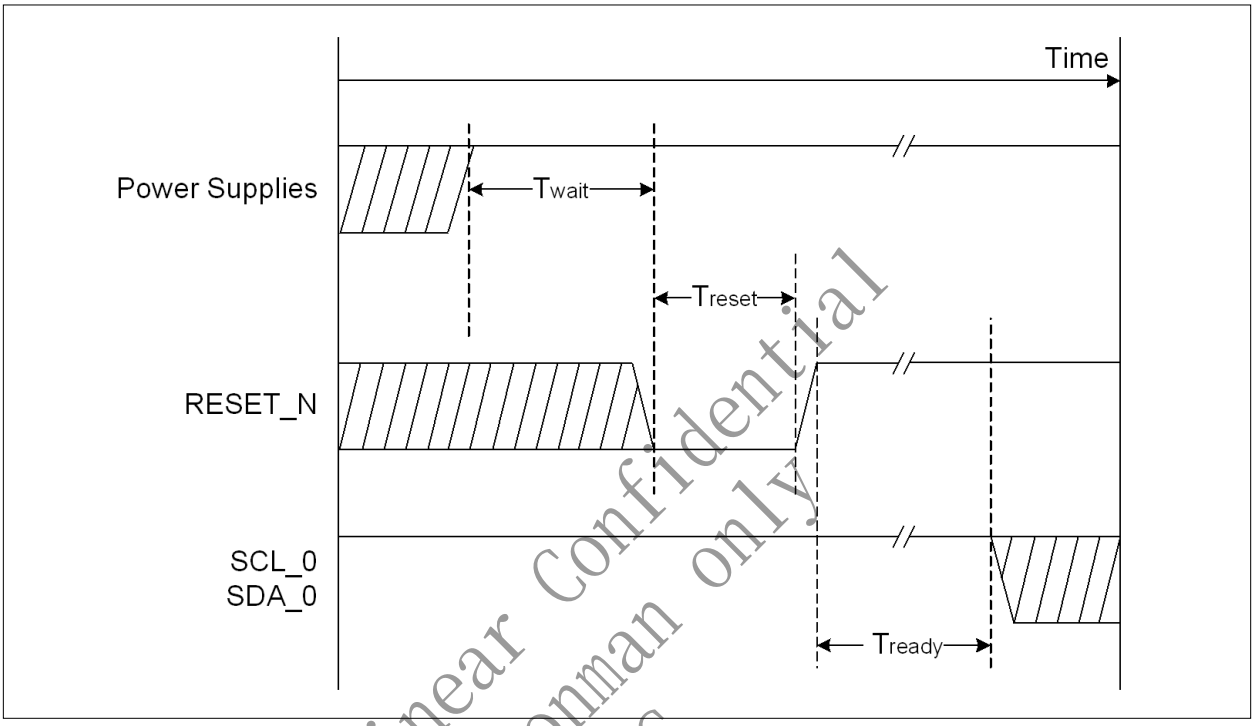


Figure 11: Reset Sequence Timing

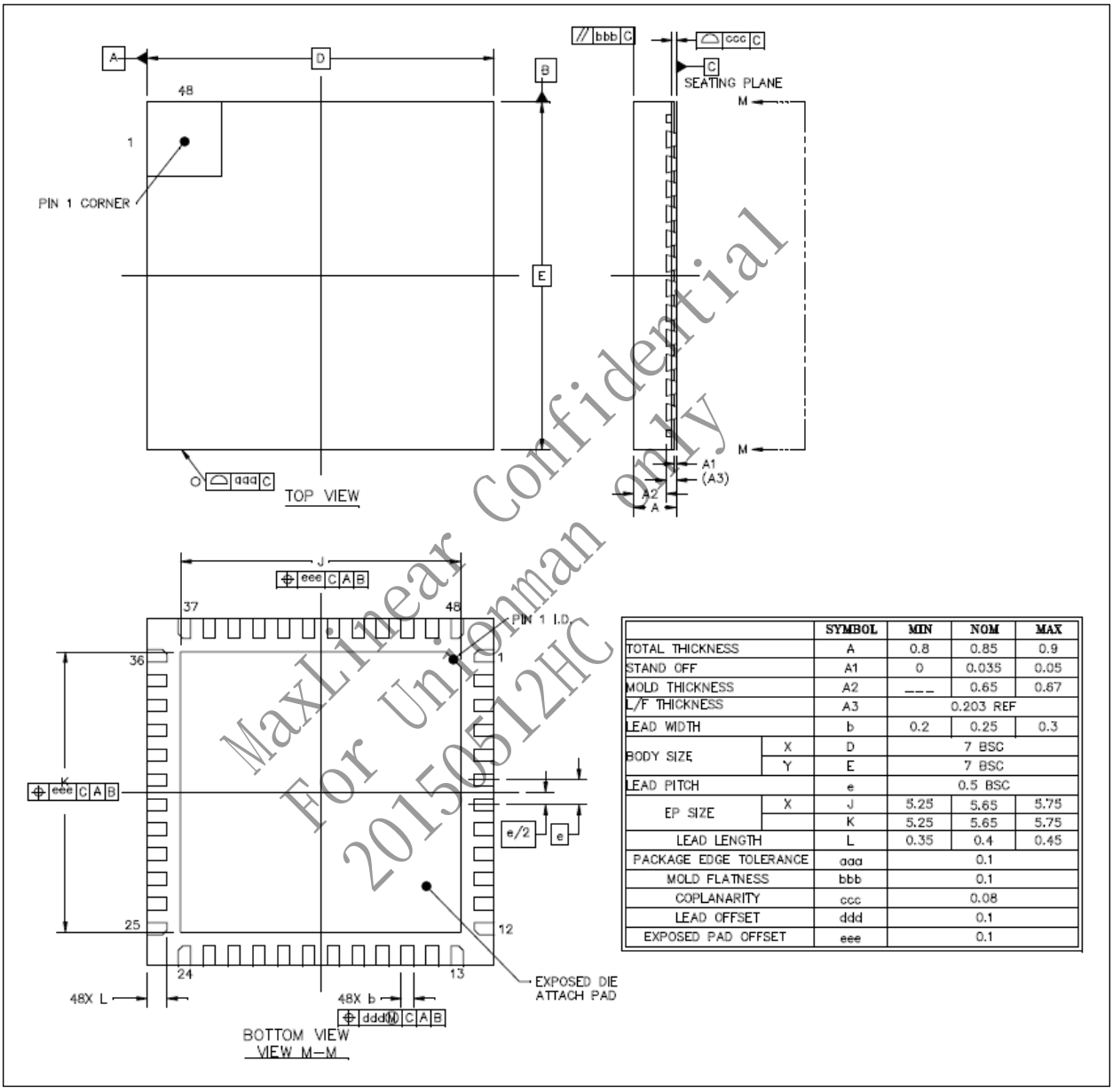
Table 22: Reset Timing Specification

Parameter	Symbol	Minimum	Typical	Maximum	Units
Wait time after all voltage supplies are stable, and before the reset is effective	T_{wait}	75	-	-	ms
Reset Pulse Width	T_{reset}	1	-	-	µs
I^2C Ready Time after Reset De-asserted	T_{ready}	500	-	-	µs

Packaging

Package Dimensions

The QFN48 package dimensions are 7mm x 7mm x 0.85mm.



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.25	5.65	5.75
		K	5.25	5.65	5.75
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 12: Packaging Dimensions

Package Thermal Information

Table 23 provides the thermal resistance value along with the test conditions. Detailed thermal design guidelines are described in *MxL214C Reference Design Guide*.

> ***Note:*** The thermal resistance information stated in Table 23 is based on a standard JEDEC PCB condition, and is for informational purposes only. The actual thermal resistance varies depending on the PCB design.

Table 23: Package Thermal Information

Parameter	Value/Condition	Unit
Thermal Resistance (Junction to Ambient)	20	°C/W
PCB Condition (Thermal Resistance Calculation)	JEDEC JESD 51-5	-
Air Flow Condition	0	mps
Recommended Number of Vias	36	-
Via Pitch	1.0 – 1.2	mm
Via Size (Diameter)	0.25 – 0.33	mm

Ordering Information

Table 24: Ordering Information

Marketing Part Number	Ordering Part Number	Package	Shipping
MxL214C	MxL214-CF-T MxL214-CF-R	SAWN QFN48 7mm x 7mm x 0.85mm	T = Tray R = Tape and Reel

Documentation

The following supplementary guides are available to customers incorporating the MxL214C chip into their designs:

- *MxL214C Reference Design Guide*
- *MxLWare API for Hercules Family Devices User Guide* (document number 005UGR)

Contact your MaxLinear Sales Representative to obtain copies of these documents.

Appendix

I²C Address Select (AS) Configuration using AS Pin 6

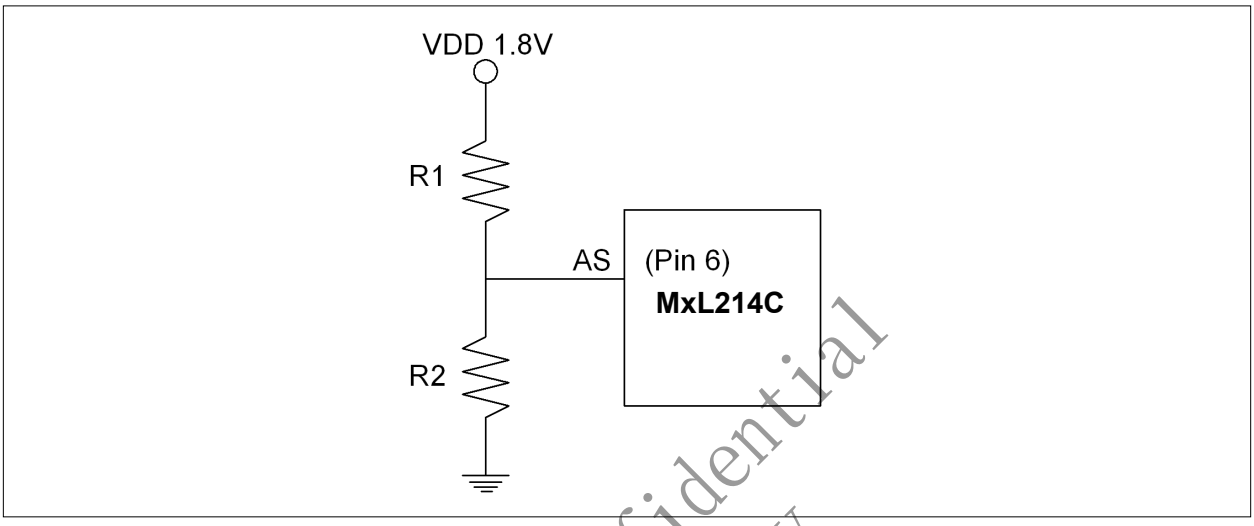


Figure 13: I²C AS Configuration using AS Pin 6

Table 25: I²C Address vs Voltage Applied on AS Pin 6

I²C Address	R1	R2
0x50	Open	30kΩ ± 1%
0x51	62kΩ ± 1%	30kΩ ± 1%
0x52	30kΩ ± 1%	62kΩ ± 1%
0x53	30kΩ ± 1%	Open

Note: Because the AS pin is also used for calibration purposes, the R1 and R2 values must be implemented as specified.

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