MAXLINEAR

MXL301RF SILICON IC TUNER

GENERAL DESCRIPTION

MxL301RF is a highly integrated low-power silicon tuner IC targeting at all global analog (NTSC, PAL, SECAM) and digital cable standards (ITU-T J.83 Annexes A and C [DVB-C] and Annex B [US Cable], DOCSIS, and EURODOCSIS) as well as digital terrestrial reception standards (DVB-T/H, ATSC, ISDB-T 13-Segment, and DTMB). Broadband input filtering and channel filtering have been completely integrated on-chip. This integration enables a very compact design requiring a small footprint, low bill-of-materials cost, and low power consumption.

A signal at the 75 RF input is filtered and converted to a programmable IF output of up to 44MHz. Automatic gain control, LO generation, and channel selectivity functions are completely integrated on the chip, which simplifies board-level design. All functions of the IC can be controlled via I2C interface.

MxL301RF is available in a 5 x 5 mm² 32-pin QFN package.

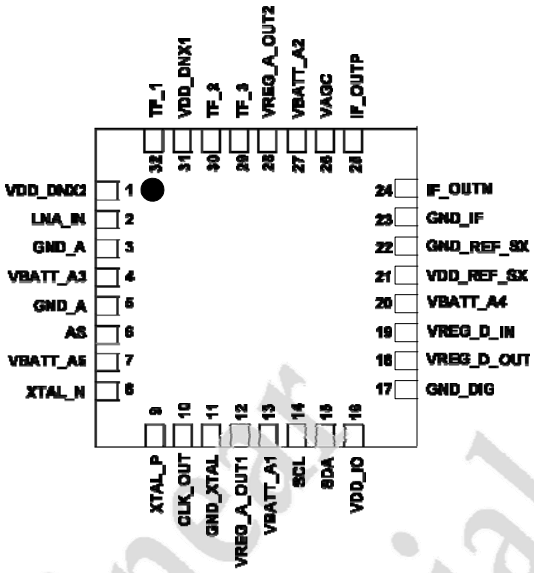
Applications

- Hybrid applications involving both digital and analog receivers for TVs
- Digital cable applications such as STBs, cable modems, EMTAs, and cable DTAs

Features

- Tuning range from 44MHz to 1002MHz
- Integrated channel filtering requiring no external SAW filters for digital applications
- On-chip 90 dB gain
- On-chip 107-dB gain control range with single AGC
  - On-chip broadband power detector
- Low power consumption
  - 170 mA typical (UHF)
- Programmable IF
  - Able to meet all common demodulator interface requirements
- Programmable channel bandwidths of 6, 7, and 8MHz
- Programmable IF spectrum inversion
- Reference clock output available for re-use by demodulators and additional tuners in multi-channel applications
- On-chip voltage regulators enable single supply 3.0V-3.6V operation
  - It can also use an additional 1.7V-2.0V supply for lower power option
- Integrated on-chip programmable loading capacitors for the reference crystal
- I²C-compatible digital control interface

Pin Configuration



IC Block Diagram

The proprietary architecture of the tuner is illustrated in the functional block diagram of Fig. 1. The chip utilizes a proprietary architecture, which achieves the required channel selection using a multi-stage channel filter. The RF input is firstly mixed to a fixed frequency, then after channel filtering it is mixed to a programmable IF frequency. Anti-alias filtering after 2nd mixing stage removes any out-of-band harmonics. A tunable IF LO allows for programmable IF frequencies. Automatic gain control is distributed throughout the signal path for optimum noise and linearity performance through a single AGC. Two on-chip voltage regulators regulate the battery voltage to the internal supply of 1.6V and one on-chip voltage regulator regulates the 1.6V supply to an internal supply of 1.2V.

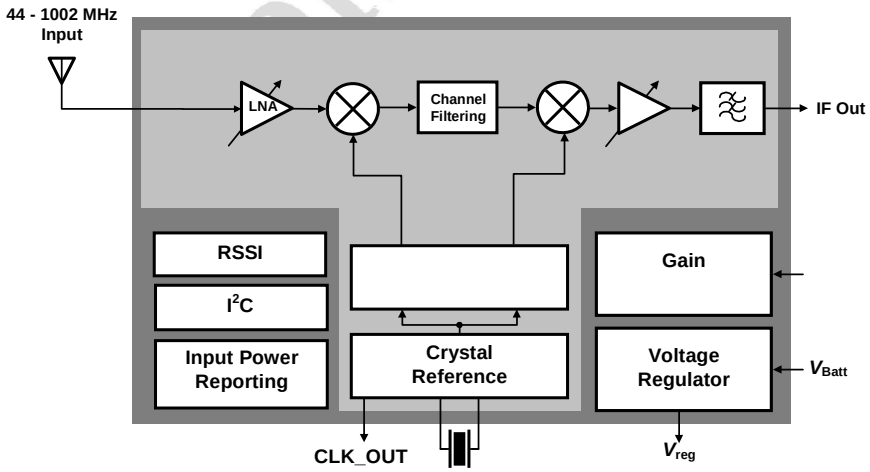


Figure 1. IC Block diagram