# MAXLINEAR

## MXL5003S DIGITAL SILICON IC TUNER

## General Description

The MxL5003S is an integrated tuner IC, which meets the specifications of digital (DVB-T, DVB-H, ISDB-T 13-seg, ATSC, and 64/256-QAM) TV standards. It enables a manufacturer to design a TV tuner module with a small footprint, low bill-of-materials cost, and low power consumption.

The tuner IC can be configured through I²C interface to change modes for receiving different standards. It takes an input from a 75Ω antenna or cable and produces a programmable channel-selected IF output up to 57MHz. Gain control, LO generation, and channel selectivity functions are completely integrated on the chip, which simplifies board-level design. The nominal power supply is 1.8V. If 1.8V supply is not available, an on-chip regulator can provide the 1.8V supply from a 2.3V to 3.6V supply.

The MxL5003S is available in a 6 x 6 mm² 40-pin QFN package. Other package options are available.

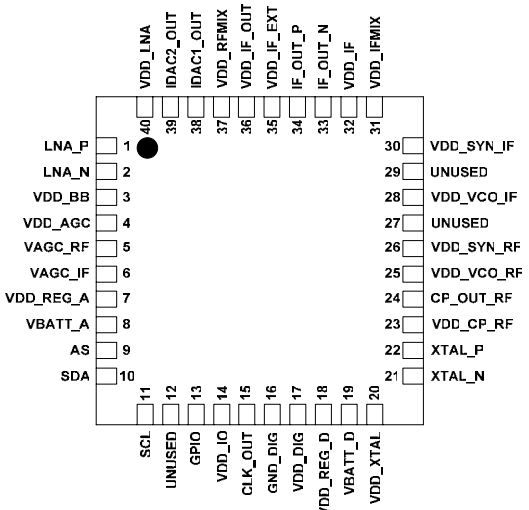
## Applications

- High-performance DVB-T, DVB-H, ISDB-T 13-seg, ATSC, and 64/246-QAM television receivers
- Flat-screen TVs with low power and small form-factor requirements such as LCD monitors
- Portable applications such as laptops, automobiles, portable DVD players
- Handheld applications such as cellular phones and PDAs

## Features

- Implemented in CMOS 0.18µm process
- Tuning range from 44 to 885 MHz
- Integrated channel filtering requiring no external SAW filters
- On-chip 75 dB AGC with single AGC
  - 57 dB RF and 32 dB IF with dual AGC
  - On-chip RSSI with single AGC
- Low power consumption
  - 165 mA typical ( UHF mode)
- Programmable IF from low to high IF
  - Flexible support for different demodulator requirements
- Programmable channel bandwidths from 6, 7, and 8MHz
- Programmable IF spectrum inversion
- Clock output available to drive demodulator to save crystal components
- On-chip regulator voltage input 2.3-3.6V
  - Can be bypassed with 1.8V supply
- I²C-compatible digital interface
- Compatible to additional off-chip LNA to reduce NF, and to increase gain and gain range

## Pin Configuration



# IC Block Diagram

The proprietary architecture of the tuner is illustrated in the functional block diagram of Fig. 1. The chip utilizes a proprietary architecture, which achieves the required channel selection using a multi-stage channel filter. The RF input is first mixed to a fixed frequency, then after channel filtering it is mixed to a programmable IF frequency. Anti-alias filtering after 2nd mixing stage removes any out-of-band harmonics. A tunable IF LO allows for programmable IF frequencies. Automatic gain control is distributed throughout the signal path for optimum noise and linearity performance. In single-AGC mode, VAGC_RF controls both the RF and IF gain. An RSSI block can be enabled to detect the LNA output and automatically adjusts the gain of the LNA. In dual-AGC mode, VAGC_RF and VAGC_IF control the RF and IF gain. An on-chip regulator regulates the battery voltage to the internal supply of 1.8V. An optional off-chip VHF/UHF pre-select filter eliminates strong blockers above the UHF band.

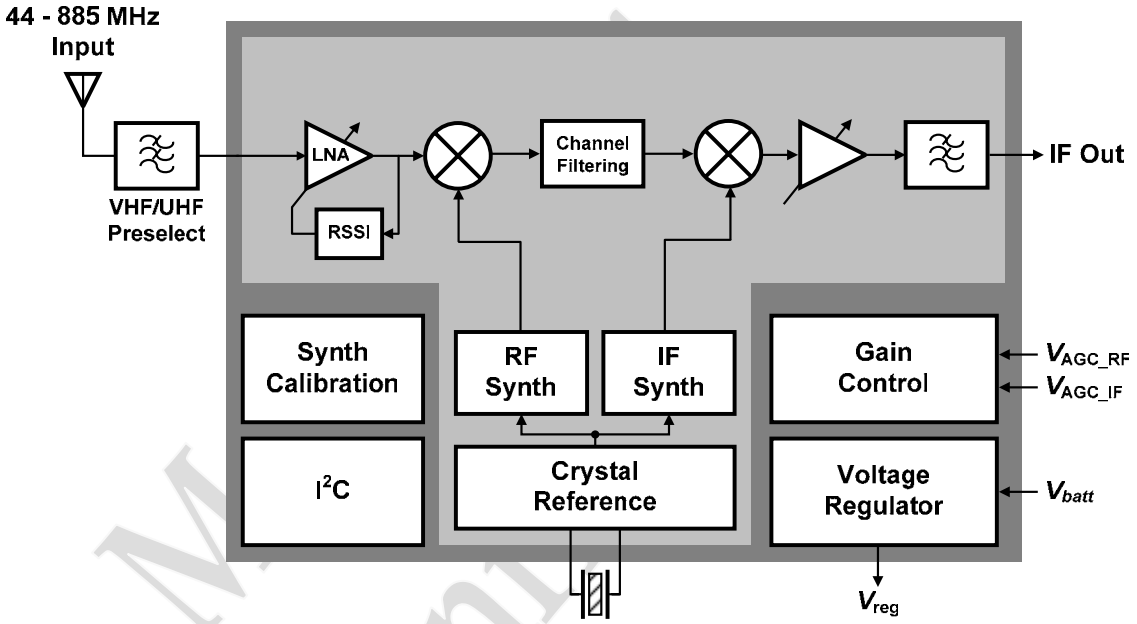



Figure 1. Block diagram

# Pin Description

## Pin Names

| Pin # | Pin Name | | Pin # | Pin Name |
|---|---|---|---|---|
| 1 | LNA_P | | 21 | XTAL_N |
| 2 | LNA_N | | 22 | XTAL_P |
| 3 | VDD_BB | | 23 | VDD_CP_RF |
| 4 | VDD_AGC | | 24 | CP_OUT_RF |
| 5 | VAGC_RF | | 25 | VDD_VCO_RF |
| 6 | VAGC_IF | | 26 | VDD_SYN_RF |
| 7 | VDD_REG_A | | 27 | UNUSED |
| 8 | VBATT_A | | 28 | VDD_VCO_IF |
| 9 | AS | | 29 | UNUSED |
| 10 | SDA | | 30 | VDD_SYN_IF |
| 11 | SCL | | 31 | VDD_IF_MIX |
| 12 | UNUSED | | 32 | VDD_IF |
| 13 | GPIO | | 33 | IF_OUT_N |
| 14 | VDD_IO | | 34 | IF_OUT_P |
| 15 | CLK_OUT | | 35 | VDD_IF_EXT |
| 16 | GND_DIG | | 36 | VDD_IF_OUT |
| 17 | VDD_DIG | | 37 | VDD_RFMIX |
| 18 | VDD_REG_D | | 38 | IDAC1_OUT |
| 19 | VBATT_D | | 39 | IDAC2_OUT |
| 20 | VDD_XTAL | | 40 | VDD_LNA |

## RF Interface

Two pins are provided for RF input. Nominally only one pin is required. An optional pin is provided for a balanced input and improved linearity.

| Pin Name | Direction | Description |
|---|---|---|
| LNA_N | Input | Tuner input with input impedance of 75 Ω |
| LNA_P | Input | Optional input pin for differential drive |

## I²C Interface

This chip provides I²C compatible interface.

| Pin Name | Direction | Description |
|---|---|---|
| SCL | Input | Clock |
| SDA | Bidir | Pull-down data pin |
| AS | Input | Address selection |

## Supply and Ground

This chip contains an on-chip regulator that regulates the battery voltage to nominally 1.8V on-chip operation.

| Pin Name | Direction | Description |
|---|---|---|
| VDD_NAME | Input | Supply voltage for on-chip circuits |
| VDD_IF_EXT | Input | Supply voltage for biasing up IF output. Connects to external supply for IF output. |
| VBATT_A | Input | Supply voltage input for on-chip analog regulator |
| VBATT_D | Input | Supply voltage input for on-chip digital regulator |
| VDD_REG_A | Output | Supply voltage output from analog regulator |
| VDD_REG_D | Output | Supply voltage output from digital regulator |
| VDD_IO | Input | Supply voltage input for I/O interface |
| GND_DIG | Input | Ground for digital circuit blocks |

## Analog and Digital I/O

| Pin Name | Direction | Description |
|---|---|---|
| IF_OUT_P | Output | Open-drain IF output |
| IF_OUT_N | Output | Open-drain IF output |
| VAGC_RF | Input | Automatic gain control for RF section. In single-AGC mode, this pin controls both the RF and IF gain. The partitioning is controlled on-chip. |
| VAGC_IF | Input | Automatic gain control for IF section. In single-AGC mode, this pin is not used. |
| XTAL_P | Input | Crystal positive input. It can be used as an external system clock input pin if no crystal is used |
| XTAL_N | Input | Crystal negative input |
| CP_OUT_RF | Output | RF PLL charge pump output for external loop filter |
| IDAC1_OUT | Output | General purpose DAC current output, controlled by I2C |
| IDAC2_OUT | Output | General purpose DAC current output, controlled by I2C |
| CLK_OUT | Output | Xtal oscillator divide-by-one or by-four clock output for demodulator |
| GPIO | Output | General purpose digital IO, controlled by I2C. This pin can sink or source current at VDD_IO voltage. |

# Specifications

## Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|---|---|---|---|
| VBATT_A | 0 | 3.6 | V |
| VBATT_D | 0 | 3.6 | V |
| VDD_IF_EXT | 0 | 3.6 | V |
| VDD_IO | 0 | 3.6 | V |
| All other VDD_NAME | 0 | 2.0 | V |
| SDA, SCL | 0 | 3.6 | V |
| AS | 0 | 2.0 | V |
| Storage Temp | -65 | 150 | °C |
| Junction Temp | | 150 | °C |
| Soldering Temp | | 260 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device above these, or any other conditions beyond those "recommended" is not implied. Exposure to conditions above those "recommended" for extended periods of time may affect device reliability.

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| Analog/Digital Supply | VDD | 1.7 | 1.8 | 1.9 | V |
| Battery Supply | VBATT | 2.3 | 2.8 | 3.3 | V |
| External VDD Supply for IF Outputs (single-ended 200 Ω pull-up resistors) | VDD_IF_EXT | 2.7 | 2.8 | 3.3 | V |
| AGC Control | VAGC_RF/IF | 0 | | 2.4 | V |
| I/O Supply | VDD_IO | 1.6 | 1.8 | 3.6 | V |
| Address Select | AS | 0 | | 1.9 | |
| Operating Temperature | T | -30 | 25 | 85 | °C |

## Tuner General Specifications

**(Digital Mode, IF = 4.57MHz)**

| Parameter | Symbol | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| System | | | | | |
| Input Return Loss 75 Ω system | $S_{11}$ | 8 | 10 | | dB |
| RF frequency range | $f_{RF}$ | 44 | | 885 | MHz |
| Channel spacing | | 6 | 7 | 8 | MHz |
| Desired Input Signal Range without off-chip LNA (appendix 2) | | -76 | | 0 | dBm |
| Maximum Voltage Gain (appendix 1) | $G_{max}$ | 72 | 80 | 88 | dB |
| Gain Control Range (single AGC, see appendix 3) | AGC | 77 | 80 | | dB |
| RF Gain Control Range (dual AGC) | RFAGC | 53 | 57 | | dB |
| IF Gain Control Range (dual AGC) | IFAGC | 30 | 32 | | dB |
| Noise Figure | NF | | 8.5 | 13.0 | dB |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Input-Referred Spurs (gain=50 dB) | | | | | -1 | 10 | dBµV |
| Output 1dB Compression | | | $OP_{1dB}$ | 120 | 123 | | dBuV |
| 3rd-order Adjacent Channel Intermod Intercept (two-tones in adjacent channel, at gain=50 dB) (see appendix 3) | | | IIP3 | -16.0 | -10 | | dBm |
| 3rd-order In-band Intermod Intercept (gain=50 dB) (appendix 3) | | | | -18.0 | -16.0 | | dBm |
| RF Harmonic Rejection Ratio (D/U = 0 dB) | | 3rd, 5th, 7th | HRR | | -65 | -60 | dBc |
| | | 9th | | | -60 | -50 | dBc |
| IF LO Feedthrough Rejection (appendix 3) | gain =0 – 50 dB | | DCOS | | -60 | -50 | dBc |
| | gain = 50 dB to maxgain | | | | -40 | -30 | dBc |
| I/Q Imbalance (at -1.75 MHz offset) | | | IQI | | -55 | -50 | dBc |
| IF Output (rms, differential) with Single-Ended 200Ω Pull-Up Resistors (desired IF out) | | | | | | 102 | dBµV |
| IF harmonic suppression (LIF and 36.17 MHz only) | | | | 50 | | | dB |
| Channel Select Filter | | | | | | | |
| Baseband Filter Band Edge Frequency Definiton | | BW=6 MHz | FBE | NA | 2.80 | NA | MHz |
| | | BW=7 MHz | | NA | 3.33 | NA | MHz |
| | | BW=8 MHz | | NA | 3.80 | NA | MHz |
| Group Delay Across +/- Band Edge | | BW=6 MHz | GD | | 500 | 600 | ns |
| | | BW=7 MHz | | | 500 | 600 | ns |
| | | BW=8 MHz | | | 500 | 600 | ns |
| Droop Across Band Edge | | BW=6 MHz | DRP | | | 3 | dB |
| | | BW=7 MHz | | | | 3 | dB |
| | | BW=8 MHz | | | | 3 | dB |
| Attenuation of adjacent analog channel (measured at offset from center of band) | BW= 6 MHz | Picture (4.25 MHz) | | 43 | 52 | | dB |
| | | Sound (3.25 MHz) | | 10 | 12 | | dB |
| | BW= 7 MHz | Picture (4.75 MHz) | | 40 | 44 | | dB |
| | | Sound (3.75 MHz) | | 7 | 9 | | dB |
| | BW= 8 MHz | Picture (5.25 MHz) | | 40 | 42 | | dB |
| | | Sound (4.75 MHz) | | 21 | 24 | | dB |
| Synthesizer | | | | | | | |
| Phase Noise | at 1 kHz Offset | | | | -89 | -86 | dBc/Hz |
| | at 10 kHz Offset | | | | -92 | -89 | dBc/Hz |
| | at 100 kHz Offset | | | | -101 | -97 | dBc/Hz |
| PLL Settling Time | | | TS | | 150 | 200 | µs |
| System power-up time | | | TP | | 5 | 7 | ms |

## Current Consumption

The current consumption accounts for temperature and process variations.

| Parameter | | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| Current (IF = 4.57 MHz) | RF=50 - 300 MHz | 170 | 175 | 195 | mA |
| | RF=300 - 900 MHz | 160 | 165 | 185 | mA |

## Crystal Requirements

A fundamental mode crystal in a low-profile SMD package is recommended to reduce component count and form factor. The default crystal frequency used is 16 MHz. This chip is flexible to accommodate other crystal frequencies needed for most demodulators.

| Parameter | Min | Typical | Max | Units |
|---|---|---|---|---|
| Frequency Range | 16 | 48 | 32 | MHz |
| ESR | | 50 | 100 | Ω |
| Static Capacitance | | 7 | | pF |
| Frequency accuracy | | +/- 30 | | ppm |
| Temperature Stability | | +/- 50 | | ppm |

The following crystal frequencies are supported for proper channel tuning with exceptions of in-band spurs in certain crystal frequencies.

| Frequency Supported (MHz) | In-band Spurs Level | | | Units |
|---|---|---|---|---|
| | Min | Typical | Max | |
| 16.0 | | | -61 | dBc |
| 20.48 | | -36 | TBD | dBc |
| 20.5 | | -36 | TBD | dBc |
| 26.057 | | -36 | TBD | dBc |
| 27.0 | | | -61 | dBc |
| 32.513 | | -36 | TBD | dBc |

## IF Frequencies Supported

| | Digital | | | |
|---|---|---|---|---|
| | Low IF (MHz) | Standard IF (MHz) | Bandwidth (MHz) | Comment |
| **ISDBT** | 4.063 | 57.0 | 6 | For 13-segment |
| **DVB-T** | 4.57 | 36.17, 43.75 | 6, 7, 8 | Switchable BW |
| **ATSC/QAM** | 5.38, 6.0, 6.28 | 44.0 | 6 | |

## On-Chip Regulator Specification

| Parameter | Min | Typical | Max | Units |
|---|---|---|---|---|
| Output Voltage | 1.7 | 1.8 | 1.9 | V |

| | | | | | |
|---|---|---|---|---|---|
| Vbatt Input Voltage | | 2.3 | 2.8 | 3.6 | V |
| Maximum Output Current | | | 200 | | mA |
| Minimum Dropout Voltage | | | 0.2 | | V |
| Ripple Rejection (regulator only) | at 1kHz | | 20 | | dBc |
| | at 100 kHz | | 28 | | dBc |
| | at 10 MHz | | 30 | | dBc |
| | at 1 GHz | | 5 | | dBc |

### Sleep Modes

The chip is capable of going into different sleep modes, which are programmable through the I²C interface.

| Mode | Current | Description |
|---|---|---|
| Off | 0 | • Tuner supply is shut off, including I²C interface and memory |
| Deep-Sleep | 50 µA | • On-chip regulator in low-power mode<br>• I²C interface is turned on and memory is maintained |
| | < 3 µA | If on-chip regulator is bypassed:<br>• I²C interface is turned on and memory is maintained |
| Idle | 4 mA | • On-chip regulator and master bias are on<br>• I²C interface is turned on and memory is maintained |
| Tuning | 32 mA | • On-chip PLLs are on and tuned to the desired band<br>• I²C interface is turned on and memory is maintained |

### ESD Performance

All pins pass the ESD performance of 2000V using the Human Body Model (HBM), and of 200V using the Machine Model (MM).

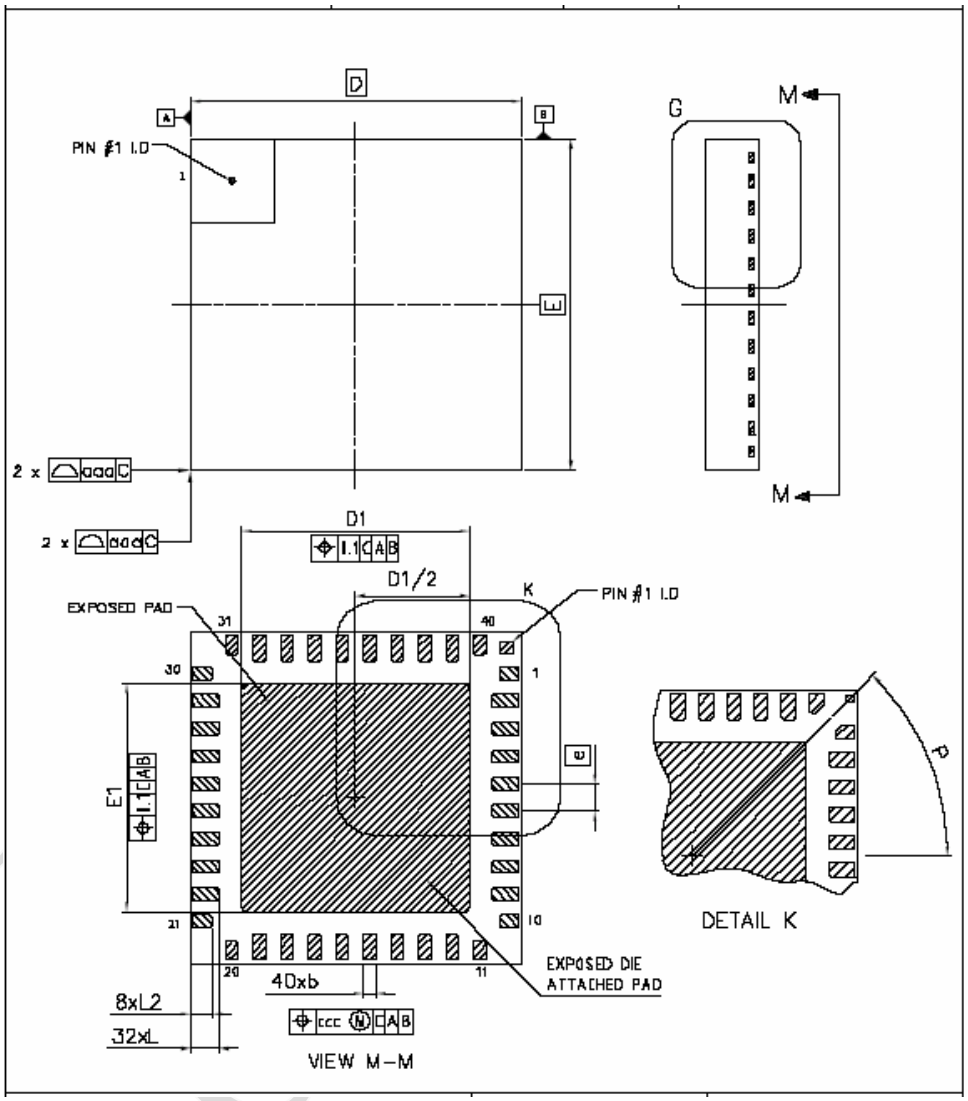


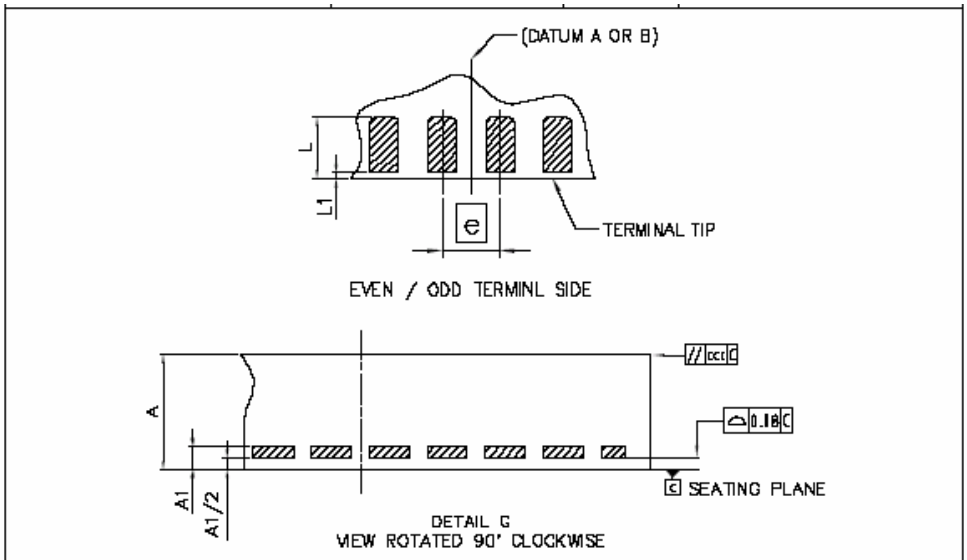
# Ordering Information

| Part Number | Package Type | Description |
|---|---|---|
| MxL5003S | QFN40 | 40-Pin QFN with no leads. Body size 6 x 6 x 0.9mm. Exposed backside paddle. |

# Packaging

QFN40 package dimensions: 6x6x0.9 mm³






| DIM | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.80 | | 1.00 |
| A1 | | 0.203 REF | |
| b | 0.18 | 0.23 | 0.30 |
| D | | 6.00 BSC | |
| E | | 6.00 BSC | |
| D1 | 4.04 | | 4.24 |
| E1 | 4.04 | | 4.24 |
| e | | 0.50 BSC | - |
| L | 0.43 | 0.53 | 0.63 |
| L1 | | | 0.10 |
| L2 | 0.30 | 0.40 | 0.50 |
| P | | 45° BSC | |
| aaa | | 0.10 | |
| ccc | | 0.10 | |

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

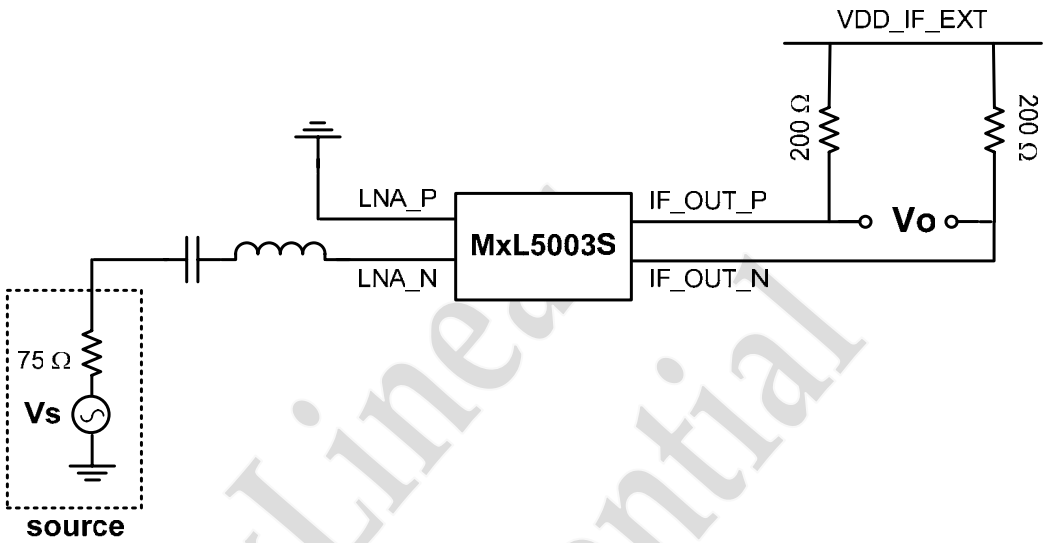
# Application Circuit

Please contact MaxLinear Applications for more information.

# Appendix

## 1. Voltage Gain Definition

$$A_v = \frac{V_o}{\left(\frac{V_s}{2}\right)} = \frac{2V_o}{Vs}$$




## 2. Desired Input Signal Range

The desired input signal range is dependent on modulation system. The data in this datasheet reflects a DVB-T input signal with 64QAM, Rate ¾, 8 MHz bandwidth, and guard interval of ¼. The sensitivity of the input signal range can be improved by 5 to 6 dB with an off-chip LNA.

## 3. Take Over Point

The parameters are specified at a take-over-point (TOP) of 25.2 dB.

# Revision History

**Rev 1.0, July 20, 2006**

1. First release for MxL5003S