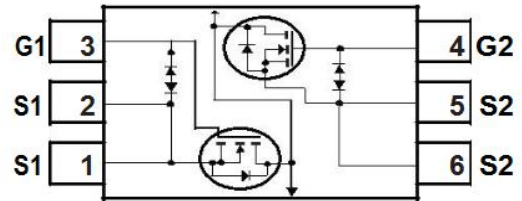




Dual N-Channel Enhancement Mode Power MOSFET

Description

The MXN2386 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected..



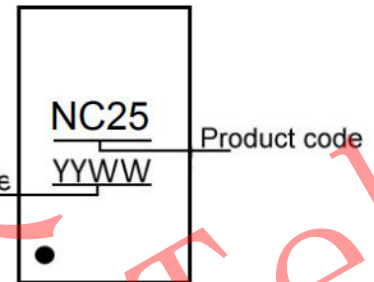
Schematic diagram

General Features

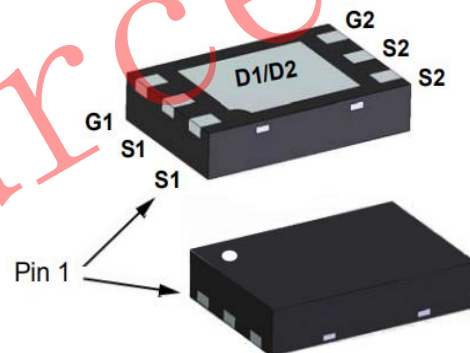
- ◆ $V_{DS} = 20V$, $I_D = 12A$
 @ $V_{GS} = 4.5V$ $R_{DS(ON)}(Typ.) = 6m\Omega$
 @ $V_{GS} = 4.2V$ $R_{DS(ON)}(Typ.) = 6.4m\Omega$
 @ $V_{GS} = 3.8V$ $R_{DS(ON)}(Typ.) = 6.6m\Omega$
 @ $V_{GS} = 2.5V$ $R_{DS(ON)}(Typ.) = 8.3m\Omega$
 ESD Rating: 2000V HBM
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

Application

- ◆ PWM applications
- ◆ Load switch



Marking Description



DFN2x3-6L Pin definition and Top / Bottom View

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	12	A
Drain Current-Pulsed (Note 1)	I_{DM}	70	A
Maximum Power Dissipation	P_D	1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C



Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	22	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$	-	-	± 10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.45	0.8	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=5.5A$	5.1	6.0	7.5	m Ω
		$V_{GS}=4.2V, I_D=5.5A$	5.3	6.4	8.0	m Ω
		$V_{GS}=3.8V, I_D=5.5A$	5.6	6.6	8.6	m Ω
		$V_{GS}=2.5V, I_D=5.0A$	7	8.3	10	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=5A$	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0MHz$	-	1767	-	PF
Output Capacitance	C_{oss}		-	184	-	PF
Reverse Transfer Capacitance	C_{rss}		-	155	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, R_L=1.35\Omega$	-	10.2	-	nS
Turn-on Rise Time	t_r		-	41	-	nS
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS}=5V, R_{GEN}=3\Omega$	-	67	-	nS
Turn-Off Fall Time	t_f		-	31	-	nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=7A,$ $V_{GS}=4.5V$	-	23	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain Charge	Q_{gd}		-	8.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=1A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	7	A

Notes:

- surface mounted on FR4 board, $t \leq 10sec$
- pulse test: pulse width $\leq 300\mu s$, duty $\leq 2\%$
- guaranteed by design, not subject to production testing

Thermal Characteristics

Thermal Resistance junction-to ambient	$R_{th JA}$	126	$^{\circ}C/W$
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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

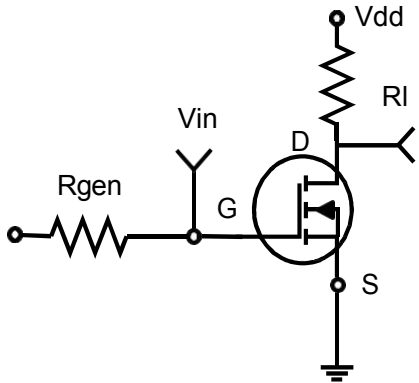


Figure 1: Switching Test Circuit

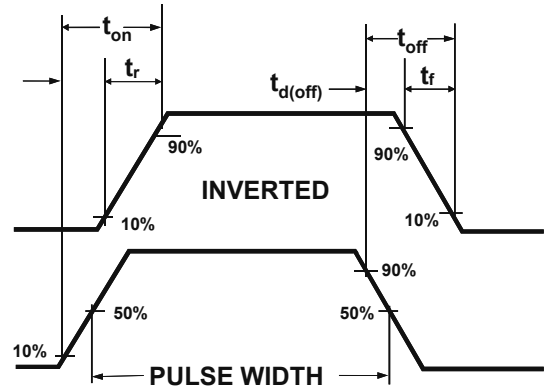


Figure 2: Switching Waveforms

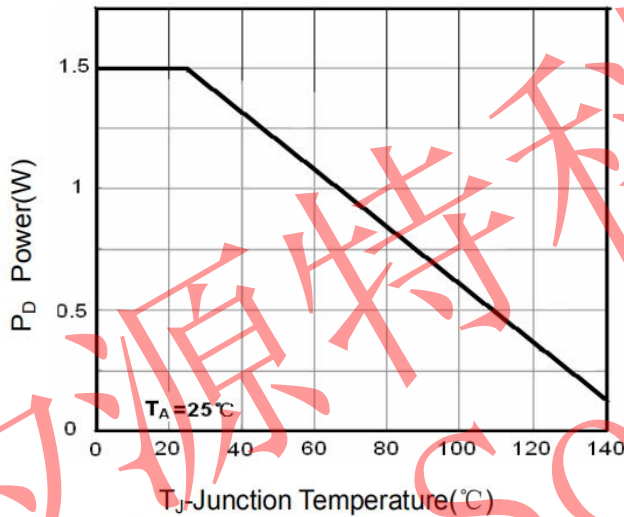


Figure 3 Power Dissipation

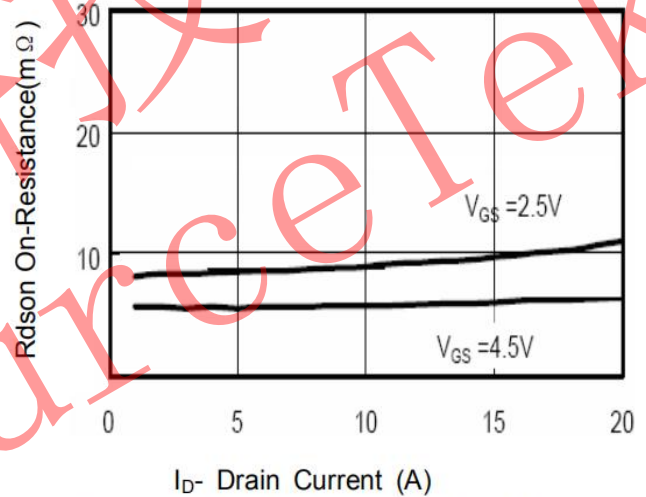


Figure 4 Drain-Source On-Resistance

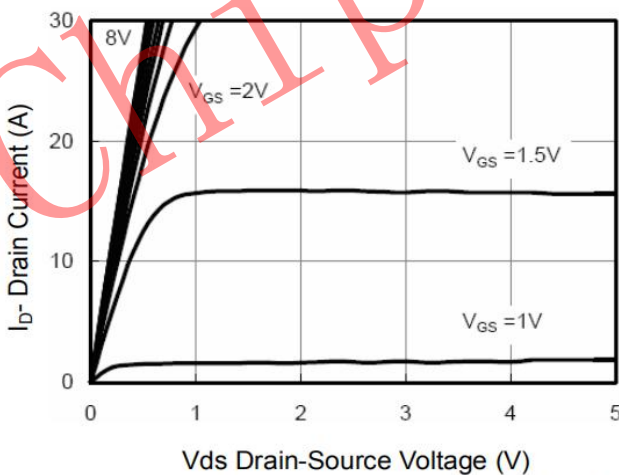


Figure 5 Output CHARACTERISTICS

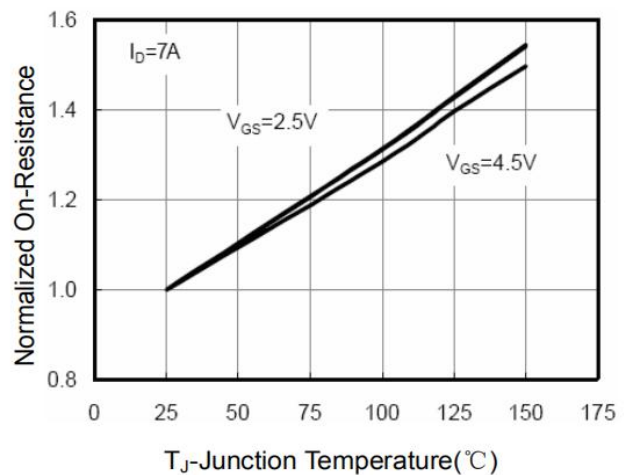


Figure 6 Drain-Source On-Resistance

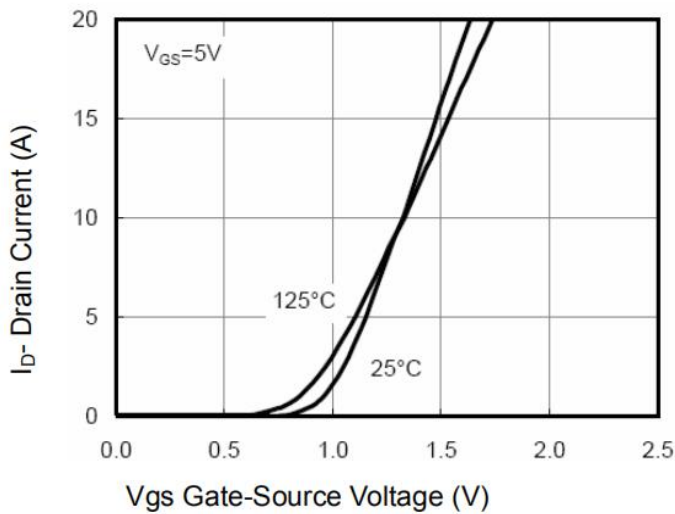


Figure 7 Transfer Characteristics

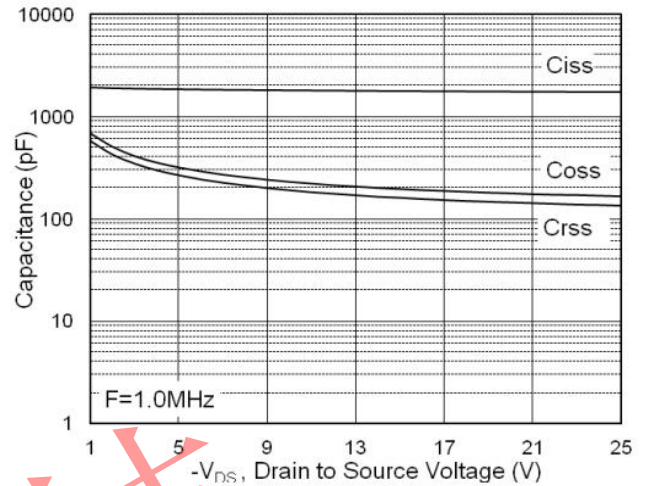


Figure 8 Capacitance vs Vds

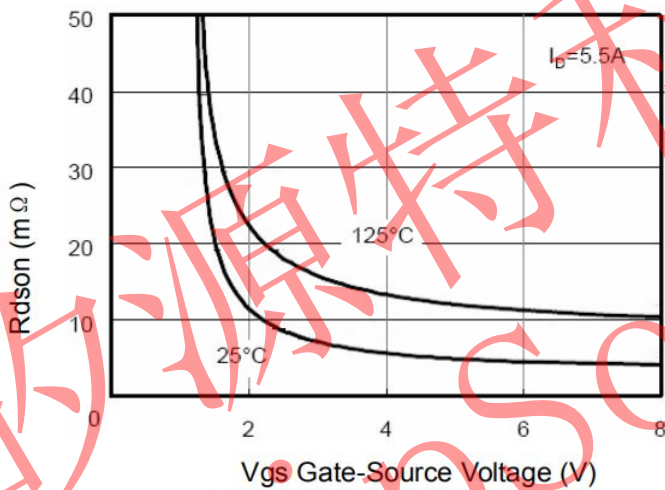


Figure 9 Rdson vs Vgs

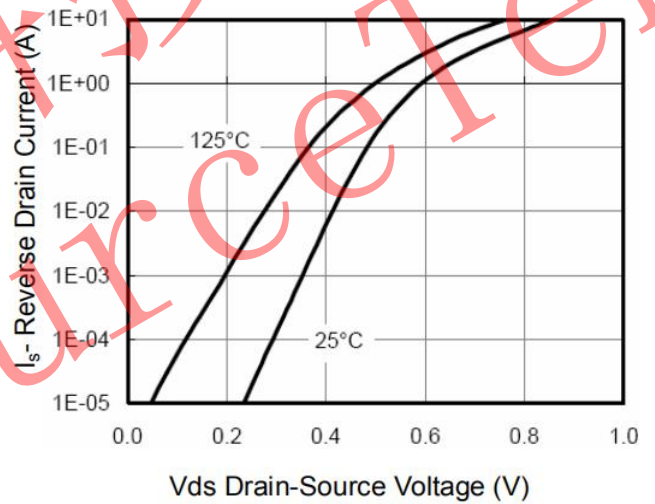


Figure 10 Capacitance vs Vds

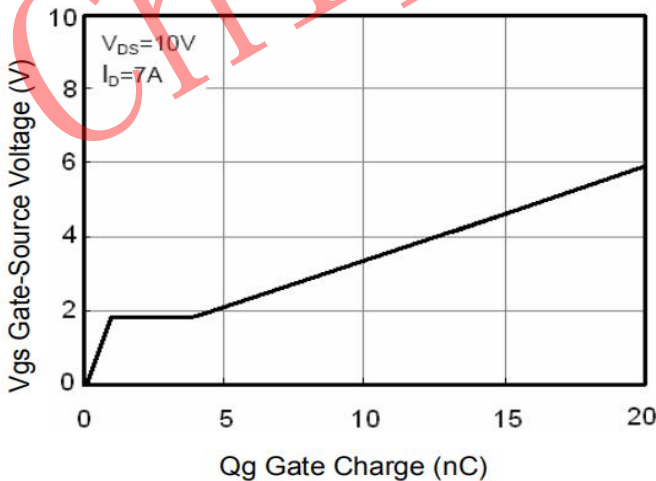


Figure 11 Gate Charge

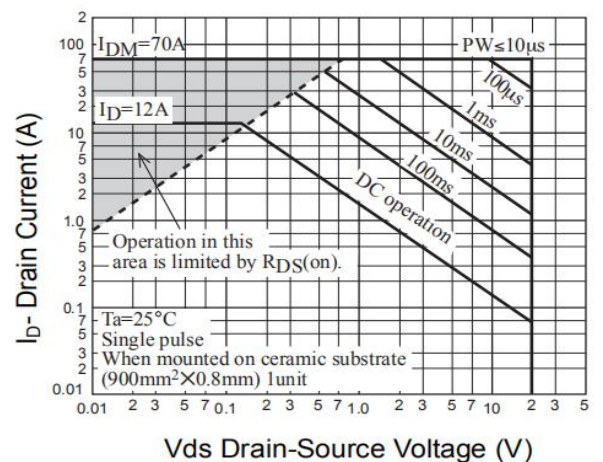
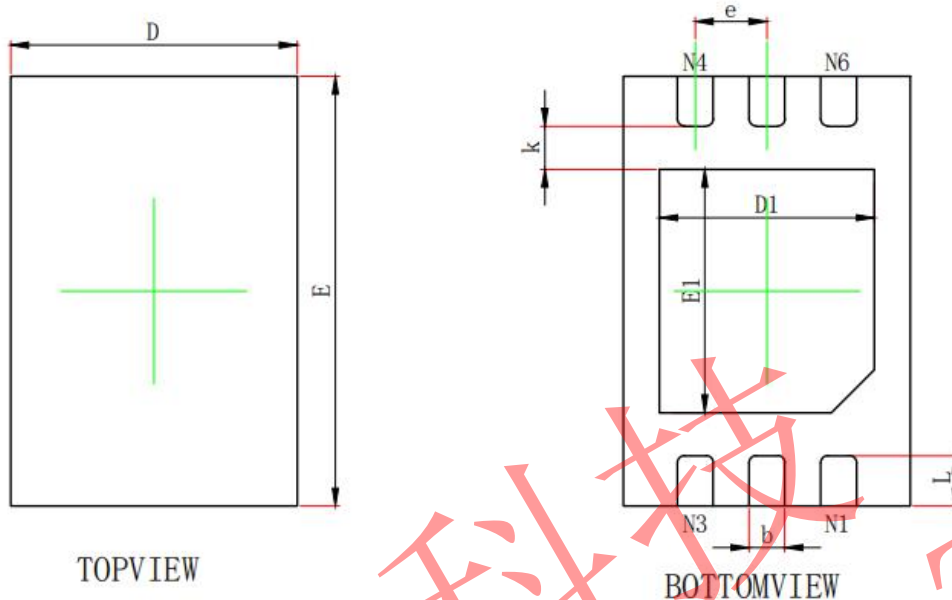


Figure 12 Safe Operation Area



DFNWB2 × 3-6L (P0.50T0.75) PACKAGE OUTLINED DIMENSIONS



矽源特科技
ChipSourceTek

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.950	2.050	0.077	0.081
E	2.950	3.050	0.116	0.120
D1	1.450	1.550	0.057	0.061
E1	1.650	1.750	0.065	0.069
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.400	0.012	0.016