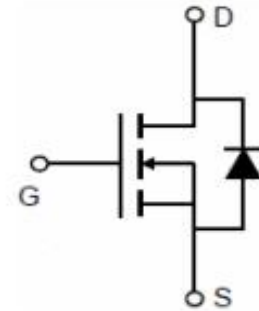




### N-Channel Enhancement Mode Power MOSFET

#### Description

The MXN3050G uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$ , With low gate charge. It can be used in a wide variety of applications.



#### General Features

$V_{DS} = 30V, I_D = 50A$

$R_{DS(ON)} < 9m\Omega @ V_{GS}=10V$

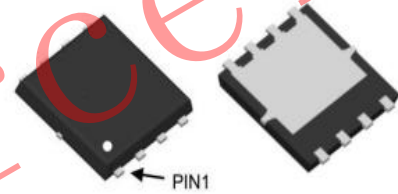
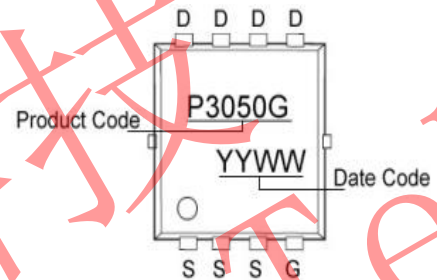
$R_{DS(ON)} < 13m\Omega @ V_{GS}=-4.5V$

Low density cell design

Fully characterized avalanche voltage and current

Good stability and uniformity with high  $E_{AS}$

Excellent package for good heat dissipation



DFN5X6-8L top&bottom view

#### Application

Power switching application

Hard switched and high frequency circuits

Uninterruptible power supply

#### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	50	A
Drain Current-Pulsed (Note 1)	$I_{DM}$	140	A
Maximum Power Dissipation	$P_D$	31	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

#### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	4.0	$^\circ C/W$
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### Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	30	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.4	2.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	7.3	9	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	9.3	13.0	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	-	70	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, F=1.0MHz	-	1200	-	PF
Output Capacitance	C <sub>OSS</sub>		-	190	-	PF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	110	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =15V, R <sub>L</sub> =15Ω V <sub>GS</sub> =10V, R <sub>G</sub> =2.5Ω	-	6.5	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	2	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	18	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	4	-	nS
Total Gate Charge	Q <sub>g</sub>		V <sub>DS</sub> =15V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	10	-
Gate-Source Charge	Q <sub>gs</sub>	-		3	-	nC
Gate-Drain Charge	Q <sub>gd</sub>	-		5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	60	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A di/dt = 100A/μs (Note 3)	-	26	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	34	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

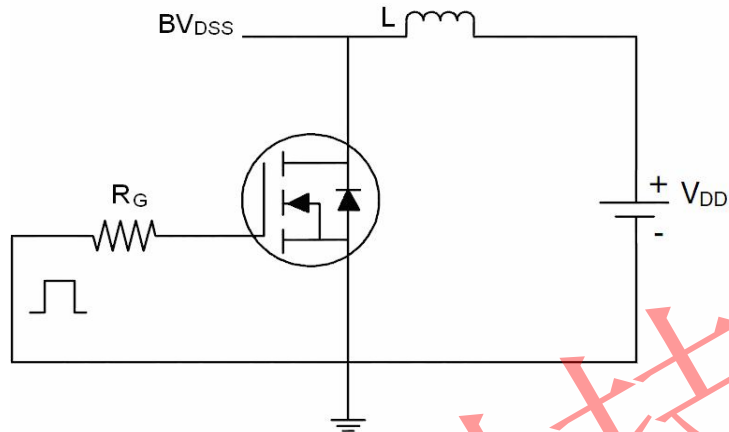
### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

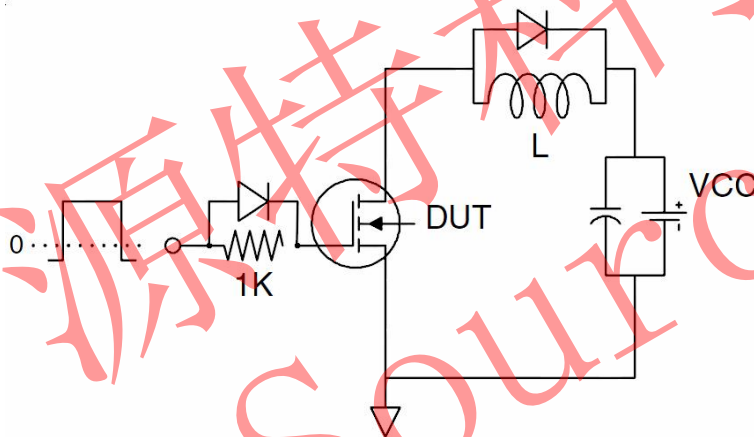


## Test circuit

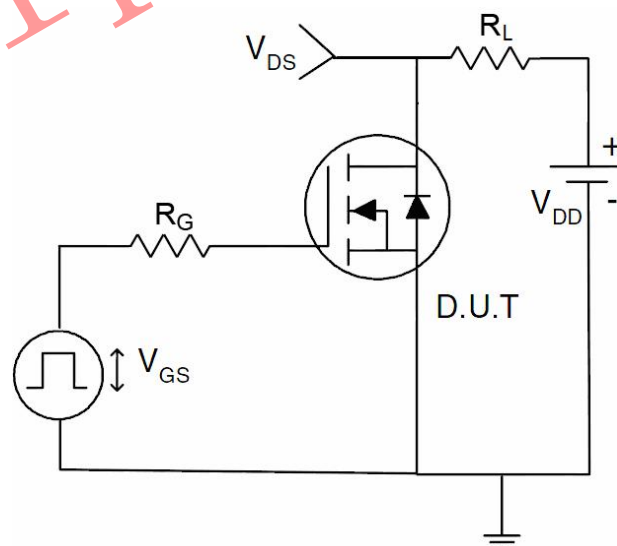
### 1) E<sub>AS</sub> Test Circuit



### 2) Gate Charge Test Circuit



### 3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

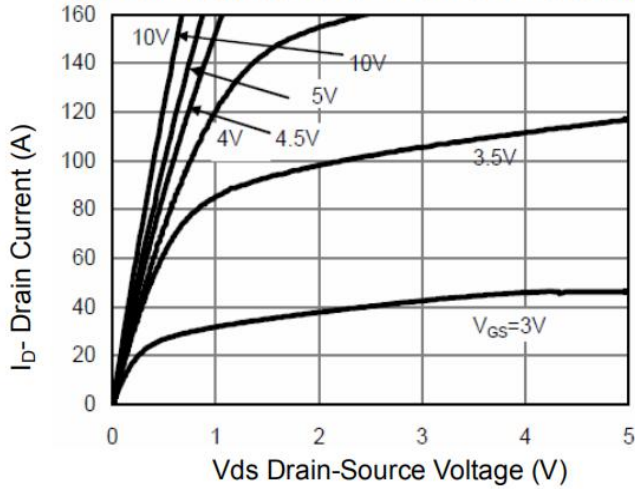


Figure 1 Output Characteristics

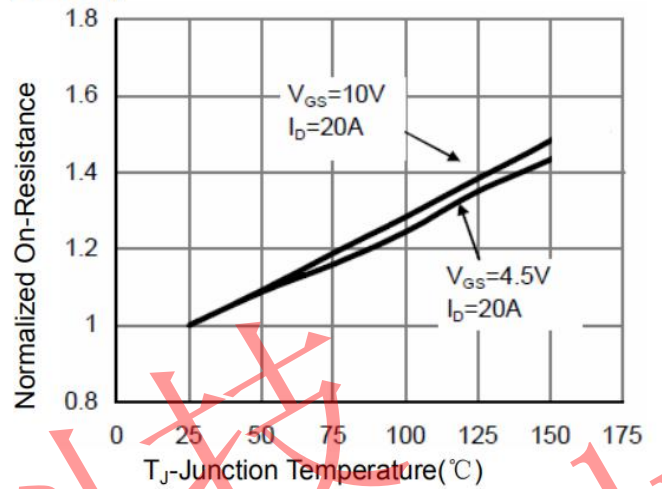


Figure 4  $R_{dson}$ -Junction Temperature

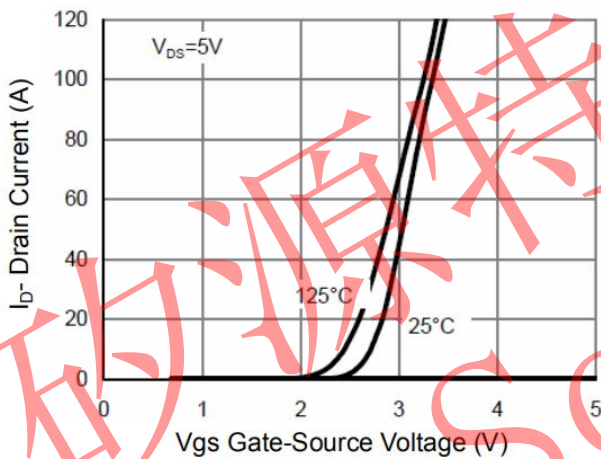


Figure 2 Transfer Characteristics

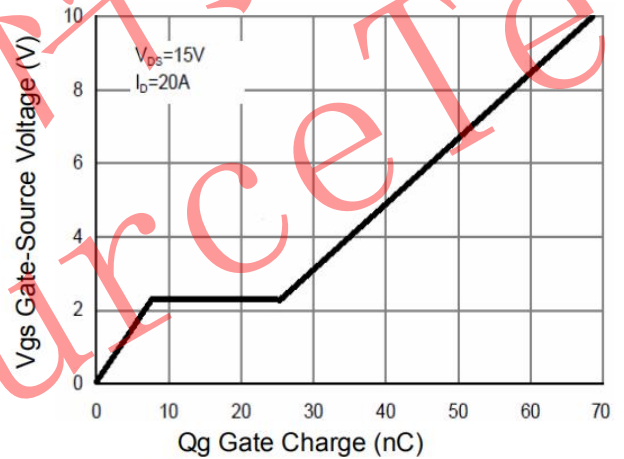


Figure 5 Gate Charge

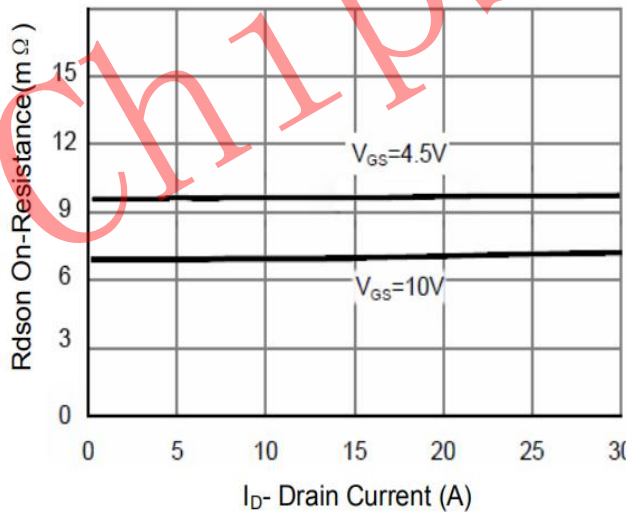


Figure 3  $R_{dson}$ - Drain Current

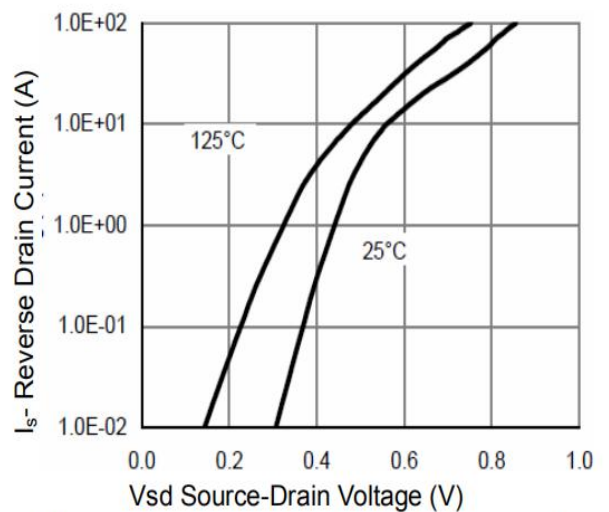


Figure 6 Source- Drain Diode Forward

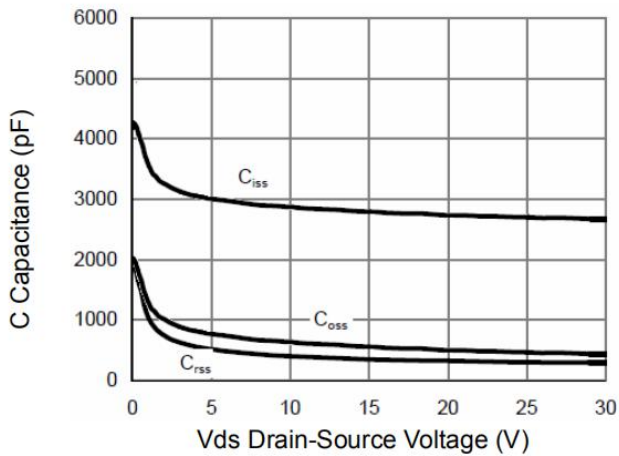


Figure 7 Capacitance vs Vds

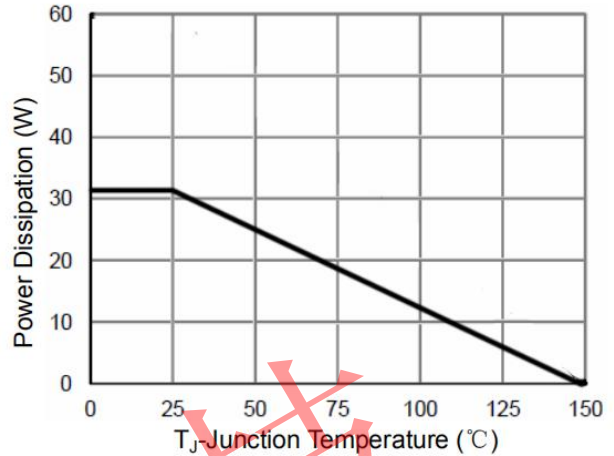


Figure 9 Power De-rating

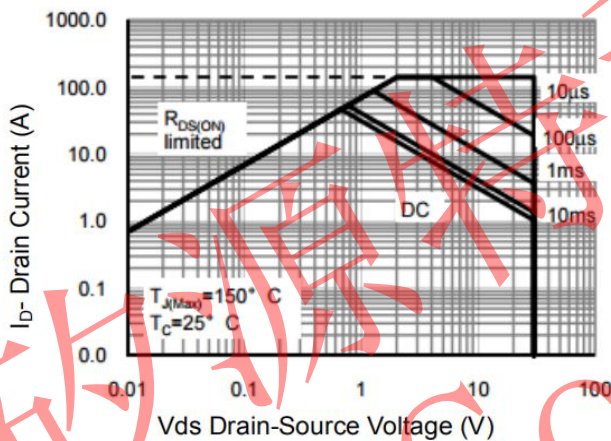


Figure 8 Safe Operation Area

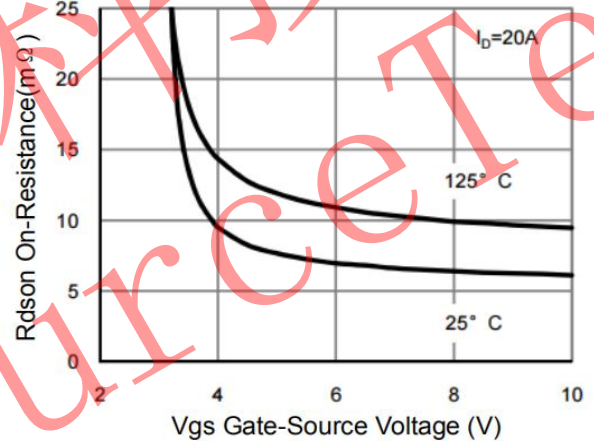


Figure 10 Rds(on) vs Gate-Source Voltage

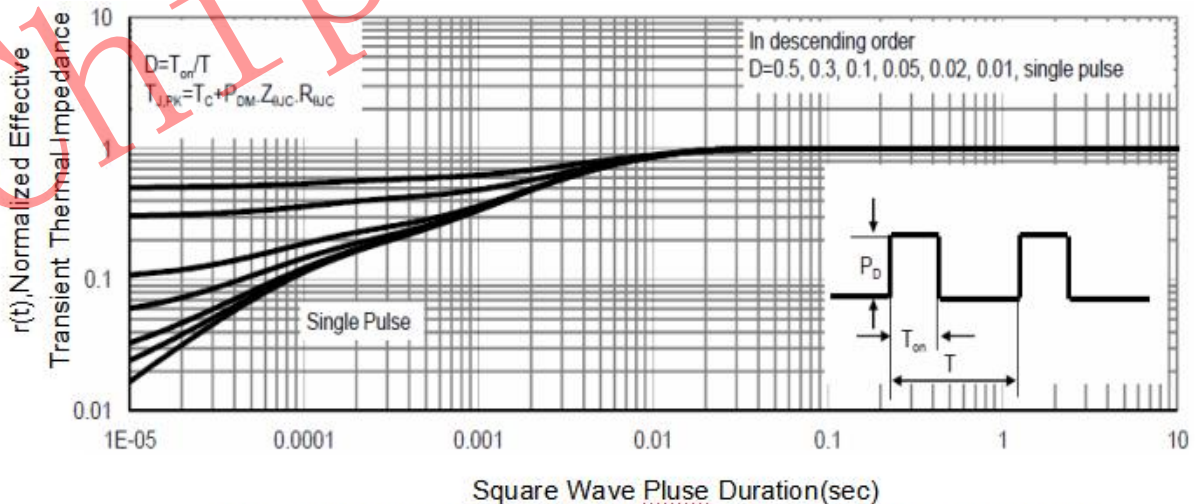
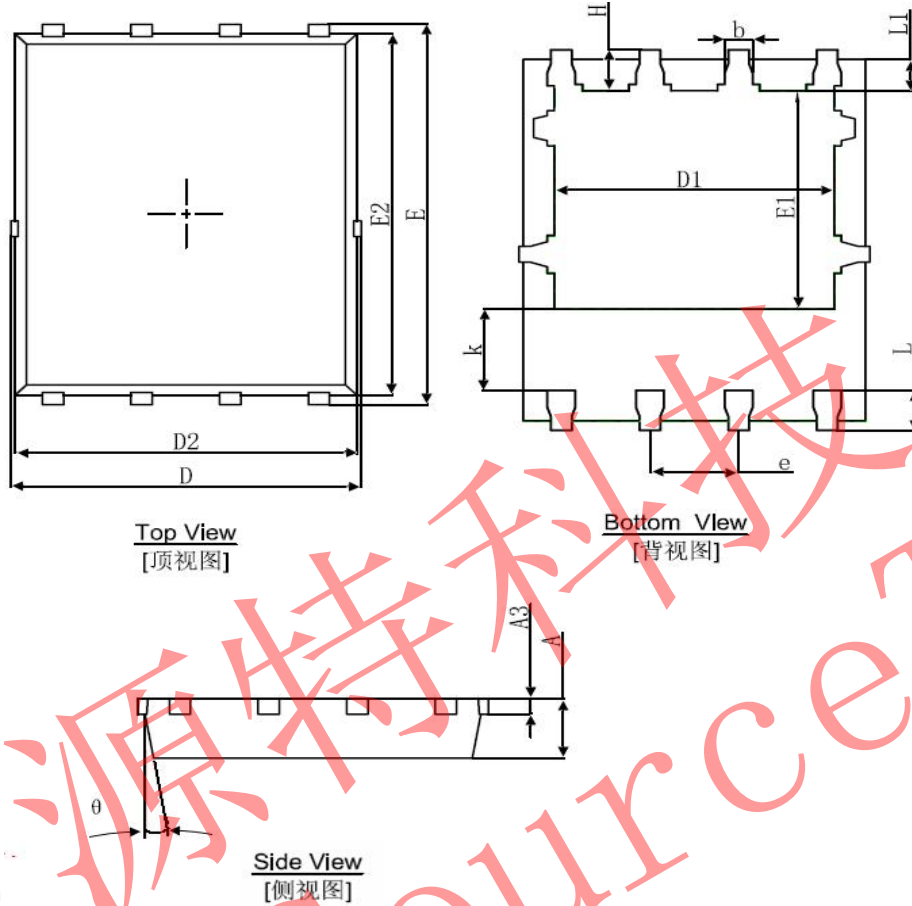


Figure 11 Normalized Maximum Transient Thermal Impedance



DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	8°	12°	8°	12°