MY-Semi

Preliminary

MY9168

16-Channel Constant Current LED Driver With Ghost Image Abatement

General Description

The MY9168 16-channel constant current LED driver with ghost image abatement is suitable for multiplexing display system. The device has wide supply voltage range (3.0V ~ 5.5V) and provides 16 open-drain constant current sinking outputs that are rated to 16V and delivers up to 55mA of high accuracy current to each string of LED. The current at each output is programmable by means of an external current-sensing resistor. The MY9168 features a fast 30MHz DCK input, allowing a wide LED dimming (on/off) range to be implemented. The MY9168 offers a 4-wire serial interface, a 16-bit shift register, and a 16-bit transparent latch. The serial interface allows a microcontroller to configure the output channels using four inputs (DI, DCK, LAT, and ENB) and a data output (DO). DO allows multiple drivers to be cascaded and operated together.

The MY9168's on-board pass elements minimize the need for external components, while at the same time, providing ±1%(typ.) LED current accuracy. Additional features include a ±0.1% regulated output current capability and 30ns fast output transient response.

The MY9168 is available in a 24-pin SOP/SSOP/QFN package and specified over the -40°C to +85°C ambient temperature range.

Features

- 3.0V ~ 5.5V Operating supply voltage
- 3~55mA/5V Constant current output range
- 3~35mA/3.3V Constant current output range
- 16V Rated output channels for long LED strings
- ±1% (typ.) Current accuracy between channels
- ±1% (typ.) Current accuracy between chips
- ±0.1% Output current regulation capability
- 30MHz Clock frequency for data transfer
- Current setting by one external resister
- Schmitt trigger input
- Power on reset
- Stagger output delay
- Fast current transient response
- Ghost image abatement
- Low knee voltage for constant current
- High level HBM ESD protection (Iout pin > 8000V)
- -40°C to +85°C Ambient temperature range

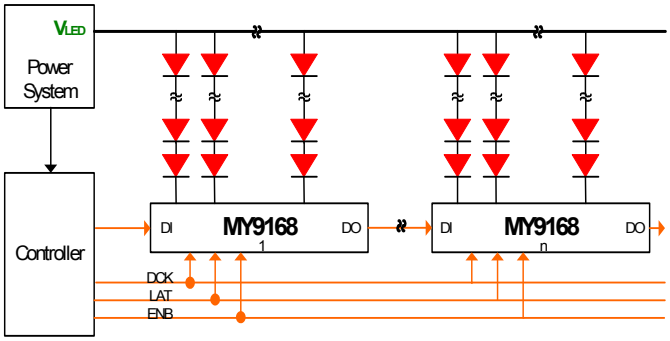
Applications

- Indoor and Outdoor LED Video Displays
- Variable Message Sign (VMS)
- Dot Matrix Module
- Architectural and Decorative Lighting
- Industrial Lighting
- LCD Display Backlighting

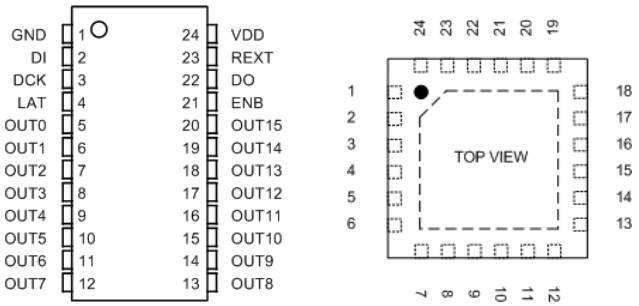
Order information

Part	Package Information	
MY9168SA	SOP24-236mil-1.0mm	2000 pcs/Reel
MY9168SS	SSOP24-150mil-0.635mm	2500 pcs/Reel
MY9168QT	QFN24-4mmx4mm-0.5mm	3000 pcs/Reel
MY9168QE	QFN24-4mmx4mm-0.5mm	3000 pcs/Reel

Typical Operating Circuits

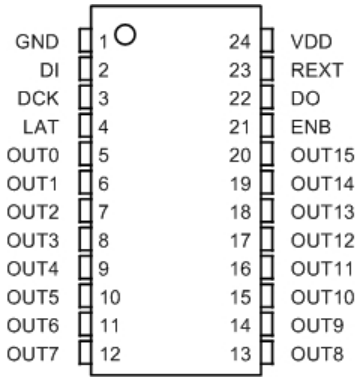


Pin Configuration

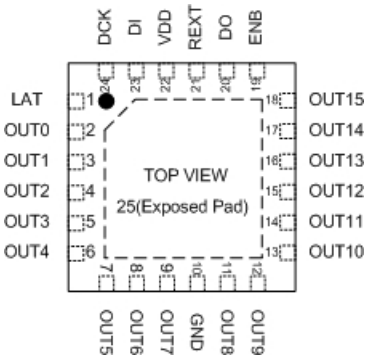


For pricing, delivery, and ordering information, pleases contact MY-Semi Inc. at +886-3-560-1668, or email to INFO@MY-Semi.com.tw or visit MY-Semi's website at www.MY-Semi.com.tw

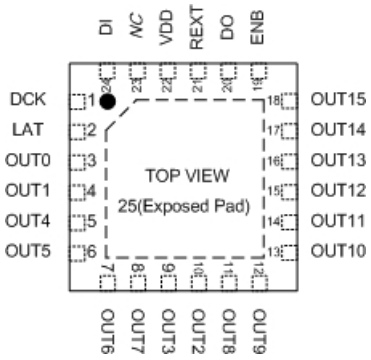
Pin Description



MY9168 SA/SS



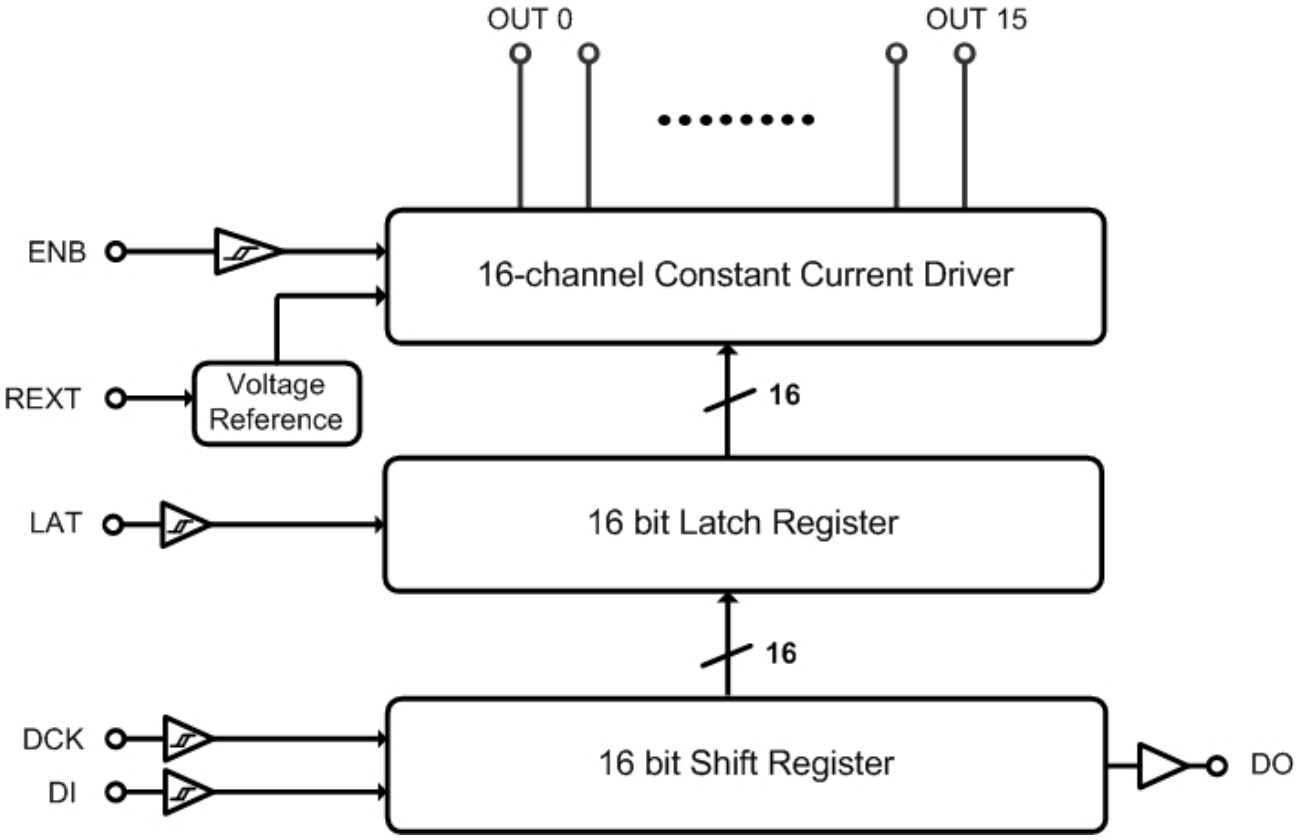
MY9168 QT



MY9168 QE

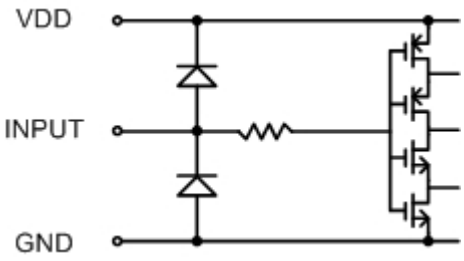
PIN No.			PIN NAME	FUNCTION
SA/SS	QT	QE		
1	10, 25	25	GND	Ground terminal.
2	23	24	DI	Serial data input terminal.
3	24	1	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
4	1	2	LAT	Input terminal of data strobe. Data on shift register is sampled at the rising edge of LAT.
5~20	2~9, 11~18	3, 4, 10, 9, 5~8, 11~18	OUT0~15	Sink constant-current outputs (open-drain).
21	19	19	ENB	Output enable terminal: '**H**' for all outputs are turned off , '**L**' for all outputs are active.
22	20	20	DO	Serial data output terminal.
23	21	21	REXT	External resistors connected between REXT and GND for output current value setting.
24	22	22	VDD	Supply voltage terminal.
—	—	23	NC	No connection.

Block Diagram

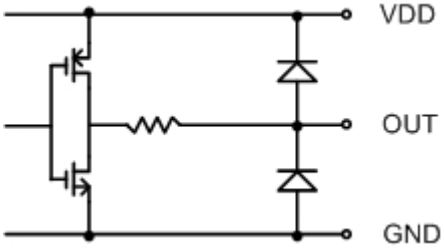


Equivalent Circuit of Inputs and Output

1. DCK, DI, LAT, ENB terminals



2. DO terminal



Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	55	mA
Output Voltage	VOUT	-0.3 ~ 16	V
Input Clock Frequency	FDCK	30	MHz
GND Terminal Current	IGND	900	mA
Thermal Resistance (On PCB)	Rth(j-a)	53.2 (SA:SOP-236mil-1.0mm)	°C/W
		70.5 (SS:SSOP-150mil-0.635mm)	
		36.9 (QT/QE:QFN24-4mmx4mm)	
Operating Supply Voltage	VDD	3.0 ~ 5.5	V
Operating Ambient Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.

(2) All voltage values are with respect to ground terminal.

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 16 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 960 Ω	—	±1.0	±3.0	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±1.0	±3.0	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 6.4 KΩ	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4		—	±1.5	±3.0	%
Output Voltage Regulation*3	% / VOUT	Rrext = 960 Ω VOUT = 1 V ~ 3 V	—	±.0.1	—	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 960 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current *5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	1.3	1.8	mA
	$I_{DD2(off)}$	input signal is static Rrext = 6.4 KΩ all outputs turn off	—	2.3	3.0	
	$I_{DD3(on)}$	input signal is static Rrext = 6.4 KΩ all outputs turn on	—	2.6	3.4	
	$I_{DD4(off)}$	input signal is static Rrext = 960 Ω all outputs turn off	—	4.7	6.1	
	$I_{DD5(on)}$	input signal is static Rrext = 960 Ω all outputs turn on	—	4.8	6.3	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right) \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

*5 IO excluded.

Electrical Characteristics (VDD = 3.3 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 16 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 960 Ω	—	±1.0	±3.0	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±1.0	±3.0	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 6.4 KΩ	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4			±1.5	±3.0	%
Output Voltage Regulation*3	% / VOUT	Rrext = 960 Ω VOUT = 1 V ~ 3 V	—	±0.1	—	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 960 Ω VDD = 3 V ~ 5.5 V	—	±0.7	±1	
Supply Current *5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	0.7	1.0	mA
	$I_{DD2(off)}$	input signal is static Rrext = 6.4 KΩ all outputs turn off	—	2.0	2.6	
	$I_{DD3(on)}$	input signal is static Rrext = 6.4 KΩ all outputs turn on	—	2.3	3.0	
	$I_{DD4(off)}$	input signal is static Rrext = 960 Ω all outputs turn off	—	4.1	5.4	
	$I_{DD5(on)}$	input signal is static Rrext = 960 Ω all outputs turn on	—	4.2	5.5	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

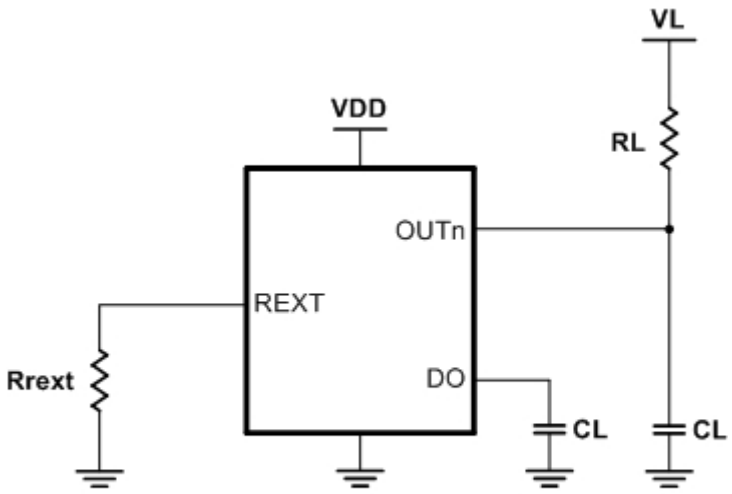
*5 IO excluded.

Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L to ‘H’)	ENB-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 960 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	26.9	—	ns
	LAT-to-OUT0	tpLH2		—	25.1	—	
	DCK-DO	tpLH3		—	22.8	—	
Propagation Delay (‘H’ to ‘L’)	ENB-to-OUT0	tpHL1		—	24.7	—	
	LAT-to-OUT0	tpHL2		—	21.8	—	
	DCK-DO	tpHL3		—	26.3	—	
Pulse Duration	ENB	$tw_{(ENB)}$		20	—	—	
	LAT	$tw_{(LAT)}$		20	—	—	
	DCK	$tw_{(DCK)}$		15	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		5	—	—	
	DI	$tsu_{(D)}$		3	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(D)}$		4	—	—	
DO Rise Time		$tr_{(DO)}$		—	14.2	—	
DO Fall Time		$tf_{(DO)}$		—	15.1	—	
Output Current Rise Time		tor		—	10.0	—	
Output Current Fall Time		tof		—	20.0	—	
Output Delay Time ($OUT_{(2n)}$-to-$OUT_{(2n+1)}$)		tod		—	0.5	—	

Switching Characteristics (VDD = 3.3V, Ta = 25°C unless otherwise noted)

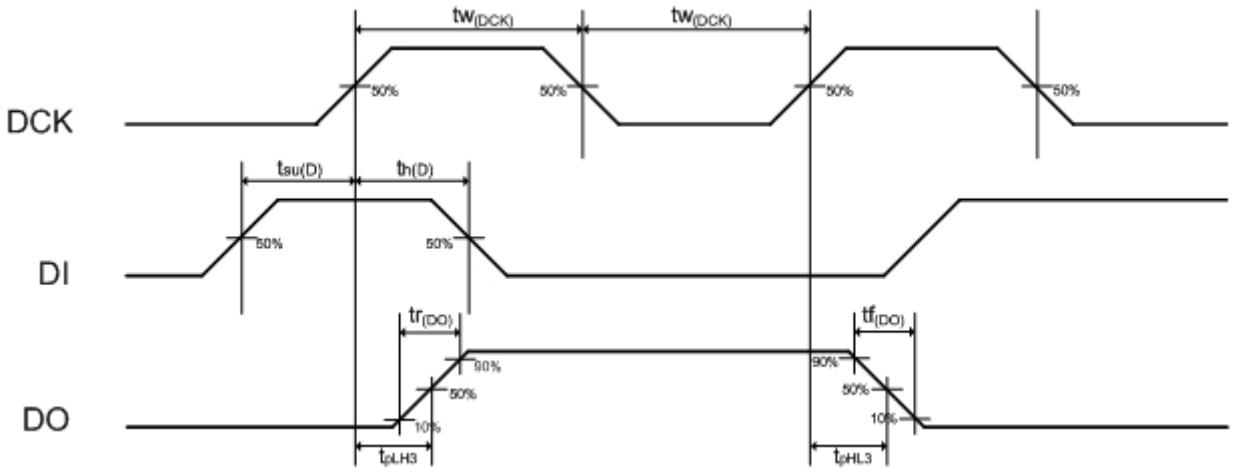
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	ENB-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 960 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	43.2	—	ns
	LAT-to-OUT0	tpLH2		—	35.9	—	
	DCK-to-DO	tpLH3		—	28.4	—	
Propagation Delay ('H' to 'L')	ENB-to-OUT0	tpHL1		—	34.1	—	
	LAT-to-OUT0	tpHL2		—	30.1	—	
	DCK-DO	tpHL3		—	29.9	—	
Pulse Duration	ENB	$tw_{(ENB)}$		20	—	—	
	LAT	$tw_{(LAT)}$		20	—	—	
	DCK	$tw_{(DCK)}$		15	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		5	—	—	
	DI	$tsu_{(D)}$		3	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(D)}$		4	—	—	
DO Rise Time		$tr_{(DO)}$		—	18.2	—	
DO Fall Time		$tf_{(DO)}$		—	19.9	—	
Output Current Rise Time		tor		—	15.0	—	
Output Current Fall Time		tof		—	30.0	—	
Output Delay Time ($OUT_{(2n)}$-to-$OUT_{(2n+1)}$)		tod		—	0.5	—	



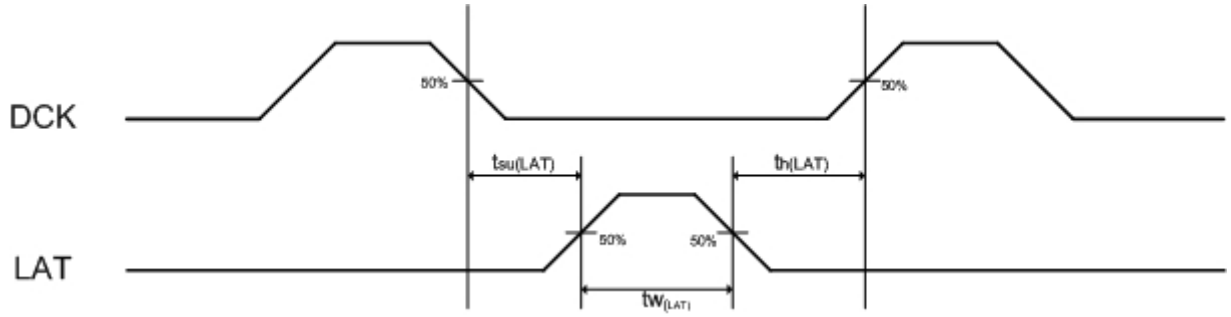
Switching Characteristics Test Circuit

Timing Diagram

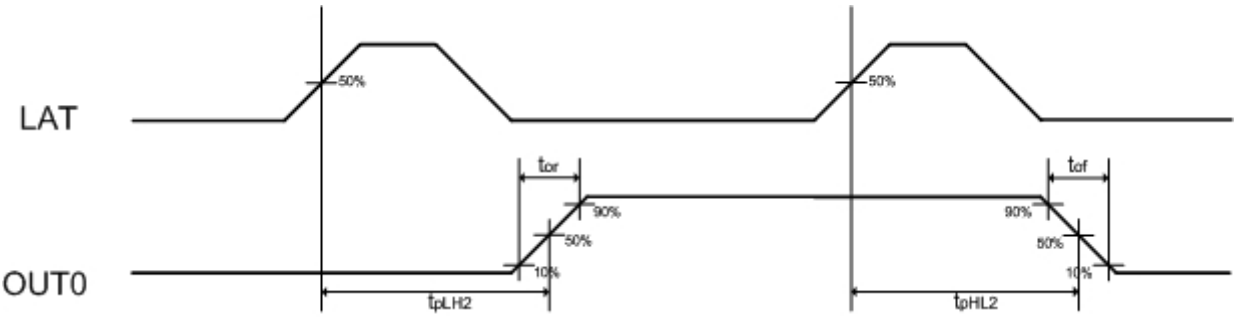
1. DCK-DI, DO



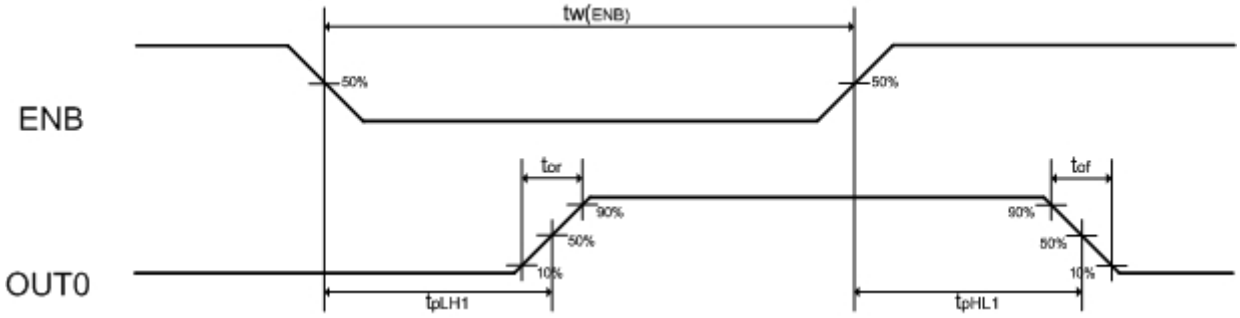
2. DCK-LAT



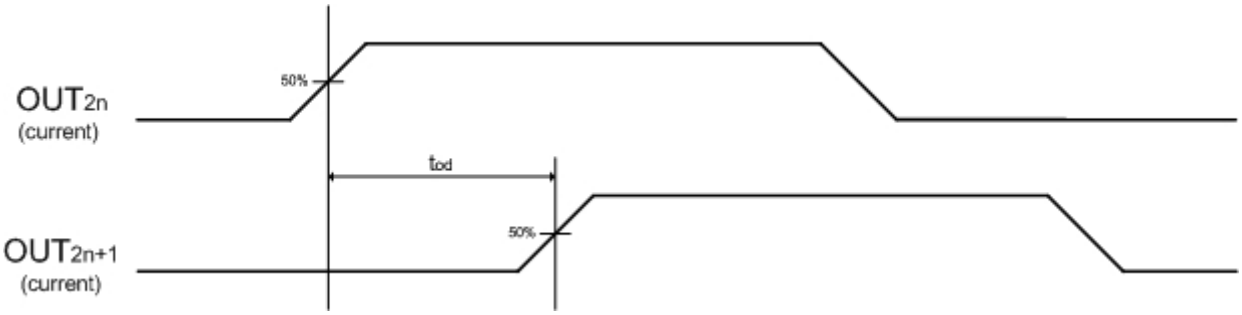
3. LAT-OUT0



4. ENB-OUT0

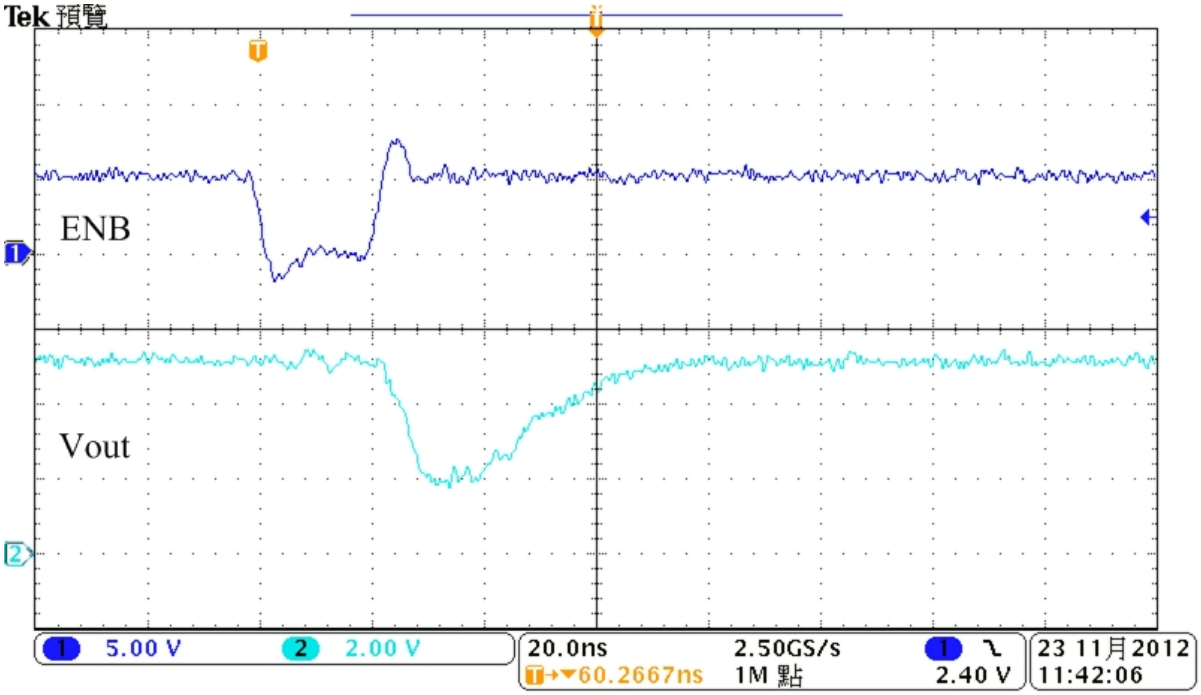


5. OUT_{2n}-OUT_{2n+1}



Fast Transient Response

The MY9168 supports the fast transient response to make high image resolution possible. The ENB pulse width of 20ns is also good enough to get a complete Vout waveform. Following shows the waveform of VDD=5V, Rext=960Ω, VLED=5V, RL=150Ω



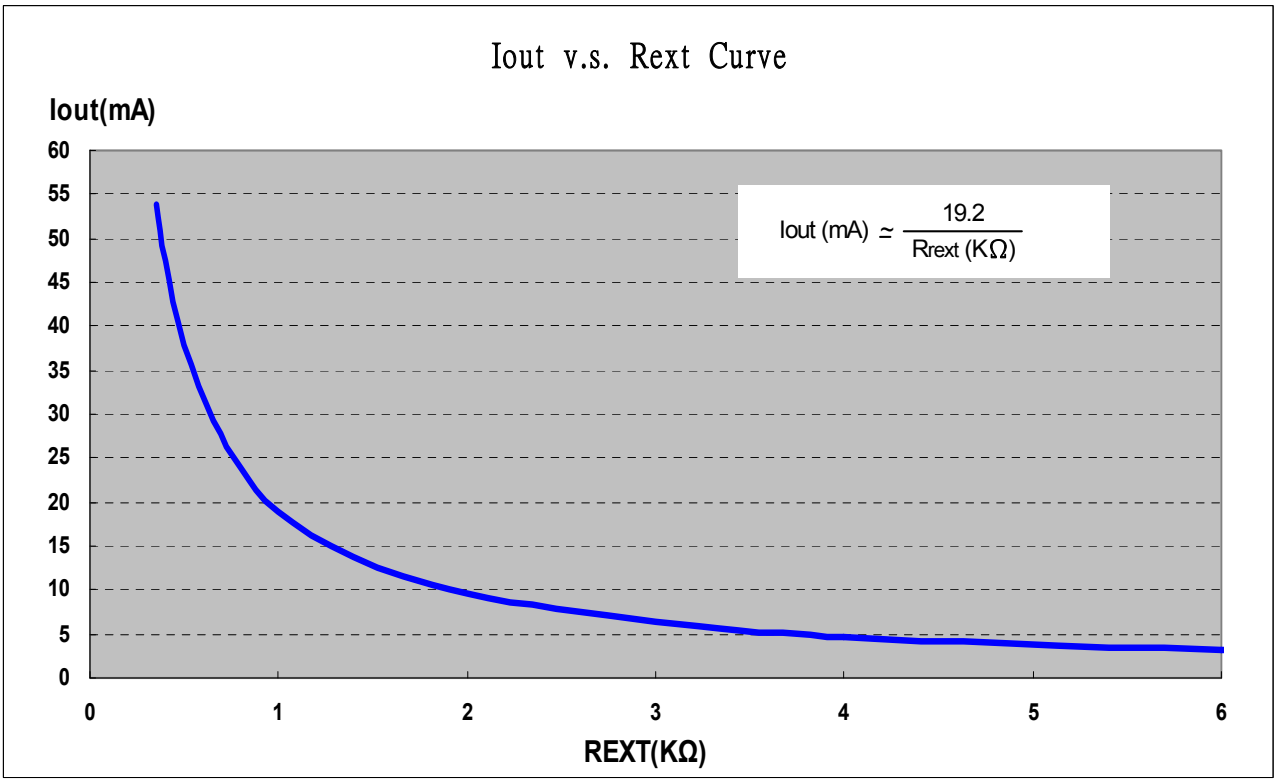
Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$Iout(mA) = \frac{19.2}{Rrext \ (K\Omega)}$$

Where Rrext is a resistor placed between REXT and GND

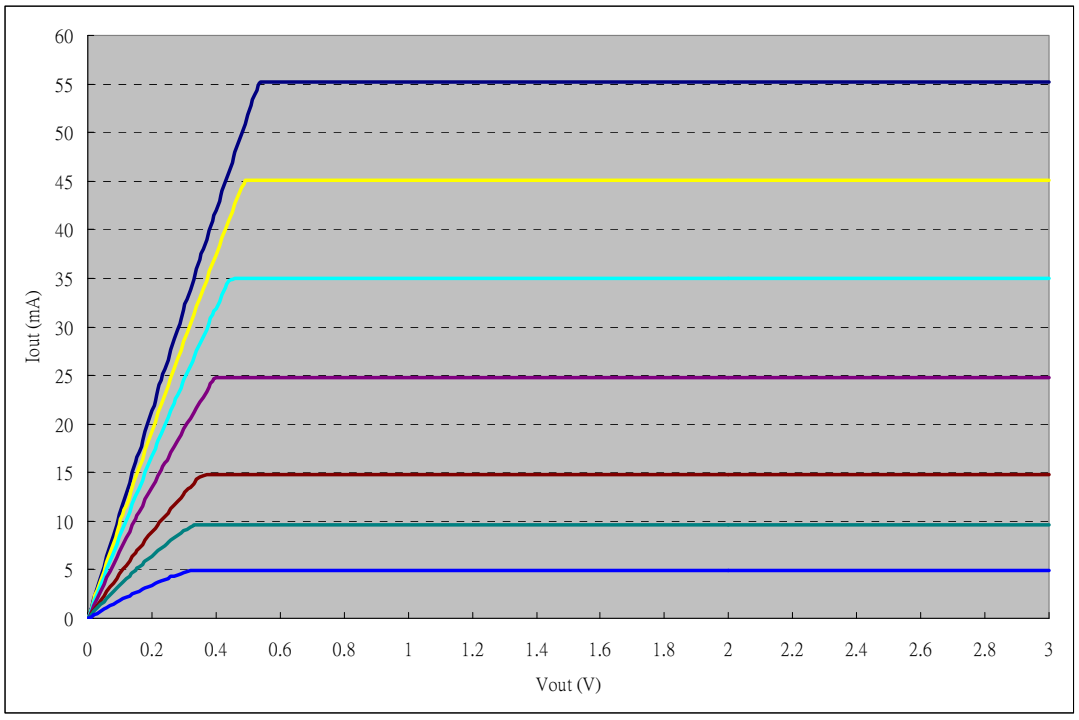
For example, Iout is 20mA when Rrext=960Ω and Iout is 3mA when Rrext=6.4KΩ



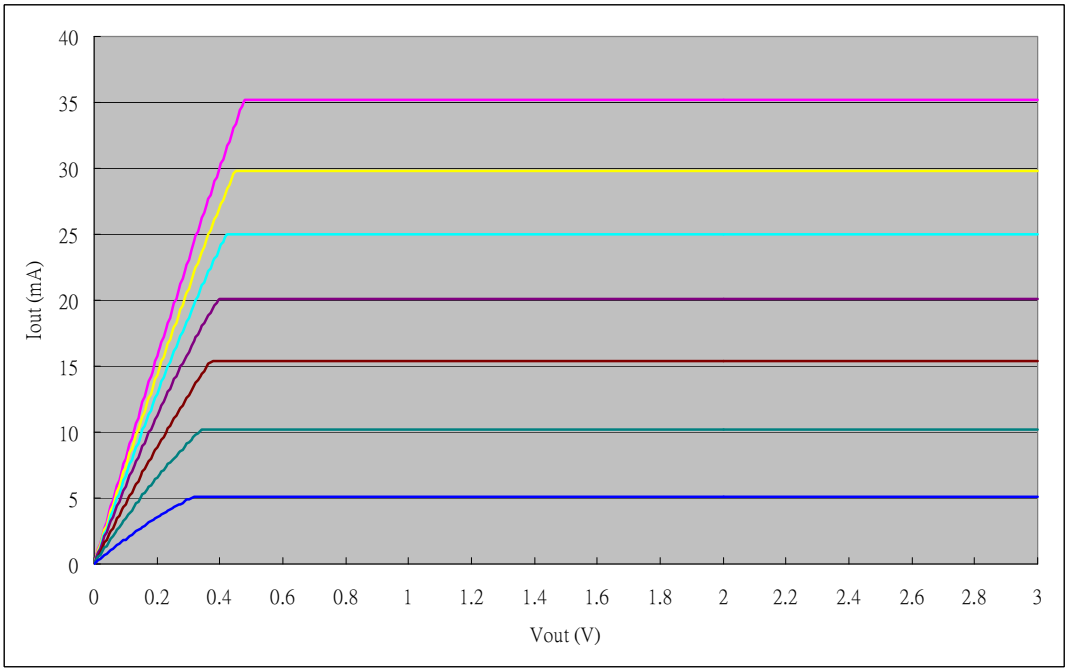
Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the MY9168 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.

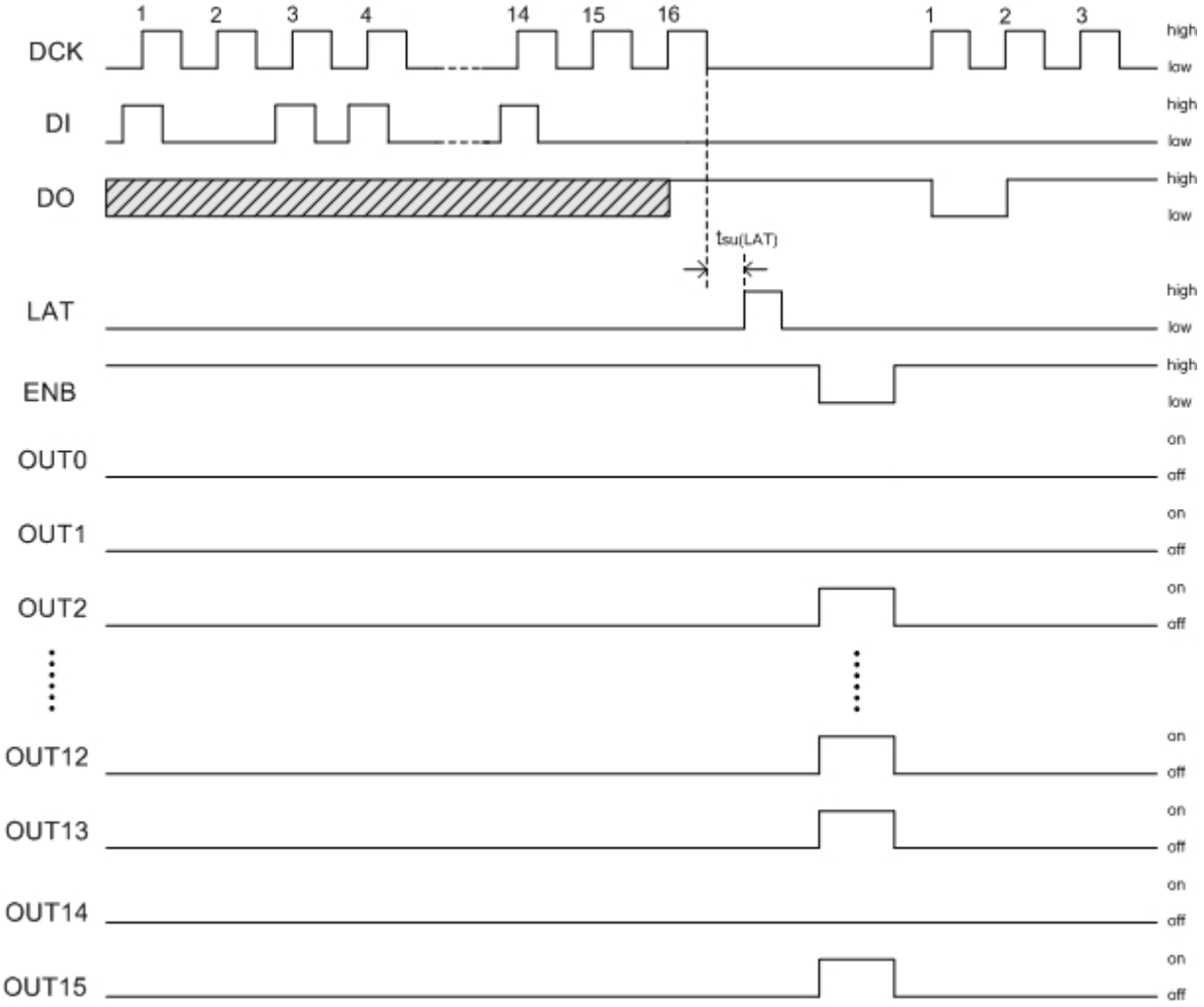
Iout v.s. Vout @ VDD=5.0V



Iout v.s. Vout @ VDD=3.3V



Serial Data Interface



The MY9168 will shifts the data to the register from the DI pin on the rising edge of data clock (DCK). After whole given frame data are transferred into 16bits shift register, the frame data are loaded into the latch register by a strobe signal (LAT). The latch action is triggered at the rising edge of LAT signal. And the serial data will be shifted out from the DO pin on the synchronization of the rising edge of DCK. Furthermore, the enable signal (ENB) will turn on all outputs when it is set to the low level.

Stagger Outputs Delay

Large in-rush currents will be induced when the system activates all the outputs at once. To reduce this interference of EMI, the MY9168 is designed to have a constant length of delay time between two output groups. The two output groups individually are the first group OUT2n and the second group OUT2n+1.

Power Dissipation

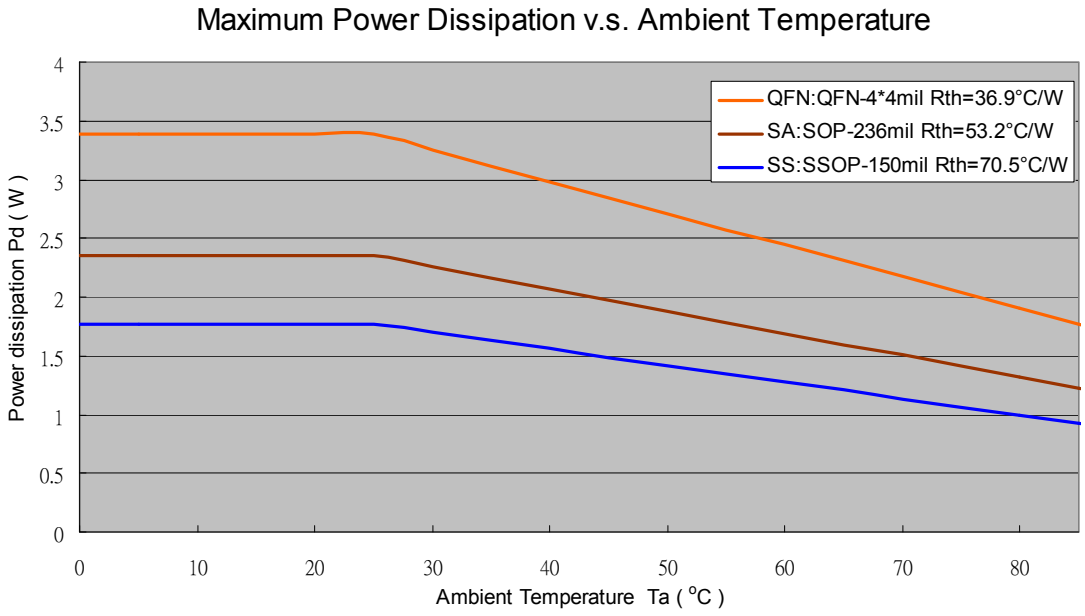
When the 16 output channels are turned on, the practical power dissipation is determined by the following equation:

$$PD\ (practical) = V_{DD} \times I_{DD} + Vout_{(0)} \times Iout_{(0)} \times Duty_{(0)} + \cdots + Vout_{(N)} \times Iout_{(N)} \times Duty_{(N)}\ ,\ where\ N=1\ to\ 15$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(^{\circ}C) - Ta(^{\circ}C)}{Rth(j\text{-}a)(^{\circ}C/Watt)}$$

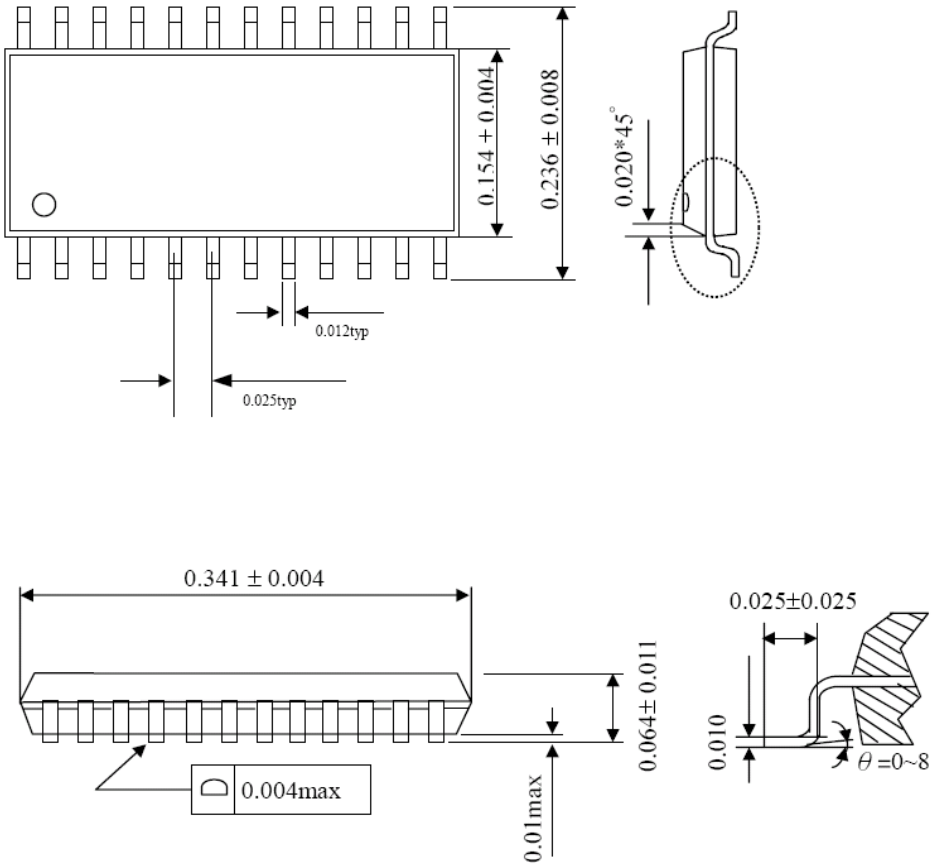
The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the four different packages.



Package Outline Dimension

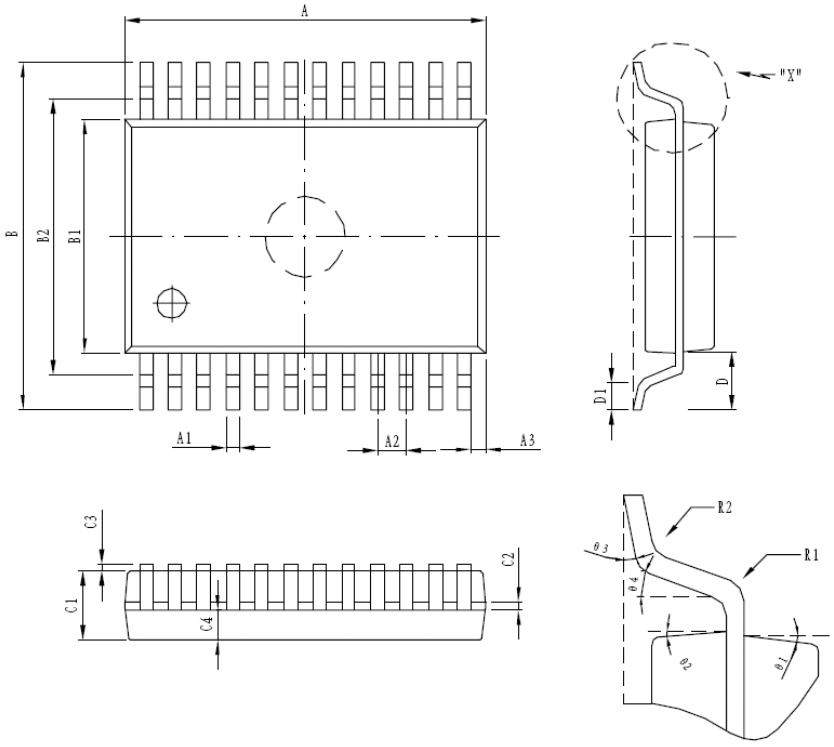
SSOP-150mil-0.635mm

Unit: inch



Package Outline Dimension

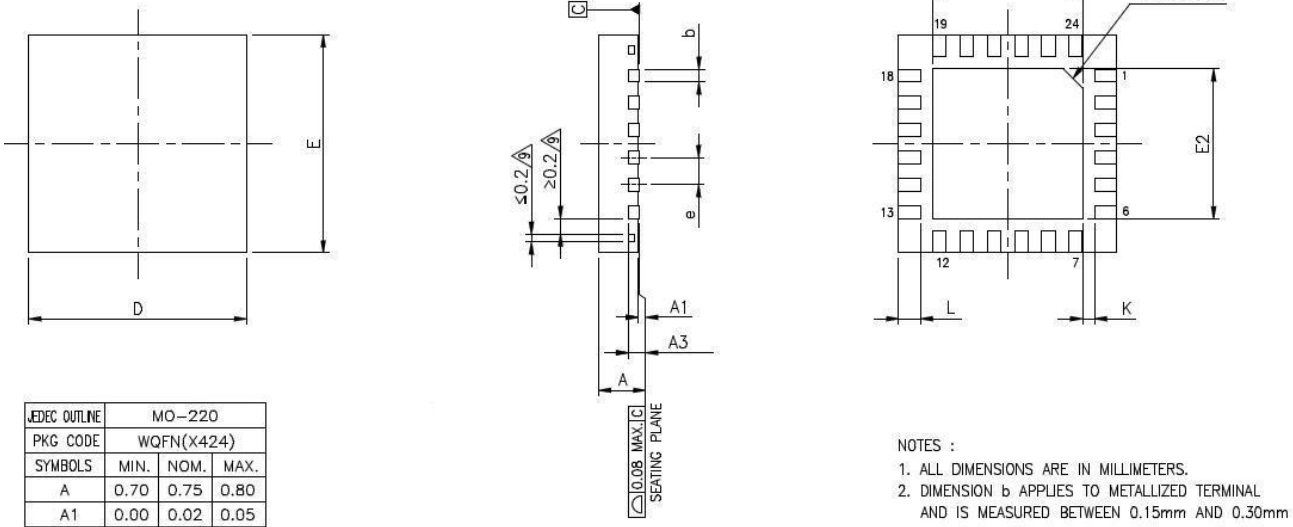
SOP-236mil-1.0mm



SYMBOL	DIMENSION(mm)		SYMBOL	DIMENSION(mm)	
	MIN.	MAX.		MIN.	MAX.
A	12.9	13.1	**C3**	0.05	0.2
A1	0.30	0.50	**C4**	0.80TYP	
A2	1.00TYP		**D**	0.95TYP	
A3	0.8TYP		**D1**	0.33	0.73
B	7.60	8.20	**R1**	0.2TYP	
B1	5.90	6.10	**R2**	0.2TYP	
B2			**θ1**	8°TYP	
C		2.20	**θ2**	10°TYP	
C1	1.70	1.90	**θ3**	4°TYP	
C2	0.15	0.30	**θ4**	5°TYP	

Package Outline Dimension

QFN24-4mm x 4mm



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X424)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
K	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

E2			D2			L			LEAD FINISH		JEDEC CODE
MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
2.40	2.50	2.55	2.40	2.50	2.55	0.35	0.40	0.45	V	X	W(V)GGD-8

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
MY-Semi Inc. will not take any responsibilities regarding the misusage of the products mentioned above. Anyone who purchases any products described herein with the above-mentioned intention or with such misused applications should accept full responsibility and indemnify. MY-Semi Inc. and its distributors and all their officers and employees shall defend jointly and severally against any and all claims and litigation and all damages, cost and expenses associated with such intention and manipulation.