Preliminary (Confidential)

MY9262

16-Channel High Accuracy Constant Current LED Driver With 16bits Adaptive Pulse Density Modulation and Power Saving Control

MY-Semi

General Description

The MY9262, 16-channel constant current LED driver with 16bits grayscale Adaptive Pulse Density Modulation (APDM) and power saving control, supports high quality LED video display applications. This distinctive APDM technology abates the non-ideal IOUT distortion due to non-symmetric transient responses and enhances the refresh rate by separating efficiently the frame waveform.

The MY9262 features a fast 30MHz DCK input, allowing a wide LED dimming (on/off) range to be implemented. This 4-wire serial interface allows a microcontroller to configure the output channels using four inputs (DI, DCK, LAT, and GCK) and a data output (DO). DO allows multiple drivers to be cascaded and operated together.

The device operates over a 3V to 5.5V input voltage range and provides 16 open-drain constant current sinking outputs that are rated to 17V and delivers up to 45mA of high accuracy current to each string of LED. The current at each output is programmable by means of an external current-sensing resistor and could be adjusted by 6bits global current control. Furthermore, the MY9262 also supports the grayscale synchronization by two functions of counter reset and data synchronization. And the sleep mode could efficiently lower down the supply current in power saving applications.

The MY9262 is available in a 24-pin SOP/SSOP/TSSOP/ QFN package and specified over the -40°C to +85°C ambient temperature range.

Features

- 3V ~ 5.5V Operating supply voltage
- 2~45mA/5V Constant current output range
- 2~30mA/3.3V Constant current output range
- 17V Rated output channels for long LED strings
- ±1.5% (typ.) LED Current accuracy between channels
- ±3% (typ.) LED Current accuracy between chips
- ±0.1% Output current regulation capability
- 16bits grayscale resolution with Adaptive Pulse Density Modulation control [patent pending]
- Grayscale counter reset selection
- Grayscale data synchronization selection
- 6bits global current control
- Sleep mode to lower down the supply current to 0.1uA
- 30MHz Clock frequency for data transfer
- 30ns fast current transient response
- Current setting by one external resister
- Schmitt trigger input
- Power on reset
- Stagger output delay for EMI reduction
- -40°C to +85°C Ambient temperature range

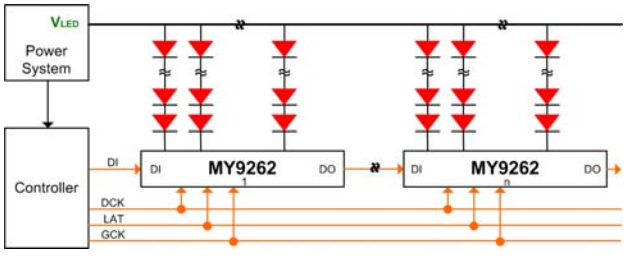
Applications

- Indoor and Outdoor LED Video Displays
- Variable Message Sign (VMS)
- Dot Matrix Module
- LCD Display Backlighting

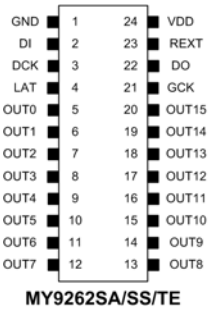
Order information

Part	Package Information	
MY9262SA	SOP24-236mil-1.0mm	2000 pcs/Reel
MY9262SS	SSOP24-150mil-0.635mm	2500 pcs/Reel
MY9262TE	TSSOP24-173mil-0.65mm (Exposed Pad)	2500 pcs/Reel
MY9262QF	QFN24-4mmx4mm-0.5mm	3000 pcs/Reel

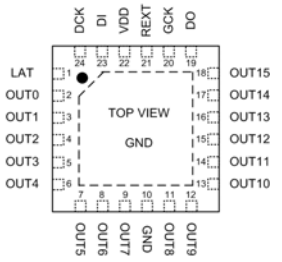
Typical Operating Circuits



Pin Configuration



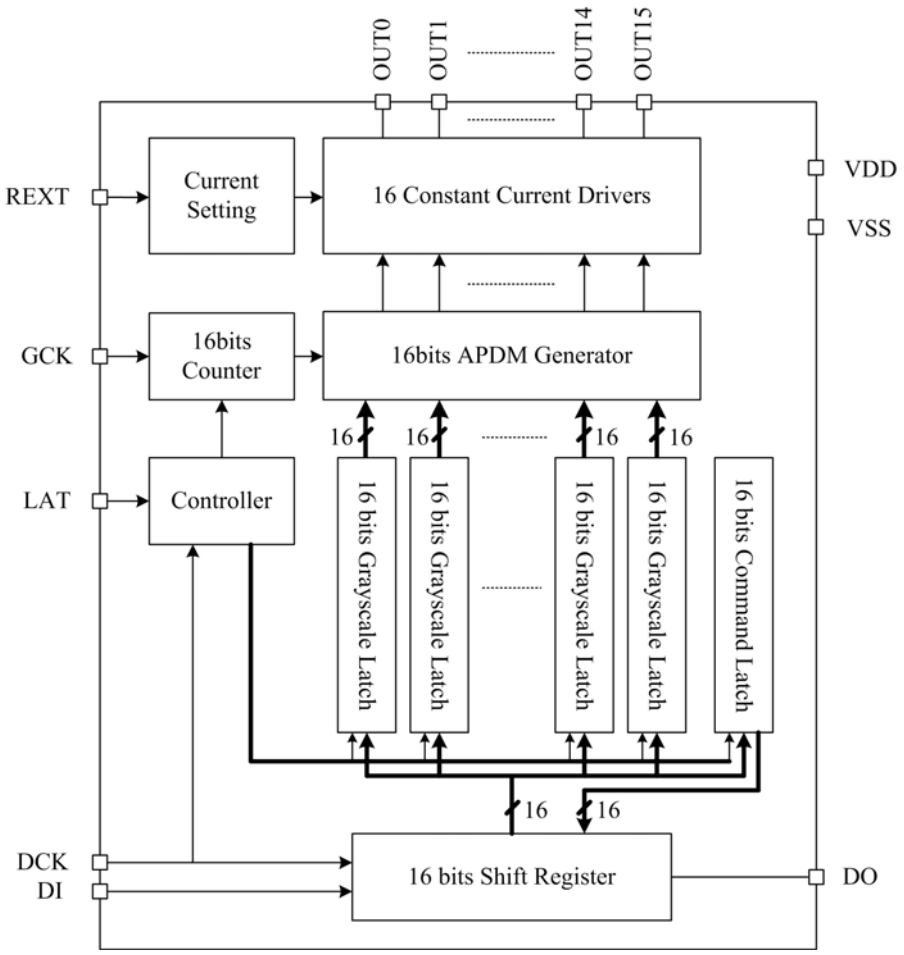
MY9262SA/SS/TE



MY9262QF

For pricing, delivery, and ordering information, pleases contact MY-Semi Inc. at +886-3-658-5656, or email to INFO@MY-Semi.com.tw or visit MY-Semi's website at www.MY-Semi.com.tw

Block Diagram

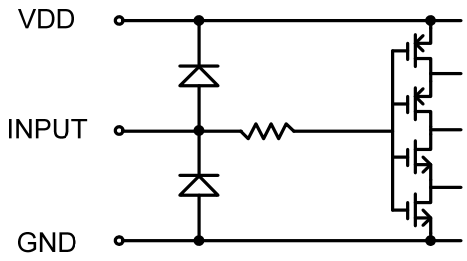


Pin Description

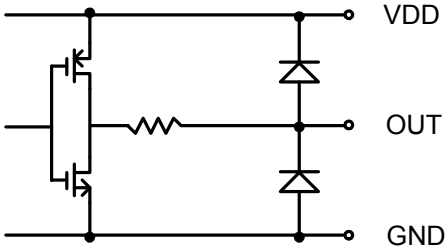
PIN No.		PIN NAME	FUNCTION
SOP/SSOP	QFN		
1	10	GND	Ground terminal.
2	23	DI	Serial data input terminal.
3	24	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
4	1	LAT	Input terminal of data strobe and mode setting. Combine DCK with LAT signal to execute the mode control
5~20	2~9,11~18	OUT0~15	Sink constant-current outputs (open-drain).
21	20	GCK	External grayscale clock input for APDM operations
22	19	DO	Serial data output terminal.
23	21	REXT	External resistors connected between REXT and GND for output current value setting.
24	22	VDD	Supply voltage terminal.

Equivalent Circuit of Inputs and Output

1. DCK, DI, LAT, GCK terminals



2. DO terminal



Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	50	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	30	MHz
Input Grayscale Frequency	FGCK	30	MHz
GND Terminal Current	IGND	800	mA
Thermal Resistance (On PCB)	Rth(j-a)	53.2 (SA:SOP-236mil-1.0mm)	°C/W
		70.5 (SS:SSOP-150mil-0.635mm)	
		31 (TE:TSSOP-173mil-0.65mm)	
		36.9 (QF:QFN24-4mmx4mm)	
Operating Supply Voltage	VDD	3.0 ~ 5.5	V
Operating Ambient Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.
(2) All voltage values are with respect to ground terminal.

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 560 Ω	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±3	±6	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 7 KΩ	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4		—	±3	±6	%
Output Voltage Regulation*3	% / VOUT	Rrext = 560 Ω VOUT = 1 V ~ 3 V	—	—	±.0.1	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 560 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current *5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	1.7	2.5	mA
	$I_{DD2(off)}$	input signal is static Rrext = 7 KΩ all outputs turn off	—	2.0	—	
	$I_{DD1(on)}$	input signal is static Rrext = 7 KΩ all outputs turn on	—	2.0	—	
	$I_{DD3(off)}$	input signal is static Rrext = 560 Ω all outputs turn off	—	4.0	—	
	$I_{DD2(on)}$	input signal is static Rrext = 560 Ω all outputs turn on	—	4.0	—	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right) \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

*5 IO excluded.

Electrical Characteristics (VDD = 3.3 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 560 Ω	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±3	±6	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 7 KΩ	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4			±3	±6	%
Output Voltage Regulation*3	% / VOUT	Rrext = 560 Ω VOUT = 1 V ~ 3 V	—	—	±0.1	% / V
Supply Voltage Regulation*4	% / VDD	Rrext =560 Ω VDD = 3 V ~ 5.5 V	—	±0.7	±1	
Supply Current *5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	1.2	2.0	mA
	$I_{DD2(off)}$	input signal is static Rrext = 7 KΩ all outputs turn off	—	2.0	—	
	$I_{DD1(on)}$	input signal is static Rrext = 7 KΩ all outputs turn on	—	2.0	—	
	$I_{DD3(off)}$	input signal is static Rrext = 560 Ω all outputs turn off	—	4.0	—	
	$I_{DD2(on)}$	input signal is static Rrext = 560 Ω all outputs turn on	—	4.0	—	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

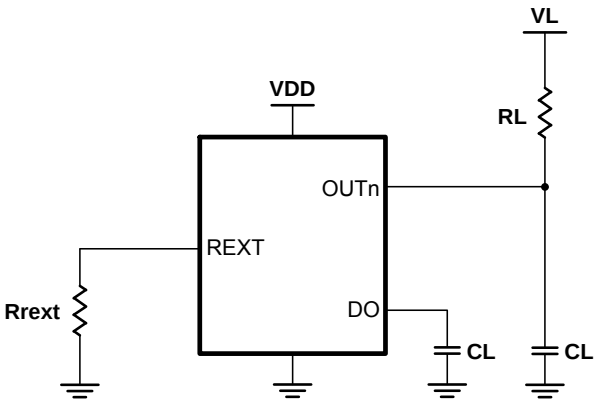
*5 IO excluded.

Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L to ‘H’)	GCK-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 560 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	25	45	ns
	LAT-DO	tpLH2		—	25	45	
	DCK-DO	tpLH3		—	24	44	
Propagation Delay (‘H’ to ‘L’)	GCK-to-OUT0	tpHL1		—	20	40	
	LAT-DO	tpHL2		—	20	40	
	DCK-DO	tpHL3		—	28	48	
Pulse Duration	LAT	$tw_{(LAT)}$		50			
	GCK	$tw_{(GCK)}$		15			
	DCK	$tw_{(DCK)}$		15			
Setup Time	LAT	$tsu_{(LAT)}$		5			
	DI	$tsu_{(D)}$		3			
Hold Time	LAT	$th_{(LAT)}$		20			
	DI	$th_{(D)}$		4			
DO Rise Time		$tr_{(DO)}$			16		
DO Fall Time		$tf_{(DO)}$			18		
Output Current Rise Time		tor		—	15	—	
Output Current Fall Time		tof		—	18	—	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+8)}$)		tod		—	16	—	
Data Clock Frequency		F_{DCK}				30	Hz
Grayscale Clock Frequency		F_{GCK}				30	

Switching Characteristics (VDD = 3.3V, Ta = 25°C unless otherwise noted)

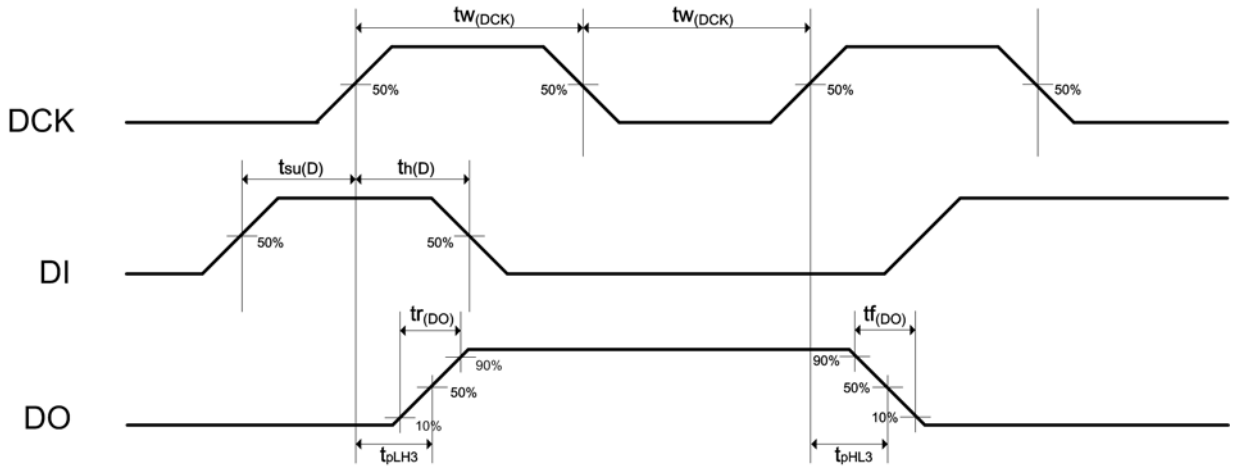
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L to ‘H’)	GCK-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 560 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	47	67	ns
	LAT-DO	tpLH2		—	48	68	
	DCK-DO	tpLH3		—	30	50	
Propagation Delay (‘H’ to ‘L’)	GCK-to-OUT0	tpHL1		—	30	50	
	LAT-DO	tpHL2		—	30	50	
	DCK-DO	tpHL3		—	30	50	
Pulse Duration	LAT	$tw_{(LAT)}$		50			
	GCK	$tw_{(GCK)}$		20			
	DCK	$tw_{(DCK)}$		20			
Setup Time	LAT	$tsu_{(LAT)}$		5			
	DI	$tsu_{(D)}$		3			
Hold Time	LAT	$th_{(LAT)}$		20			
	DI	$th_{(D)}$		4			
DO Rise Time		$tr_{(DO)}$			24		
DO Fall Time		$tf_{(DO)}$			23.5		
Output Current Rise Time		tor		—	24.5	—	
Output Current Fall Time		tof		—	23.5	—	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+8)}$)		tod		—	26	—	
Data Clock Frequency		F_{DCK}				25	Hz
Grayscale Clock Frequency		F_{GCK}				20	



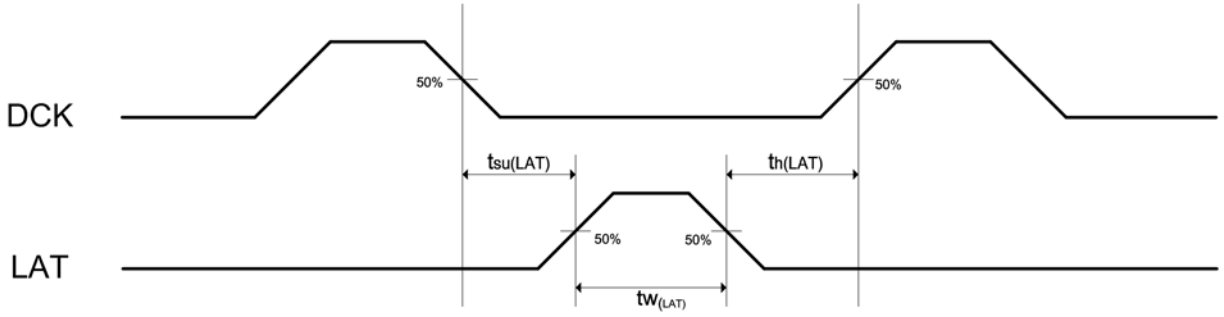
Switching Characteristics Test Circuit

Timing Diagram

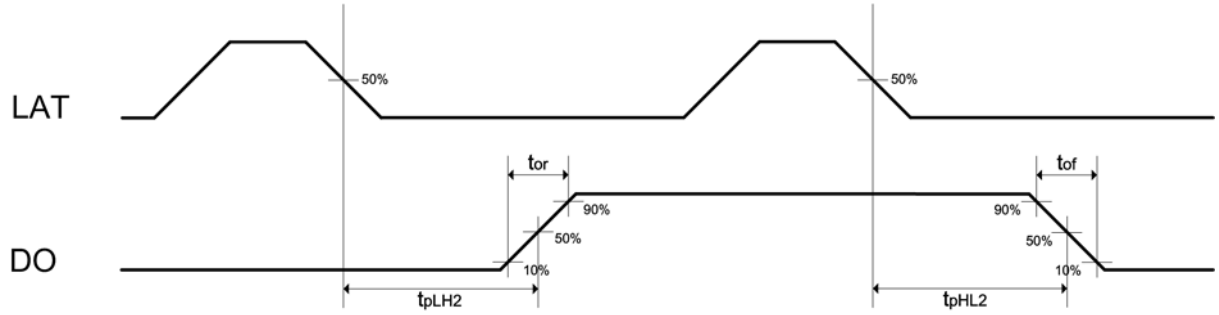
1. DCK-DI, DO



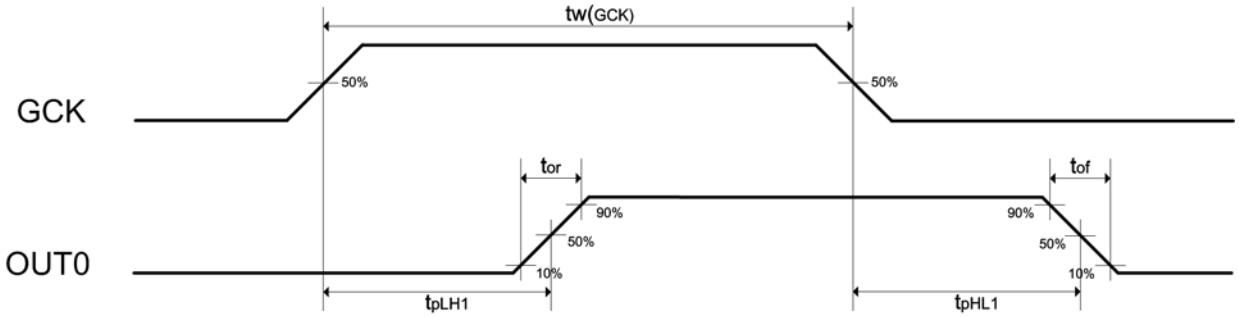
2. DCK-LAT



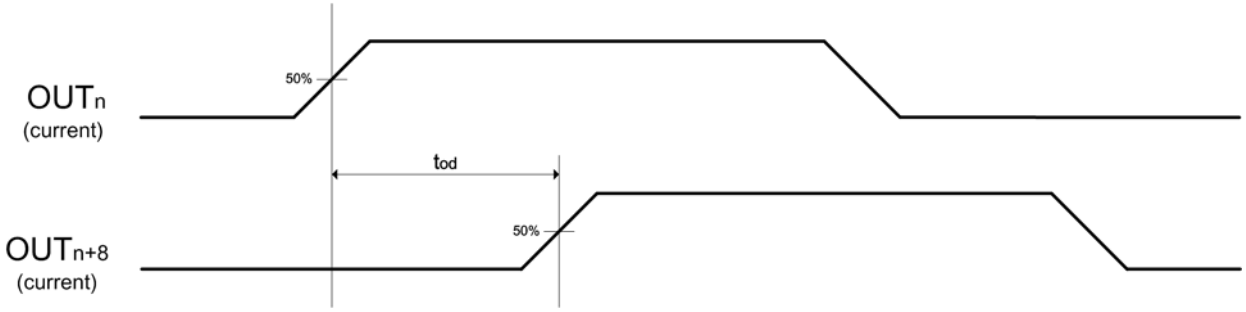
3. LAT-DO



4. GCK-OUT0



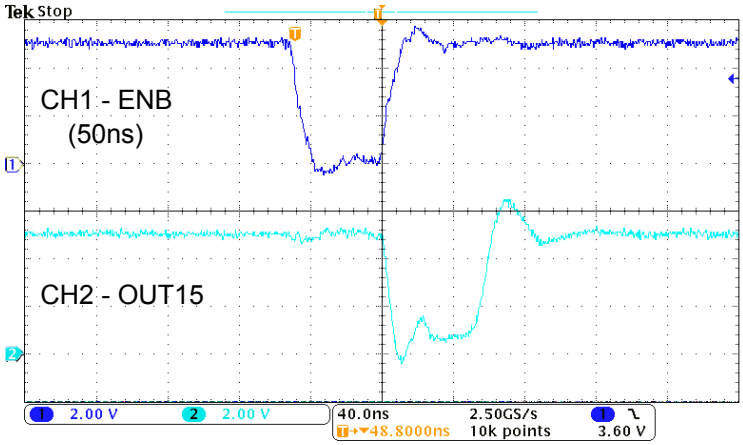
5. OUTn-OUTn+8



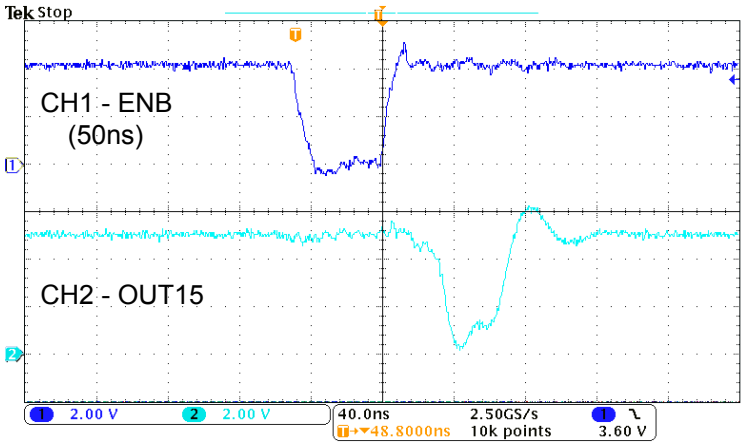
Fast Transient Response

The MY9262 supports the fast transient response to make high image resolution possible. The GCK period of 50ns is guaranteed to get a complete Vout waveform.
Test condition: VL=5V, RL=150Ω, CL=13pF, Rrext=560Ω

Output Voltage Waveform @VDD=5V



Output Voltage Waveform @VDD=3.3V



Reference Resistor

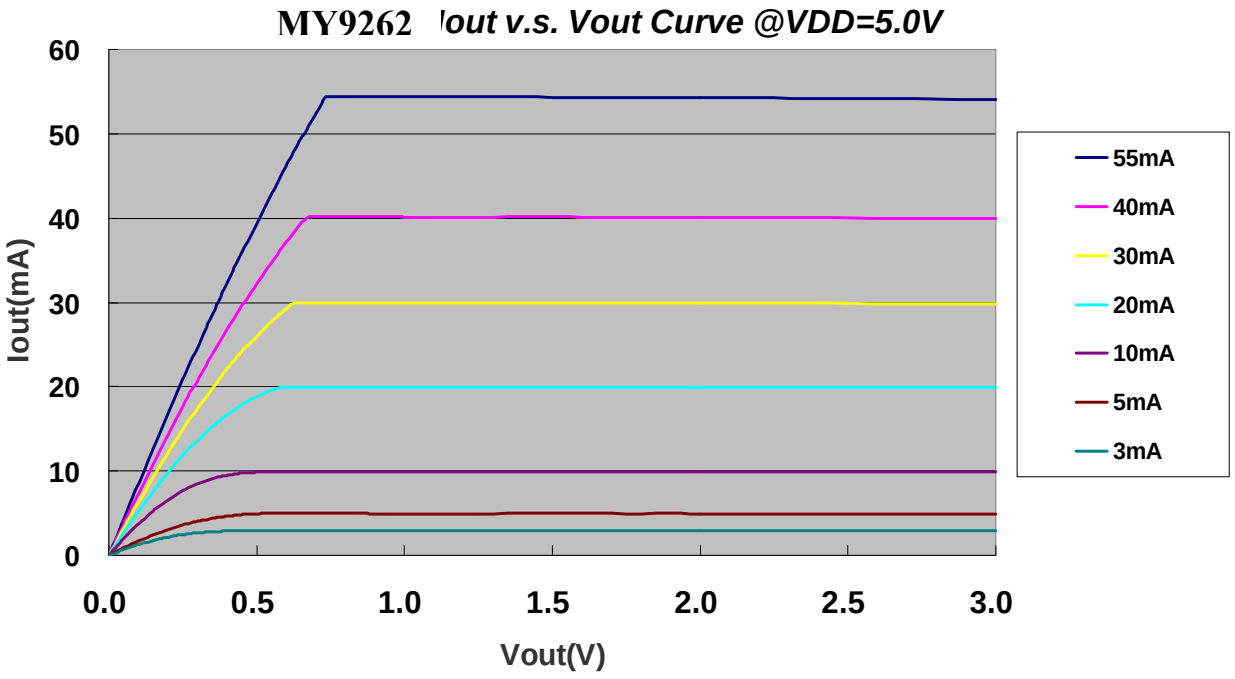
The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

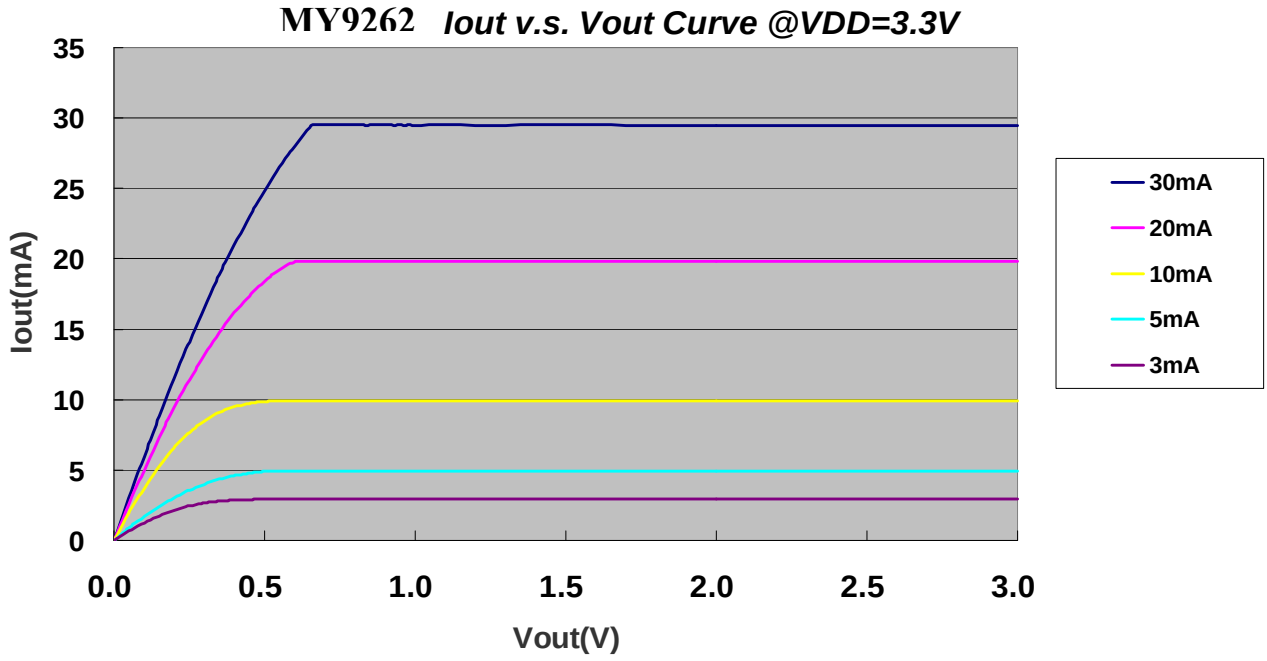
$$Iout(mA) = \frac{14}{Rrext \quad (K\Omega)} \times Gain$$

Where Rrext is a resistor placed between REXT and GND
And Gain is the factor of global current control refer to page 16
For example, Iout is 25mA when Rrext=560Ω

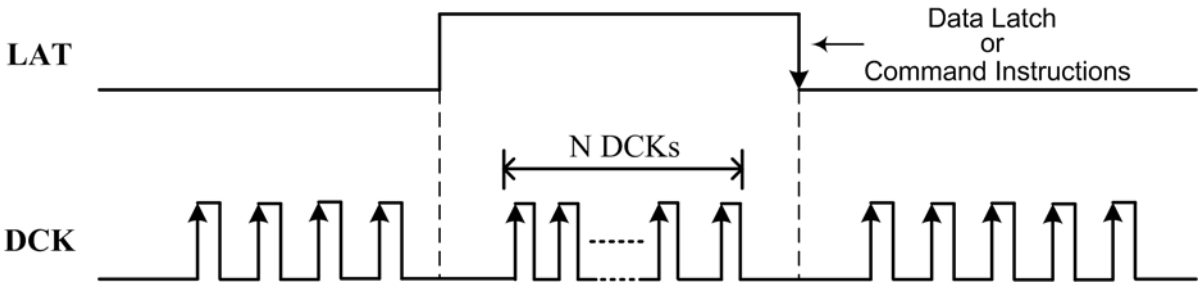
Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the MY9262 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.



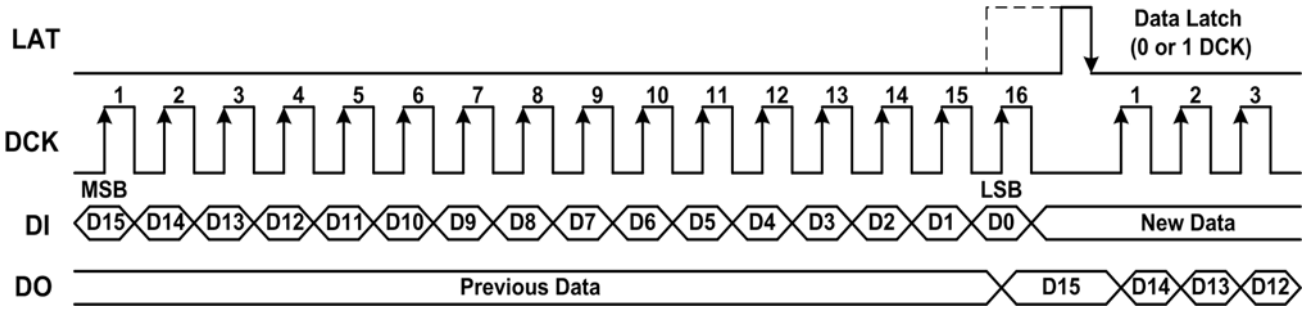


Instructions

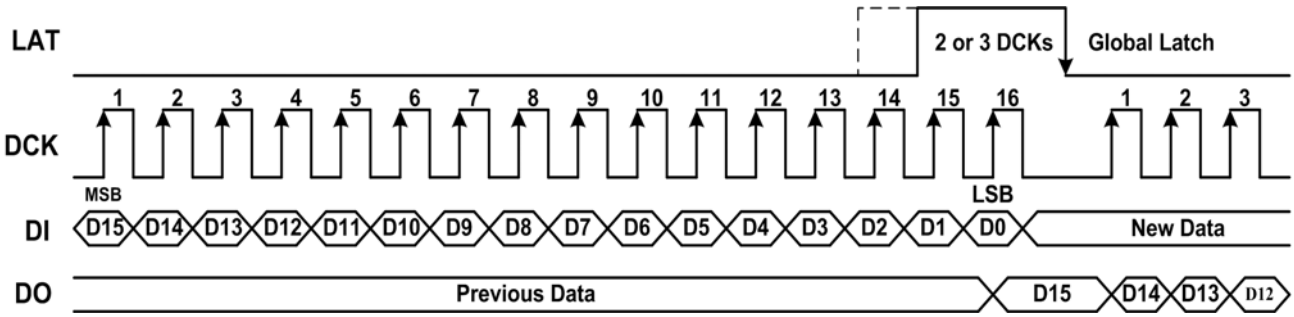


Instruction Name	Number of DCK Pulses when LAT is at High	Function Description
Data Latch	0 or 1	Strobes image data into temporary registers. In this time, constant current outputs are not updated to a new frame data.
Global Latch	2 or 3	Strobes image data from temporary registers into an APDM/PWM generator. In this time, constant current outputs are updated to a new frame data.
Reading Command	4 or 5	Read out command data from the command latch cell to the 16bits shift registers. And the command data could shift out from DO pin by serial DCK pulses.
Writing Command	10 or 11	Strobes command data from the 16bits shift register into the command latch cell. Note that this instruction must follow by the "Enable Writing Command" instruction.
Reset APDM/PWM Counter	12 or 13	This instruction will reset APDM/PWM counter to synchronize a new frame if CMD[11]="H".
Enable Writing Command	14 or 15	This instruction enables the "Writing Command" instruction. This instruction should be executed before the "Writing Command" instruction every time.

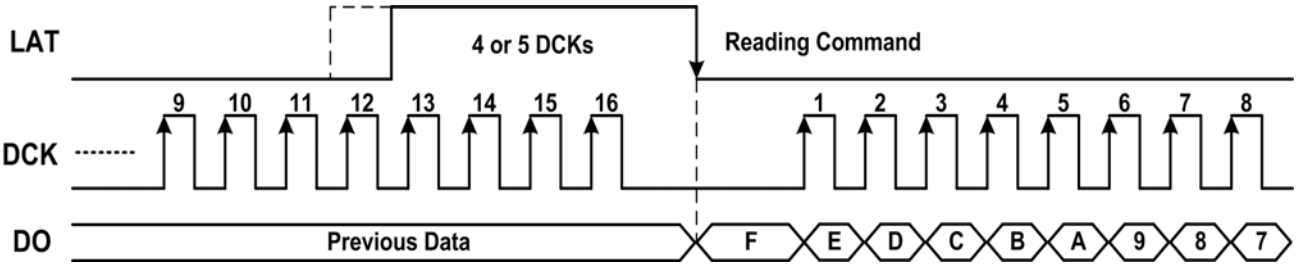
Data Latch



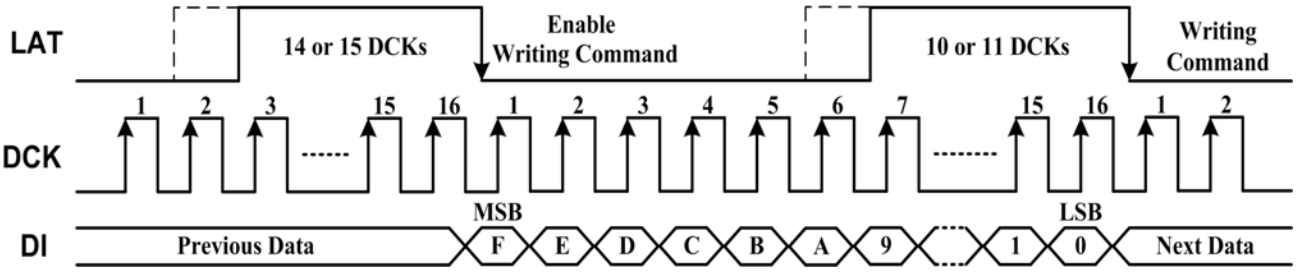
Global Latch



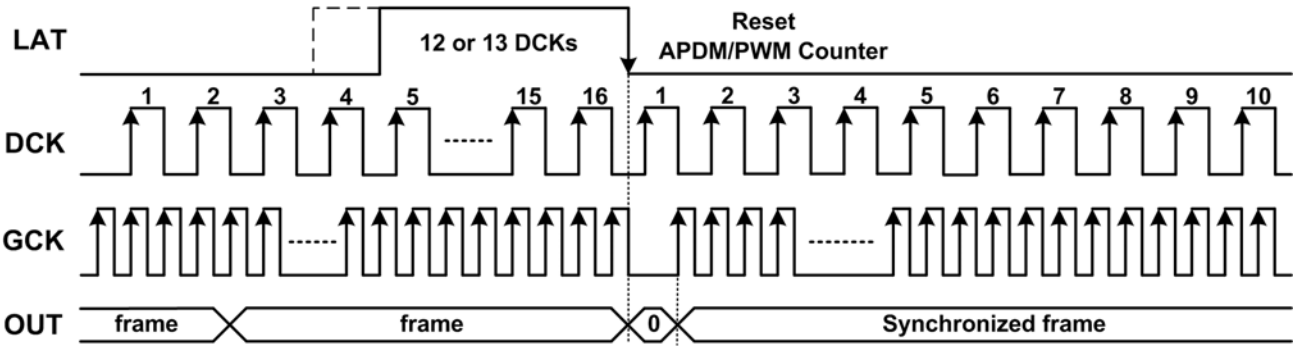
Reading Command



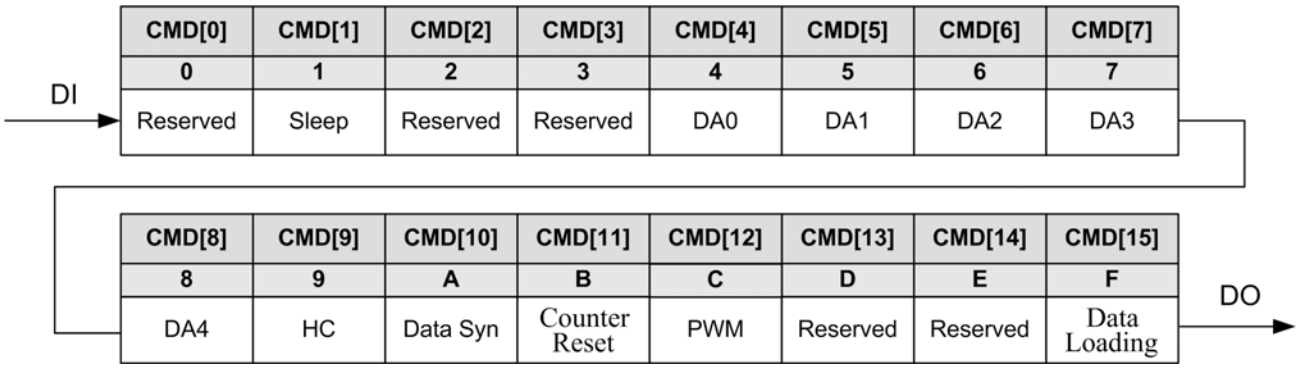
Writing Command



Reset APDM/PWM Counter (set CMD[11]=”1”)

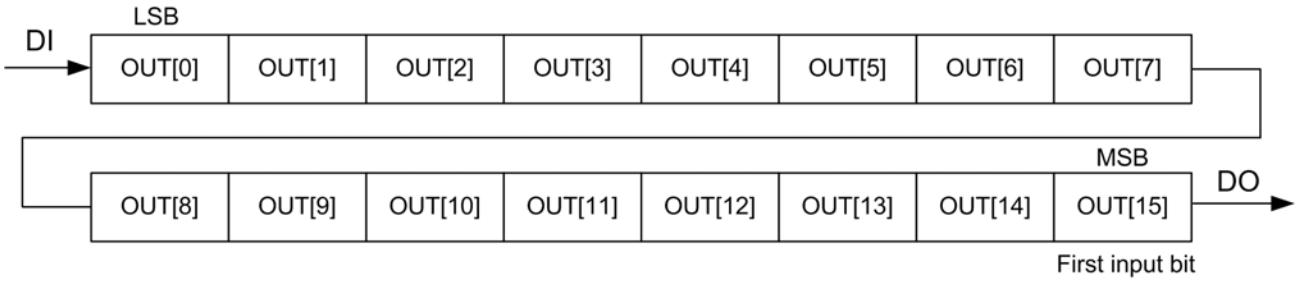


Command Data Format



CMD Bit	Initial Value	Value	Function	Description
CMD[15]	1'b0	1'b0	Mode0	Data transmitting Format: 15 times of data latch + one global latch
		1'b1	Mode1	Data transmitting Format: 16 times of data latch + one global latch
CMD[14:13]	2'b00	Reserved	Reserved	Reserved bits
CMD[12]	1'b0	1'b1	PWM mode	Enter the PWM mode to abate the transient loss when MY9262 is as a PWM generator when CMD[12]=1'b1 => PWM mode when CMD[12]= 1'b0 => APDM mode
		1'b0	APDM mode	
CMD[11]	1'b0	1'b0	Disable	Disable
		1'b1	Enable	Execute counter reset by inserting 12 or 13 DCKs (rising edge) when LAT keeps at high
CMD[10]	1'b0	1'b0	Auto Synchronization	When the device receives a latch signal, the new frame is updated until the end of old frame
		1'b1	Manual Synchronization	When the device receives a latch signal, the new frame is updated immediately
CMD[9:4]	6'b101011	6'b000000~ 6'b111111	G.C.C	6bits DA data for global current control (allow 64-step programmable current gain)
CMD[3:2]	2'b00	Reserved	Reserved	Reserved bits
CMD[1]	1'b0	1'b1	Sleep Mode	Enter the sleep mode to lower down the power supply current to 0.1uA when CMD[1]=1'b1 => Sleep when CMD[1]= 1'b0 => Normal
		1'b0	Normal Mode	
CMD[0]	1'b0	Reserved	Reserved	Reserved bits

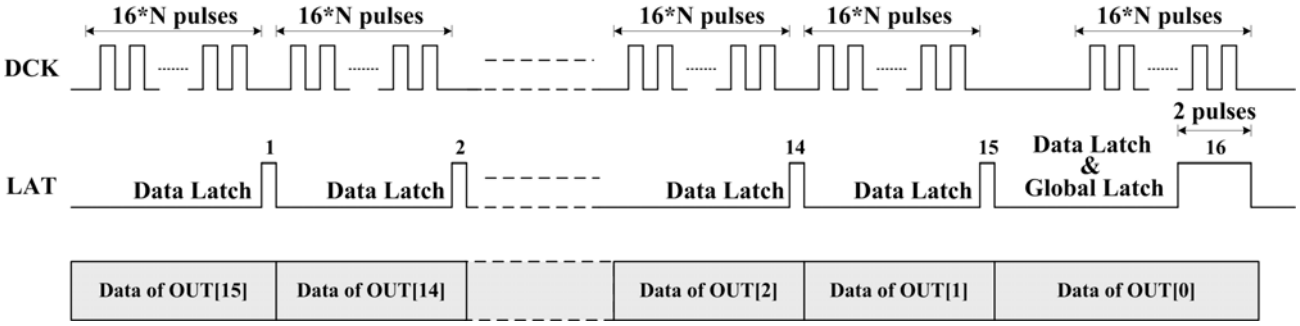
Image Data Format



16bits APDM/PWM data are transmitted into the 16bits shift register according to the format illustrated above. The first input bit is the most significant bit of each channel.

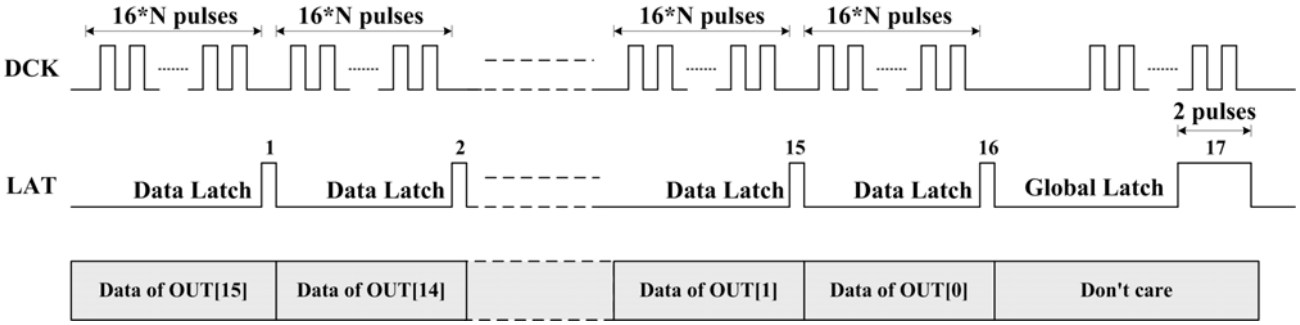
Data Transmitting Protocol

MODE0 (CMD[15]="0")



This data transmitting mode is comprised of 15 data latches and one global latch. The first data latch strobes image data for OUT[15]. And the last global latch strobes image data for OUT[0] and loads all image data of 16 channels into the APDM/PWM generator. N is the number of devices in series.

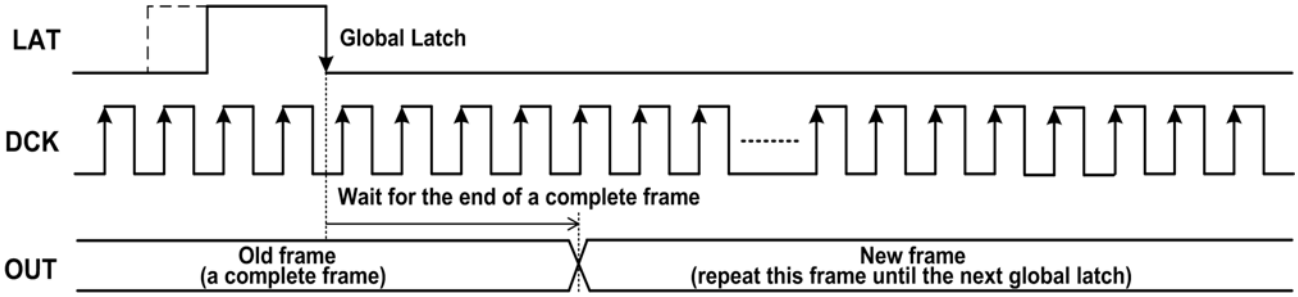
MODE1 (CMD[15]="1")



This data transmitting mode is comprised of 16 data latches and one global latch. The first data latch strobes image data for OUT[15]. And the last global latch loads all image data of 16 channels into the APDM/PWM generator but doesn't strobe any image data for output channels. N is the number of devices in series.

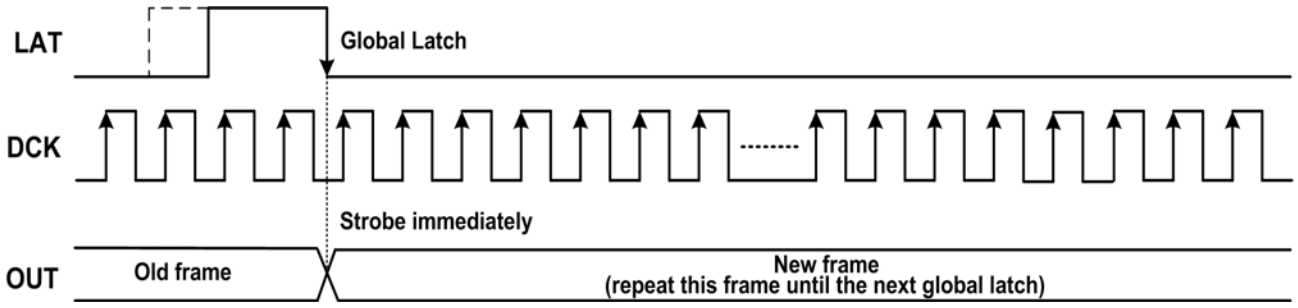
Data Synchronization

Auto Synchronization (CMD[10]="0")



MY9262 could abate the grayscale loss during the renewal of frame by this approach of auto synchronization. When the command bit CMD[10] is set to "0", this function could be executed automatically. After a global latch, all OUTs would accomplish a complete frame of old data and then update new frame data. Therefore, each frame maintains the fixed time and the assigned grayscale. A controller just provides a free-running GCK for grayscale display in this mode.

Manual Synchronization (CMD[10]="1")

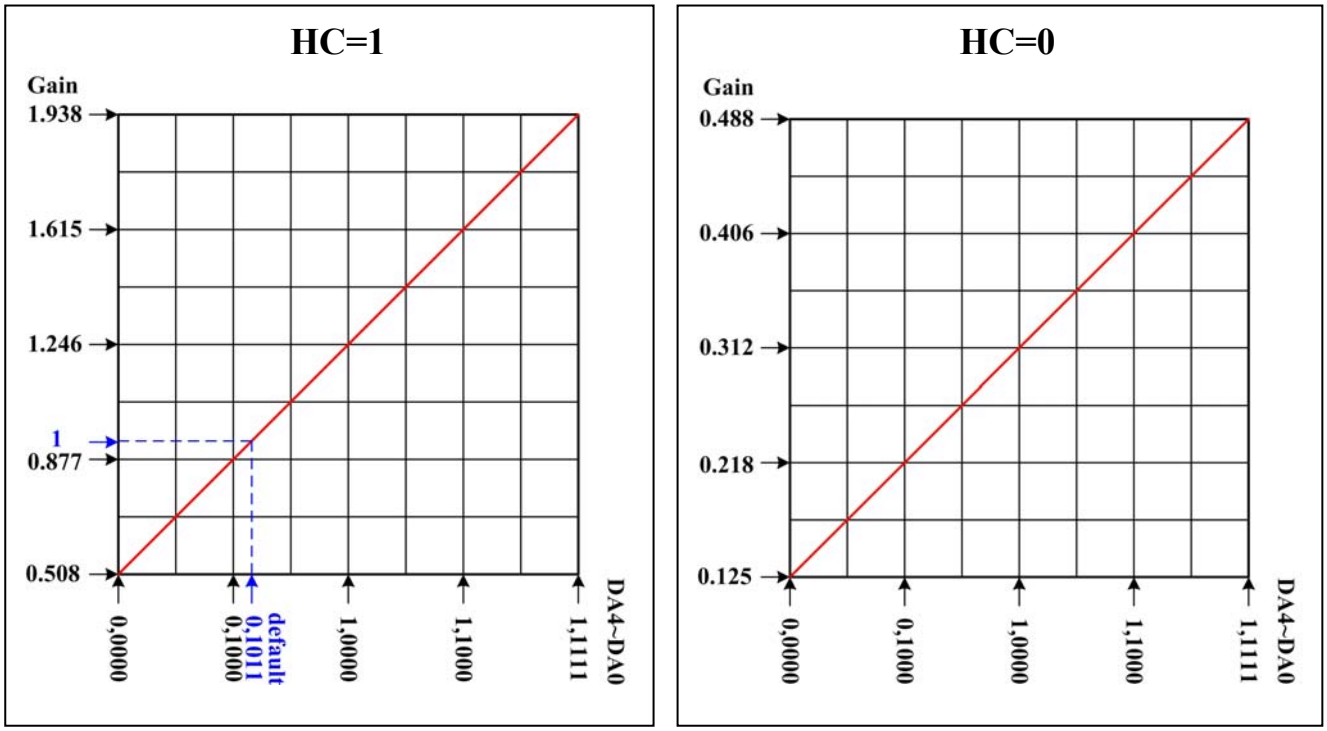


When the command bit CMD[10] is set to "1", the new frame data would be updated immediately. The old frame loses probably a little grayscale due to a non-complete frame time. In this mode, a controller must calculate carefully the number of GCKs in order to synchronize a frame.

Stagger Outputs Delay

Large in-rush currents will be induced when the system activates all the outputs at once. To reduce this interference of EMI, the MY9262 is designed to have a constant length of delay time (around 16ns) between two output groups. The two output groups individually are the first group from OUT0 to OUT7 and the second group from OUT8 to OUT15.

Global Current Control (GCC)



The MY9262 provides 6bits global current control which could adjust the output current by 64 steps. The GCC bits are included in the command data defined as follow:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	HC	DA4	DA3	DA2	DA1	DA0	—	—	—	—

The relationship between the current gain and GCC bits is described below:

HC=1, Gain = (3 x D + 33) / 65, the gain range is from 0.508 to 1.938

HC=0, Gain = (3 x D + 33) / 256, the gain range is from 0.125 to 0.488

Where D = DA4 x 2^4 + DA3 x 2^3 + DA2 x 2^2 + DA1 x 2^1 + DA0 x 2^0

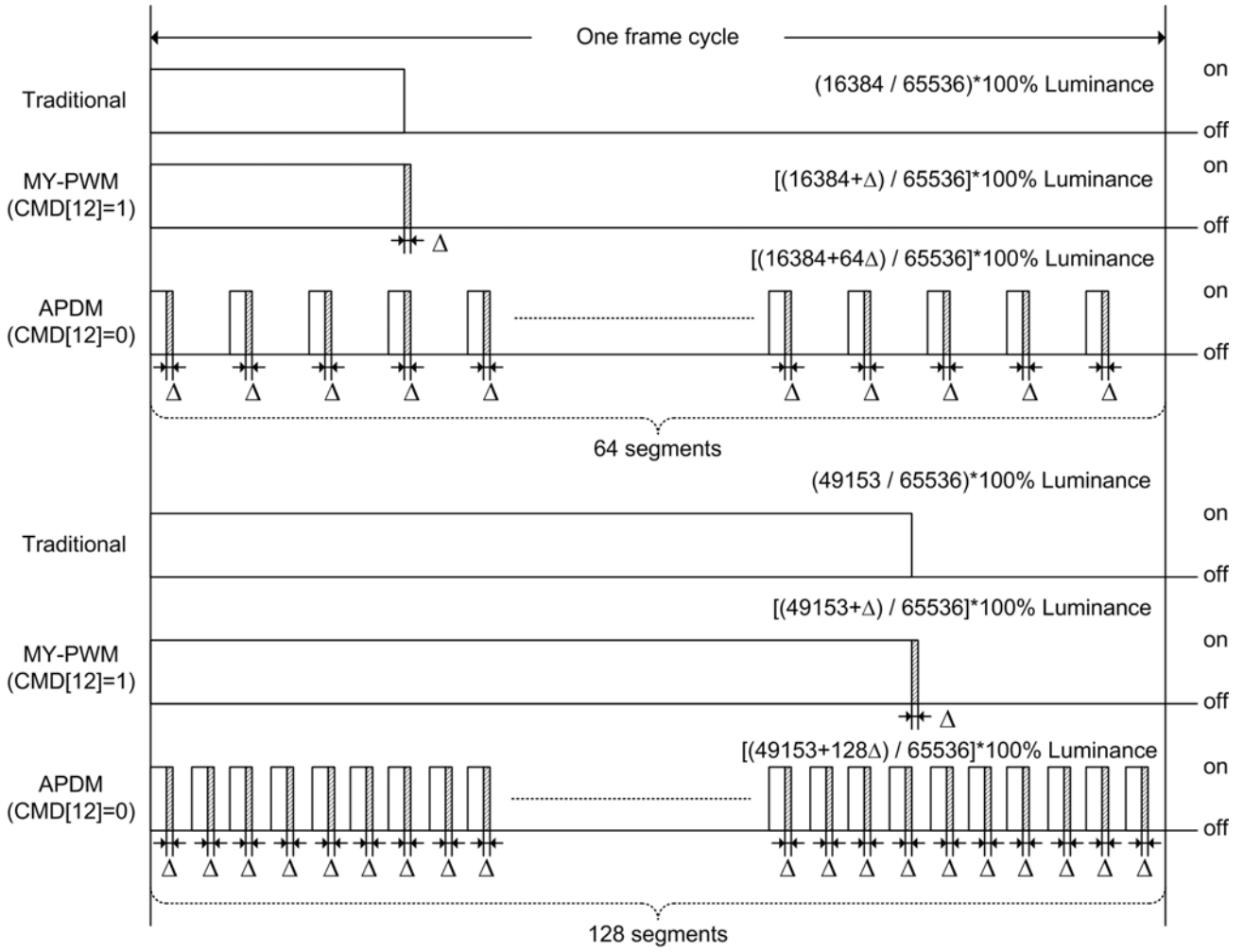
For example, HC=1 and DA[4:0]=5'b11000

D = 1x 2^4 + 1 x 2^3 + 0 x 2^2 + 0 x 2^1 + 0 x 2^0 = 24 and Gain = (3 x 24 + 33) / 65 =1.615

Sleep Mode

In order to power saving, MY9262 supports the sleep mode to turn off all circuits except for digital ones. It is necessary to set CMD[1]="1" to enter into this mode. In the sleep mode, the supply current maintains below 0.1uA because all analog circuits are shutdown but the digital interface is still activated in order to receive external digital data. When CMD[1] is reset to "0", MY9262 would revive automatically.

Adaptive Pulse Density Modulation with Δ-Width Correction



Adaptive Pulse Density Modulation (APDM) is a technique to improve output current waveform distortion and increase visual refresh rate. The adaptive output waveform is determined automatically by the grayscale value. When all outputs operate at high grayscale resolution (grayscale resolution ≧ 50%), the output waveform is divided into 128 segments to increase visual refresh rate. Otherwise the output waveform is divided into 64 segments at low grayscale resolution to improve output current waveform distortion. And the Δ-width correction (Δ≠0) is used to compensate the non-ideal output current transient response.

When CMD[12]=”0”, the output waveform operates according to APDM. When CMD[12]=”1”, the output waveform is a form of non-scrambling PWM in order to drive high power LED and decrease the transient loss.

Power Dissipation

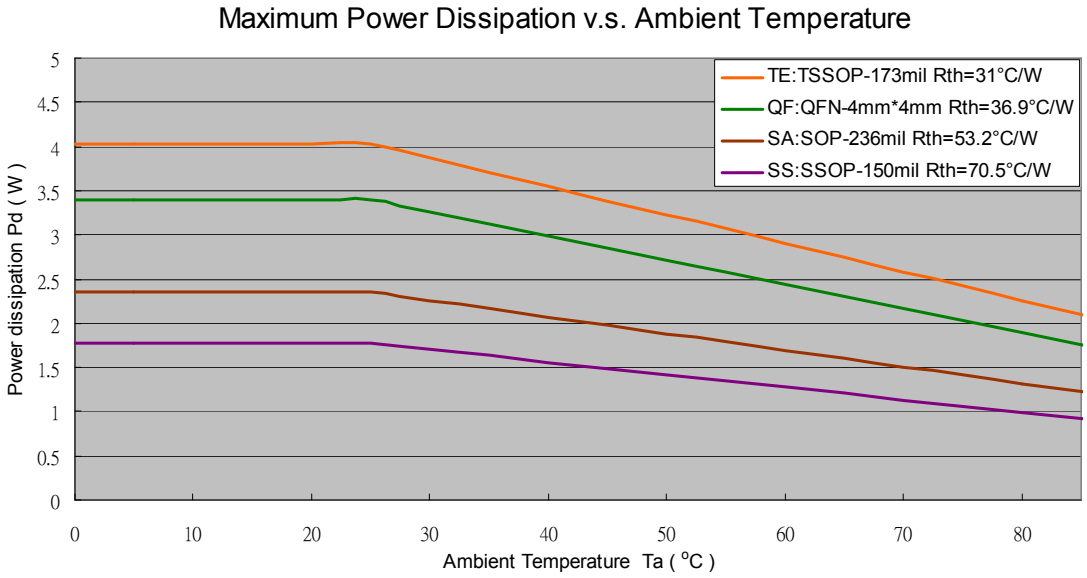
When the 16 output channels are turned on, the practical power dissipation is determined by the following equation:

$$PD\ (practical) = V_{DD} \times I_{DD} + Vout_{(0)} \times Iout_{(0)} \times Duty_{(0)} + \cdots + Vout_{(N)} \times Iout_{(N)} \times Duty_{(N)}\ ,\ where\ N=1\ to\ 15$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

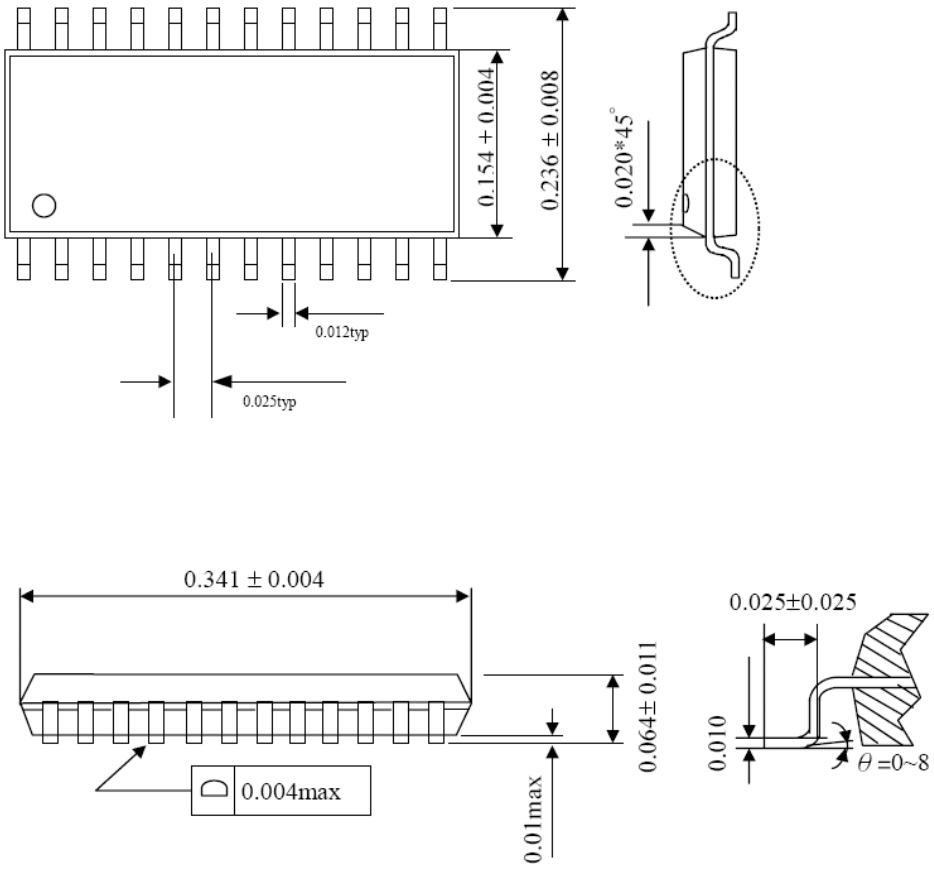
$$PD\ (max) = \frac{Tj(max)(℃) - Ta(℃)}{Rth(j\text{-}a)(℃/Watt)}$$

The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the four different packages.



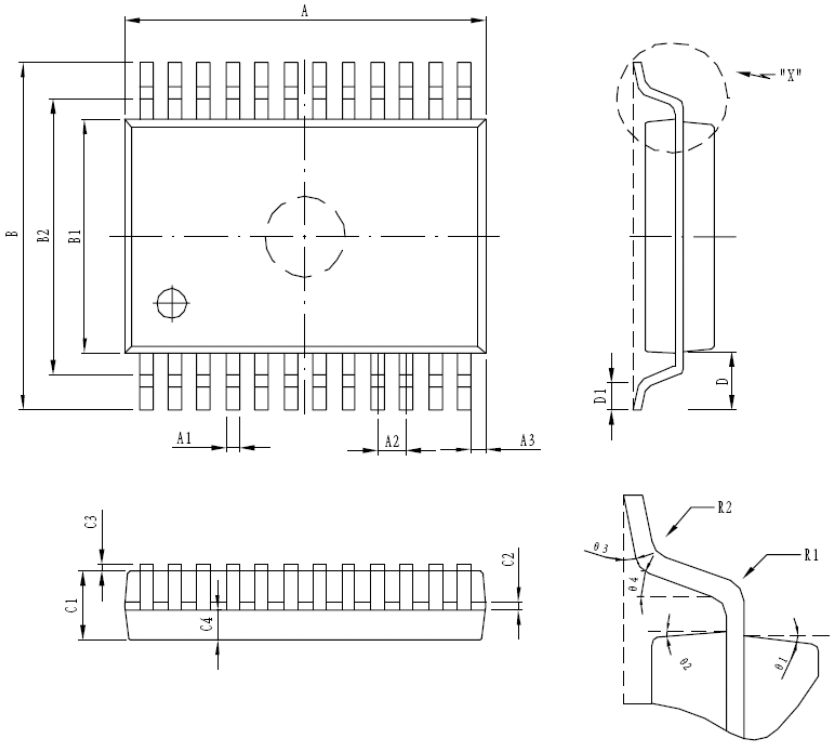
Package Outline Dimension

SSOP-150mil-0.635mm



Package Outline Dimension

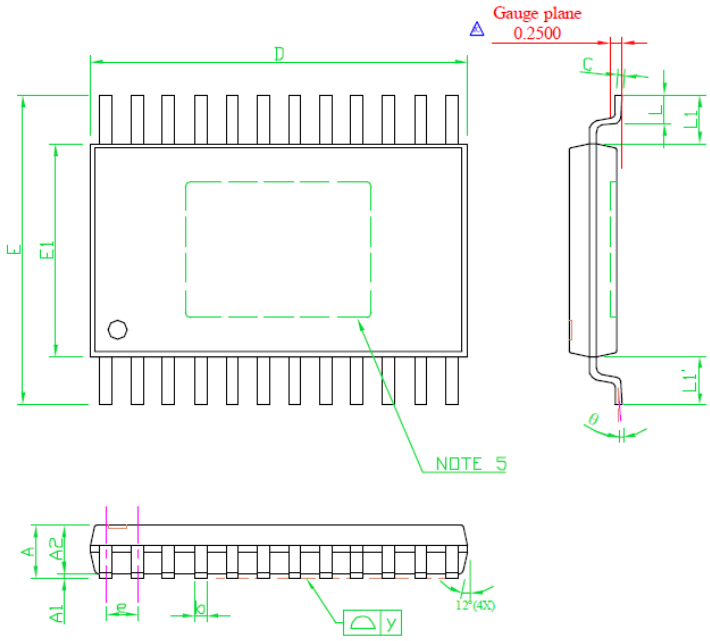
SOP-236mil-1.0mm



SYMBOL	DIMENSION(mm)		SYMBOL	DIMENSION(mm)	
	MIN.	MAX.		MIN.	MAX.
A	12.9	13.1	**C3**	0.05	0.2
A1	0.30	0.50	**C4**	0.80TYP	
A2	1.00TYP		**D**	0.95TYP	
A3	0.8TYP		**D1**	0.33	0.73
B	7.60	8.20	**R1**	0.2TYP	
B1	5.90	6.10	**R2**	0.2TYP	
B2			**θ1**	8°TYP	
C		2.20	**θ2**	10°TYP	
C1	1.70	1.90	**θ3**	4°TYP	
C2	0.15	0.30	**θ4**	5°TYP	

Package Outline Dimension

TSSOP-173mil-0.65mm

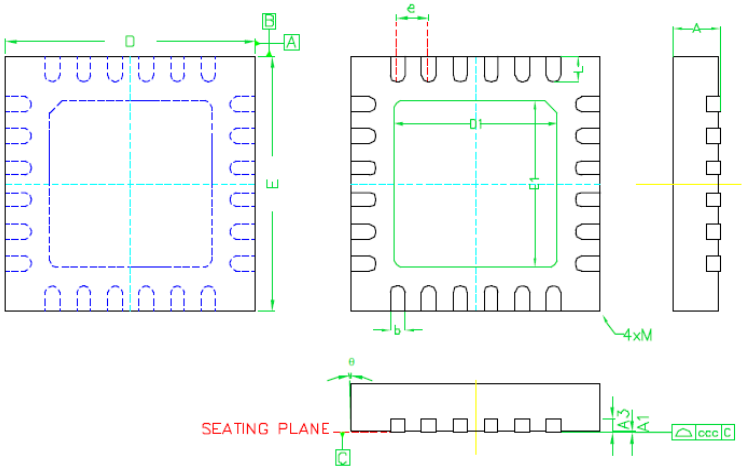


NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE ±0.1 mm UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1 mm
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. DIE PAD EXPOSURE SIZE IS ACCORDING TO LEAD FRAME DESIGN.
6. REFER TO JEDEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	——	1.15	——	——	0.045
A1	0.00	——	0.10	0.000	——	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	——	0.30	0.007	——	0.012
C	0.09	——	0.20	0.004	——	0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	——	0.65	——	——	0.026	——
L	0.45	0.60	0.75	0.018	0.024	0.030
y	——	——	0.10	——	——	0.004
θ	0°	——	8°	0°	——	8°
|L1-L1'|	——	——	0.12	——	——	0.005
L1	1.00REF			0.039REF		

Package Outline Dimension

QFN24-4mm x 4mm



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.010	0.030
A3	----	0.20REF.	----
b	0.18	0.23	0.28
D	3.95	4.00	4.03
D1	----	2.60BSC	----
E	3.95	4.00	4.03
E1	----	2.60BSC	----
e	----	0.50BSC	----
L	0.35	0.40	0.45
θ	-12	----	0
ccc	----	0.08	----
M	----	----	0.05
Burr	0	0.030	0.060

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
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