MY-Semi

Preliminary

MY9268

16-Channel High Accuracy Constant Current LED Driver With 16bits Multiplex-PDM Control for Dynamic Scanning Systems

General Description

The MY9268, 16-channel constant current LED driver with 16bits grayscale M-PDM (Multiplex Pulse Density Modulation) control, supports dynamic 1/2, 1/4, 1/8 scanning applications. The distinctive M-PDM technology enhances the refresh rate of dynamic scanning systems without increasing the frequency of grayscale clock in order to prevent from EMI interference. And the technique of automatic black frame insertion could abate efficiently the influence of blurs caused by the scanning switch.

The device operates over a 3V to 5.5V input voltage range and provides 16 open-drain constant current sinking outputs that are rated to 17V and delivers up to 70mA of high accuracy current to each string of LED. The current at each output is programmable by means of an external current-sensing resistor and could be adjusted by 8bits linear global current control. By this advanced M-PDM approach, the frame refresh rate could be improved up to 16000Hz in dynamic 1/8 scanning systems and 32000Hz in dynamic 1/4 scanning systems when the grayscale clock is 16MHz.

The MY9268's on-board pass elements minimize the need for external components, while at the same time, providing ±1.5% LED current accuracy. Additional features include a ±0.1% regulated output current capability and 30ns fast output transient response.

The MY9268 is available in a 24-pin SOP/SSOP/TSSOP /QFN package and specified over the -40°C to +85°C ambient temperature range.

Features

- 3.3V ~ 5V Operating supply voltage
- 3~70mA/5V Constant current output range
- 3~50mA/3.3V Constant current output range
- 17V Rated output channels for long LED strings
- ±1.5% (typ.) LED Current accuracy between channels
- ±3% (typ.) LED Current accuracy between chips
- ±0.1% Output current regulation capability
- Build-in 4K bits SRAM
- For dynamic 1/2, 1/4, 1/8 scanning systems
- 16bits grayscale resolution with Multiplex Pulse Density Modulation [patent pending]
- Supports diverse applications of 8bits~16bits grayscale resolution
- Refresh rate up to 32000Hz in 1/4 scanning systems
  Refresh rate up to 16000Hz in 1/8 scanning systems
- EMI reduction grayscale clock
- Automatic black frame insertion
- Ghost image abatement
- 8bits linear global current control
- 30MHz Clock frequency for data transfer
- 30ns fast current transient response
- Current setting by one external resister
- Schmitt trigger input
- Power on reset
- -40°C to +85°C Ambient temperature range

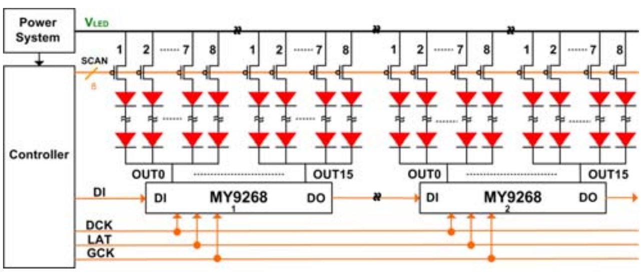
Applications

- Indoor and Outdoor LED Video Displays
- Variable Message Sign (VMS)
- Dot Matrix Module
- LCD Display Backlighting

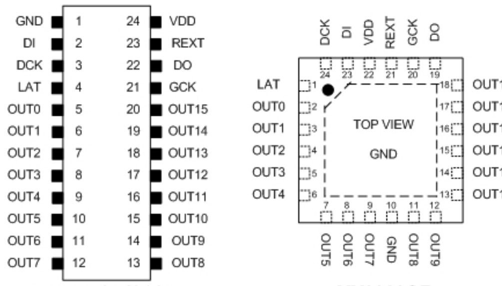
Order information

Part	Package Information	
MY9268SA	SOP24-236mil-1.0mm	2000 pcs/Reel
MY9268SS	SSOP24-150mil-0.635mm	2500 pcs/Reel
MY9268TE	TSSOP24-173mil-0.65mm (Exposed Pad)	2500 pcs/Reel
MY9268QF	QFN24-4mmx4mm-0.5mm	3000 pcs/Reel

Typical Operating Circuits

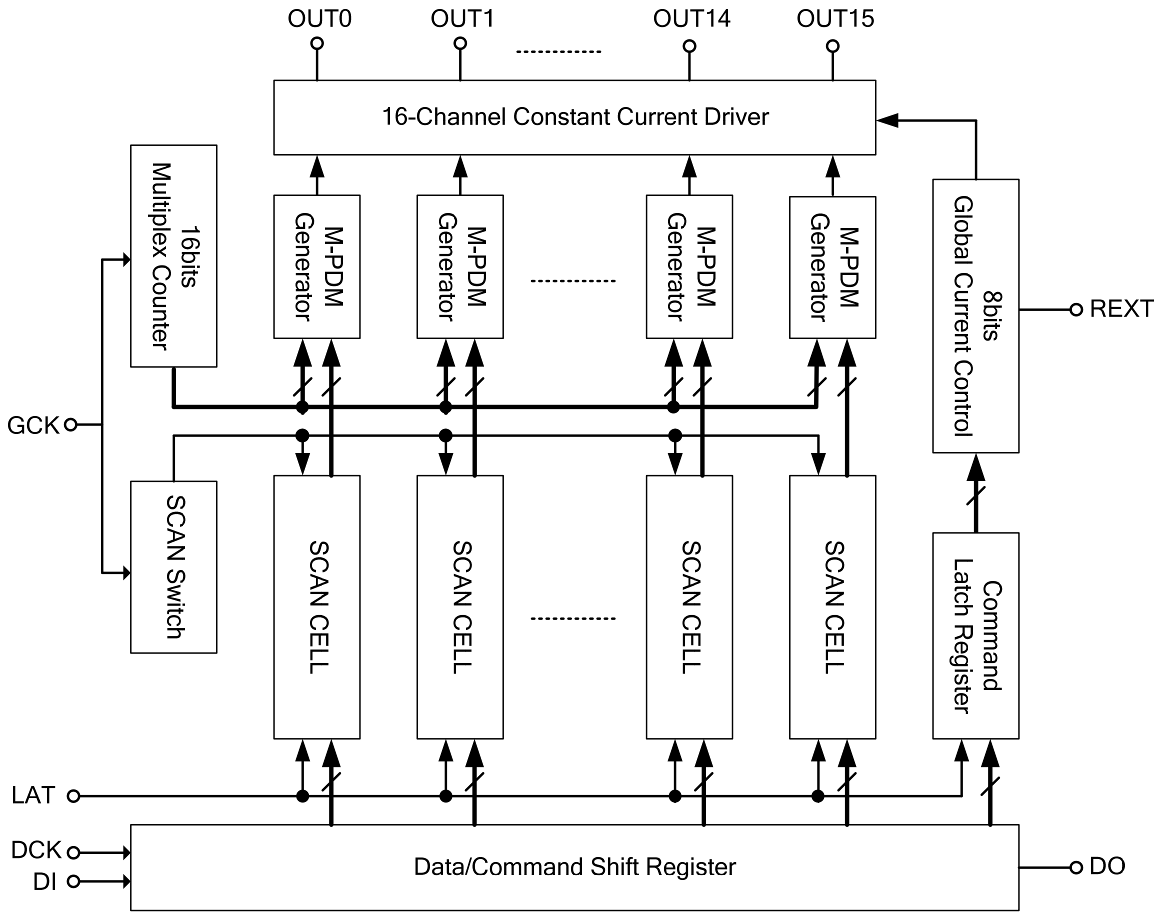


Pin Configuration



MY9268SA/SS/TE   MY9268QF

Block Diagram

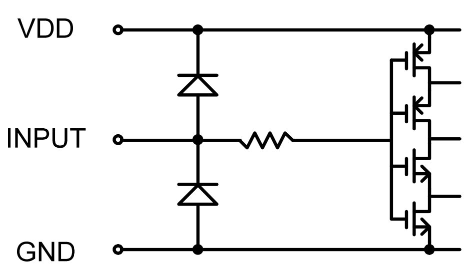


Pin Description

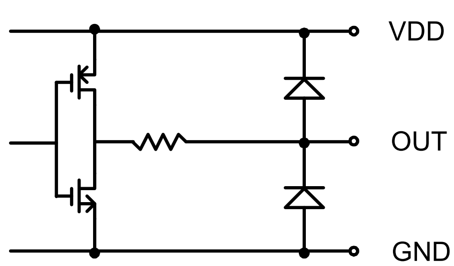
PIN No.		PIN NAME	FUNCTION
SOP/SSOP	QFN		
1	10	GND	Ground terminal.
2	23	DI	Serial data input terminal.
3	24	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
4	1	LAT	Input terminal of data strobe and SCAN mode setting. Combine DCK with LAT to execute the frame latch and define the initial position of SCAN mode
5~20	2~9, 11~18	OUT0~15	Sink constant-current outputs (open-drain).
21	20	GCK	External grayscale clock input for PDM operations and black frame insertion
22	19	DO	Serial data output terminal.
23	21	REXT	External resistors connected between REXT and GND for output current value setting.
24	22	VDD	Supply voltage terminal. A capacitor ranging from 4.7uF to 10uF must be connected between VDD and VSS pin of each chip.

Equivalent Circuit of Inputs and Output

1. DCK, DI, LAT, GCK terminals



2. DO terminal



Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	80	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	25	MHz
GND Terminal Current	IGND	1280	mA
Thermal Resistance (On PCB)	Rth(j-a)	31 (TE:TSSOP-173mil-0.65mm)	°C/W
		53.2 (SA:SOP-236mil-1.0mm)	
		70.5 (SS:SSOP-150mil-0.635mm)	
		36.9 (QF:QFN24-4mmx4mm)	
Operating Supply Voltage	VDD	3.0 ~ 5.5	V
Operating Ambient Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.
(2) All voltage values are with respect to ground terminal.

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage “H” Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage “L” Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel)*1	dIOUT1	VOUT = 1.0 V Rrext = 720 Ω	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT2		—	±3	±6	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 6 KΩ	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4		—	±3	±6	%
Output Voltage Regulation*3	% / VOUT	Rrext = 720 Ω VOUT = 1 V ~ 3 V	—	—	±.0.1	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 720 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current*5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	1.7	2.5	mA
	$I_{DD2(off)}$	input signal is static Rrext = 6 KΩ all outputs turn off	—	2.3	3.1	
	$I_{DD1(on)}$	input signal is static Rrext = 6 KΩ all outputs turn on	—	2.4	3.2	
	$I_{DD3(off)}$	input signal is static Rrext = 720 Ω all outputs turn off	—	6.0	6.5	
	$I_{DD2(on)}$	input signal is static Rrext = 720 Ω all outputs turn on	—	6.1	6.6	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16} - (Ideal\ Output\ Current)}{(Ideal\ Output\ Current)} \right) \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

*5 IO excluded.

Electrical Characteristics (VDD = 3.3 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage “H” Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage “L” Level	VIL	CMOS logic level	GND	—	0.3VDD	V
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	V
Output Current Skew (Channel-to-Channel)*1	dIOUT1	VOUT = 1.0 V Rrext = 720 Ω	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT2	VOUT = 1.0 V Rrext = 720 Ω	—	±3	±6	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 6 KΩ	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4	VOUT = 1.0 V Rrext = 6 KΩ		±3	±6	%
Output Voltage Regulation*3	% / VOUT	Rrext = 720 Ω VOUT = 1 V ~ 3 V	—	—	±0.1	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 720 Ω VDD = 3 V ~ 5.5 V	—	±0.7	±1	% / V
Supply Current*5	IDD1(off)	all pins are open unless VDD and GND	—	1.2	2.0	mA
	IDD2(off)	input signal is static Rrext = 6 KΩ all outputs turn off	—	2.1	2.8	mA
	IDD1(on)	input signal is static Rrext = 6 KΩ all outputs turn on	—	2.1	2.9	mA
	IDD3(off)	input signal is static Rrext = 720 Ω all outputs turn off	—	5.8	6.5	mA
	IDD2(on)	input signal is static Rrext = 720 Ω all outputs turn on	—	5.8	6.5	mA

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16} - (Ideal\ Output\ Current)}{(Ideal\ Output\ Current)} \right) \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

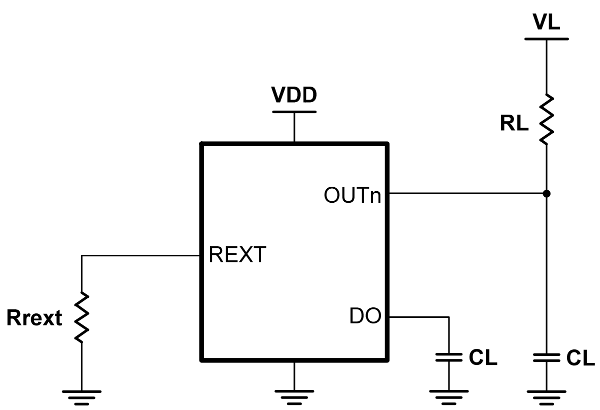
*5 IO excluded.

Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L to ‘H’)	GCK-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 720 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	25	45	ns
	LAT-to-OUT0	tpLH2		—	25	45	
	DCK-DO	tpLH3		—	24	44	
Propagation Delay (‘H’ to ‘L’)	GCK-to-OUT0	tpHL1		—	20	40	
	LAT-to-OUT0	tpHL2		—	20	40	
	DCK-DO	tpHL3		—	28	48	
Pulse Duration	LAT	$tw_{(LAT)}$		50			
	GCK	$tw_{(GCK)}$		30			
	DCK	$tw_{(DCK)}$		20			
Setup Time	LAT	$tsu_{(LAT)}$		5			
	DI	$tsu_{(D)}$		3			
Hold Time	LAT	$th_{(LAT)}$		20			
	DI	$th_{(D)}$		4			
Hold Time of Instruction		$th_{(CM)}$		20			
DO Rise Time		$tr_{(DO)}$			16		
DO Fall Time		$tf_{(DO)}$			18		
Output Current Rise Time		tor		—	15	—	
Output Current Fall Time		tof		—	18	—	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+8)}$)		tod		—	16	—	
Data Clock Frequency		F_{DCK}				30	MHz
Grayscale Clock Frequency		F_{GCK}				16	

Switching Characteristics (VDD = 3.3V, Ta = 25°C unless otherwise noted)

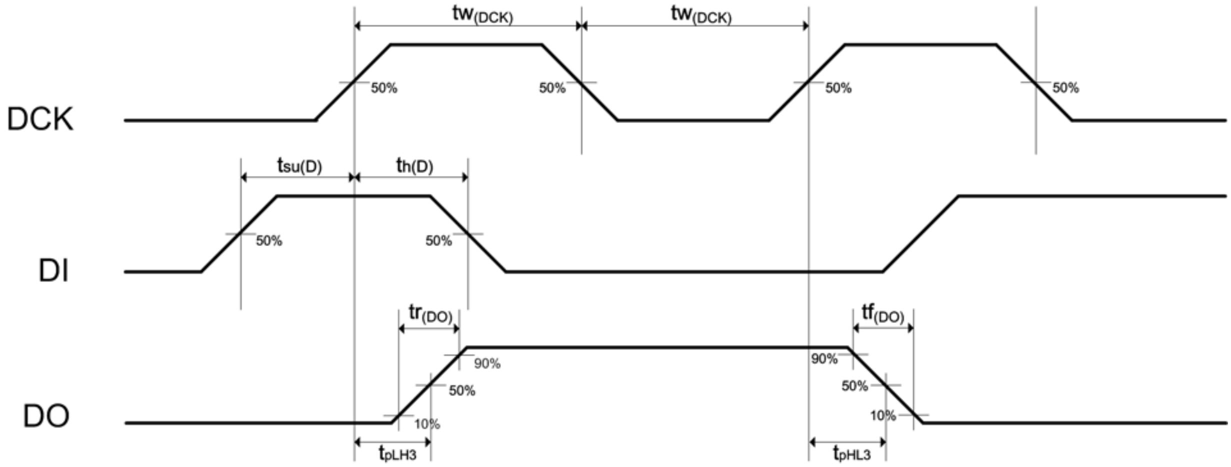
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	GCK-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 720 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	47	67	ns
	LAT-to-OUT0	tpLH2		—	48	68	
	DCK-to-DO	tpLH3		—	30	50	
Propagation Delay ('H' to 'L')	GCK-to-OUT0	tpHL1		—	30	50	
	LAT-to-OUT0	tpHL2		—	30	50	
	DCK-DO	tpHL3		—	30	50	
Pulse Duration	LAT	$tw_{(LAT)}$		50			
	GCK	$tw_{(GCK)}$		30			
	DCK	$tw_{(DCK)}$		20			
Setup Time	LAT	$tsu_{(LAT)}$		5			
	DI	$tsu_{(D)}$		3			
Hold Time	LAT	$th_{(LAT)}$		20			
	DI	$th_{(D)}$		4			
Hold Time of Instruction		$th_{(CM)}$		20			
DO Rise Time		$tr_{(DO)}$			24		
DO Fall Time		$tf_{(DO)}$			23.5		
Output Current Rise Time		tor		—	24.5	—	
Output Current Fall Time		tof		—	23.5	—	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+8)}$)		tod		—	26	—	
Data Clock Frequency		F_{DCK}				25	MHz
Grayscale Clock Frequency		F_{GCK}				16	



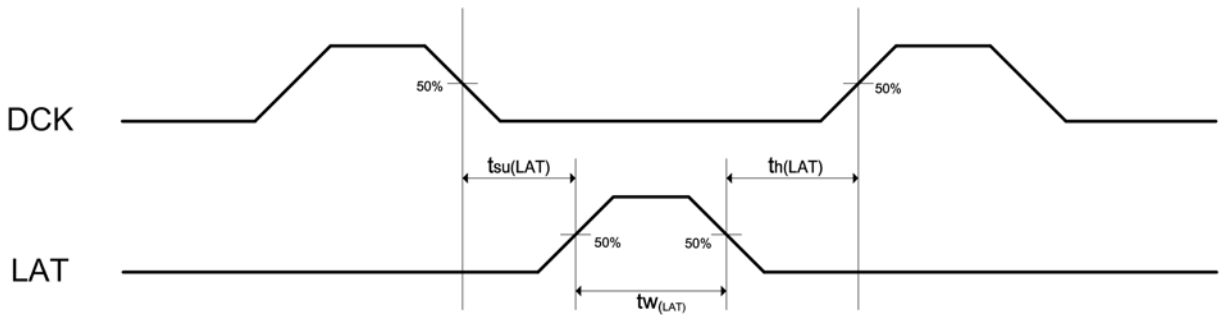
Switching Characteristics Test Circuit

Timing Diagram

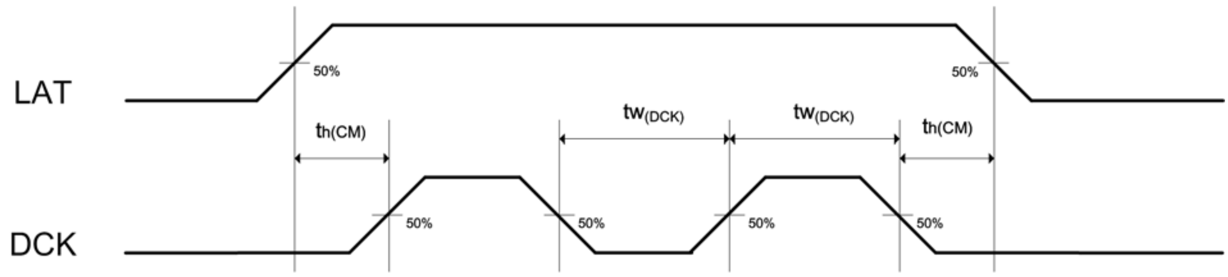
1. DCK-DI, DO



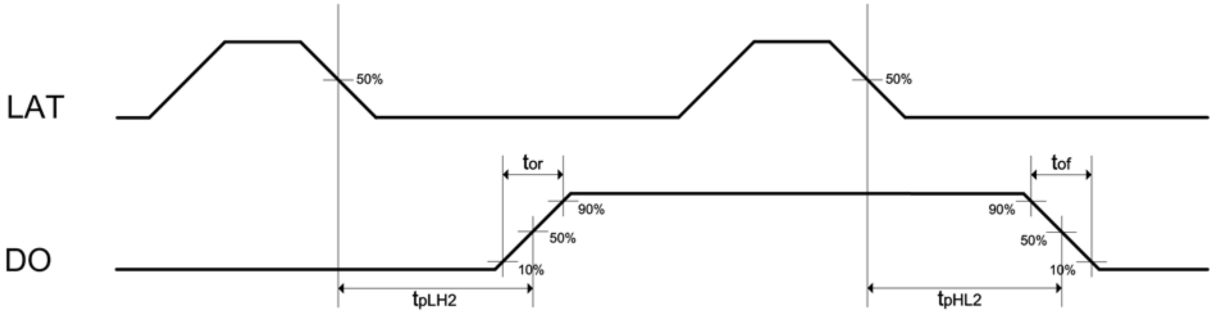
2. DCK-LAT



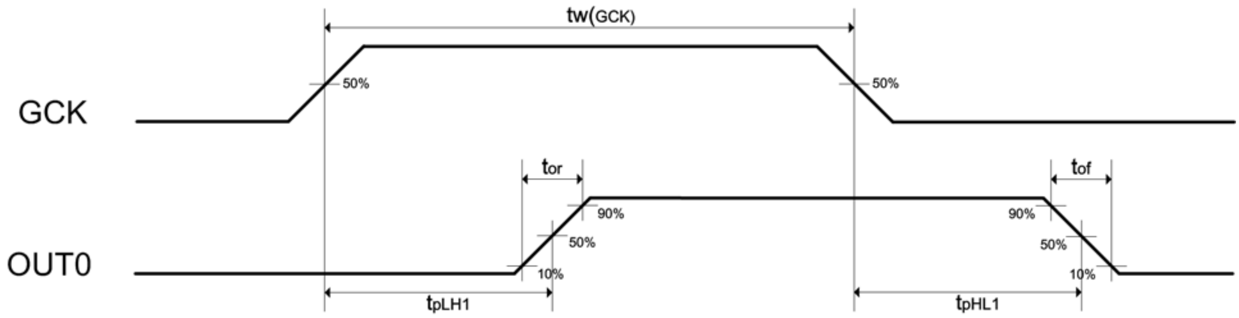
3. LAT-DCK (Instruction)



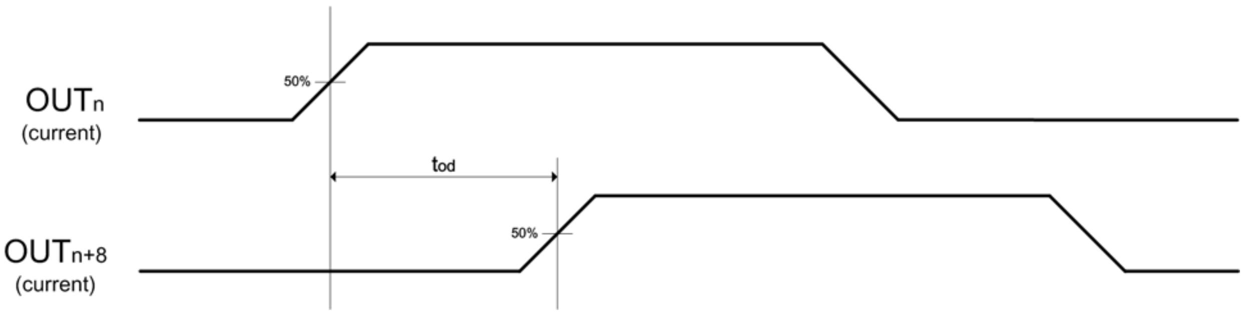
4. LAT-OUT0



5. GCK-OUT0



6. OUT_n-OUT_{n+8}



Fast Transient Response

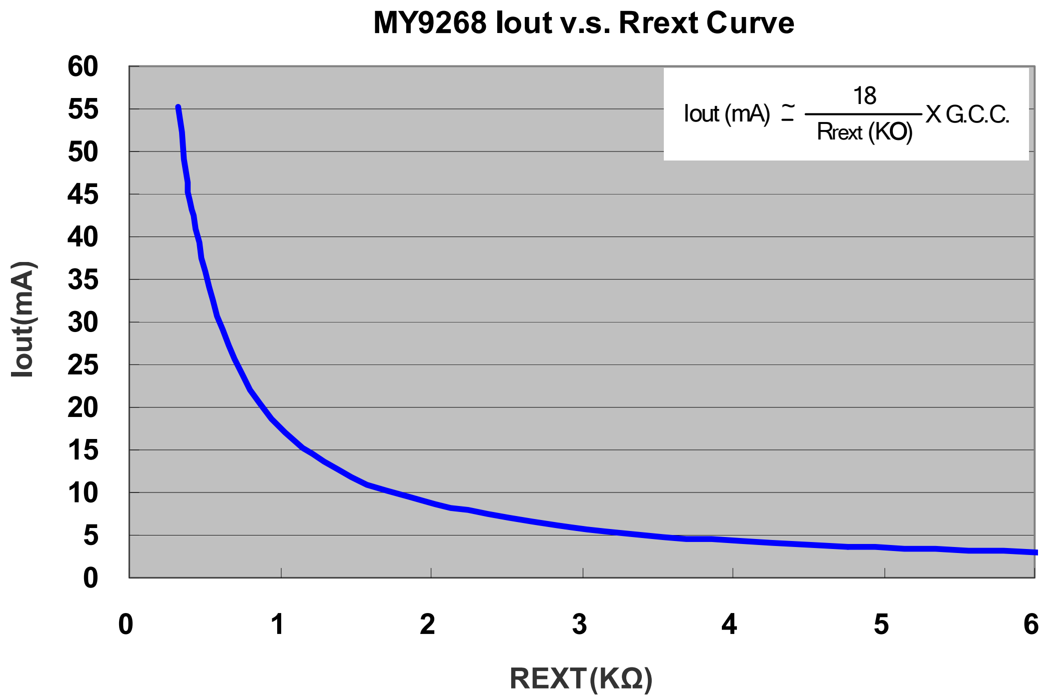
The MY9268 supports the fast transient response to make high image resolution possible. The GCK pulse width of 30ns is guaranteed to get a complete Vout waveform.

Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

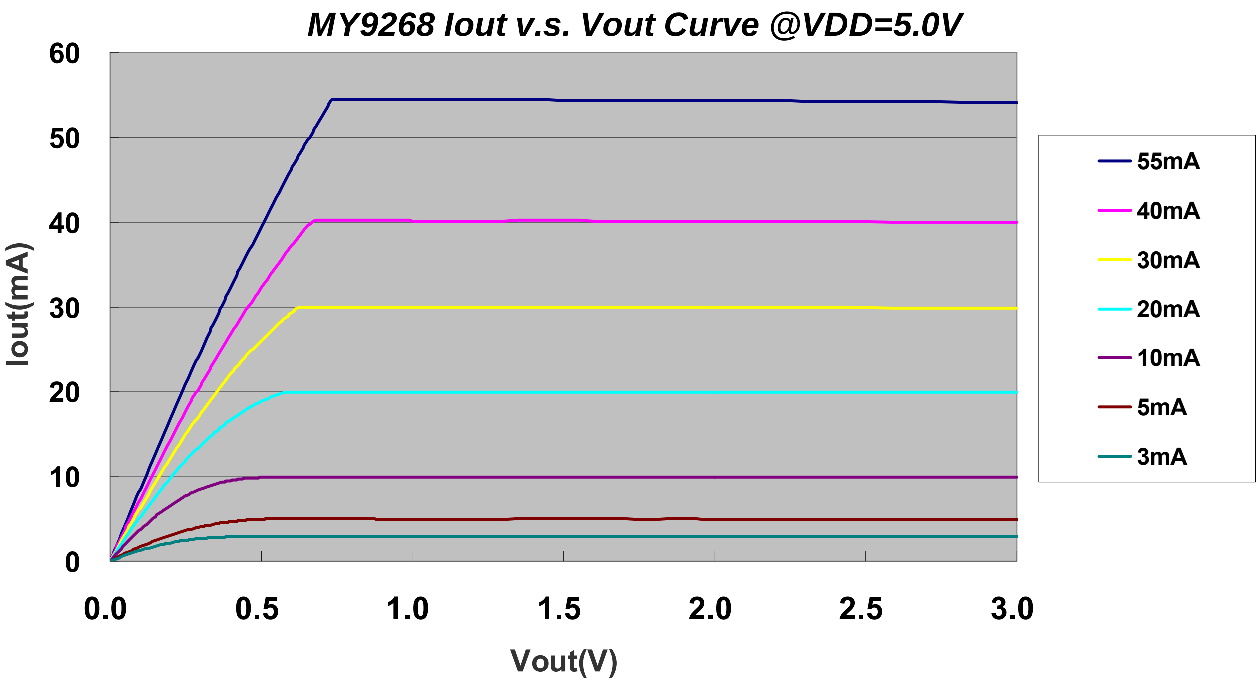
$$Iout(mA) \;=\; \frac{18}{Rrext \quad (K\Omega)} \times G.C.C.$$

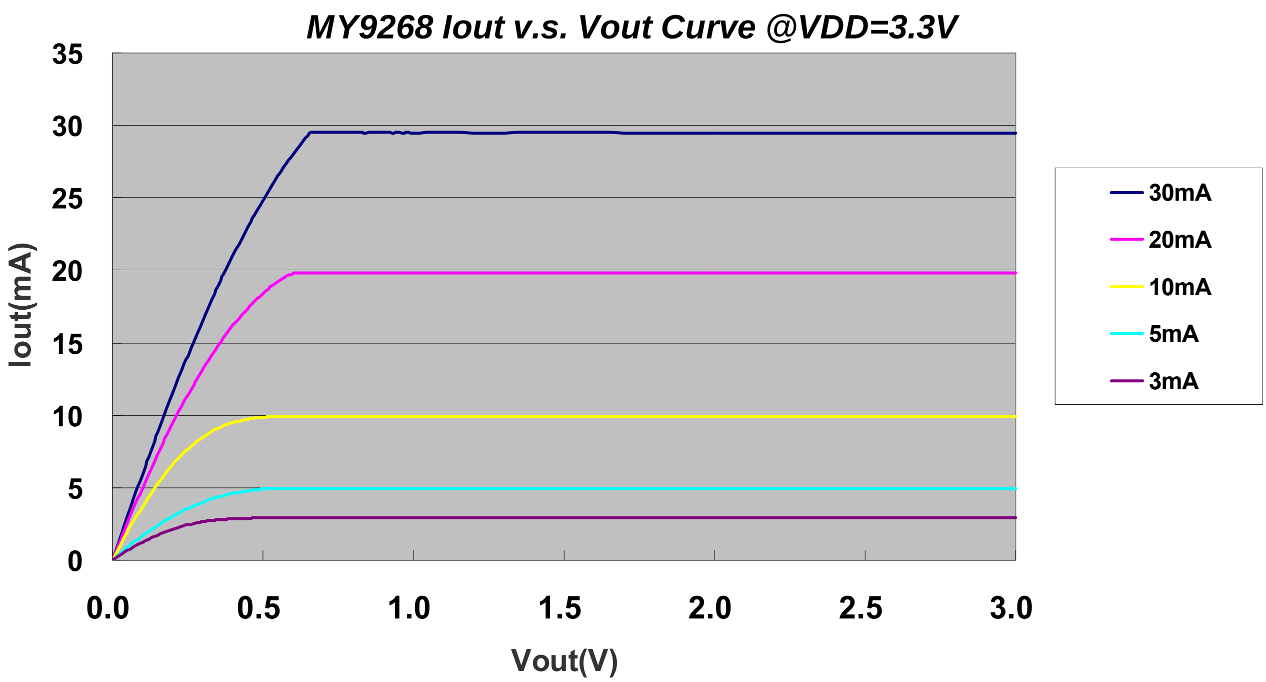
Where Rrext is a resistor placed between REXT and GND
And G.C.C. is the factor of global current control refer to page14
For example, Iout is 25mA when Rrext=720Ω and Iout is 3mA when Rrext=6KΩ



Constant-Current Output

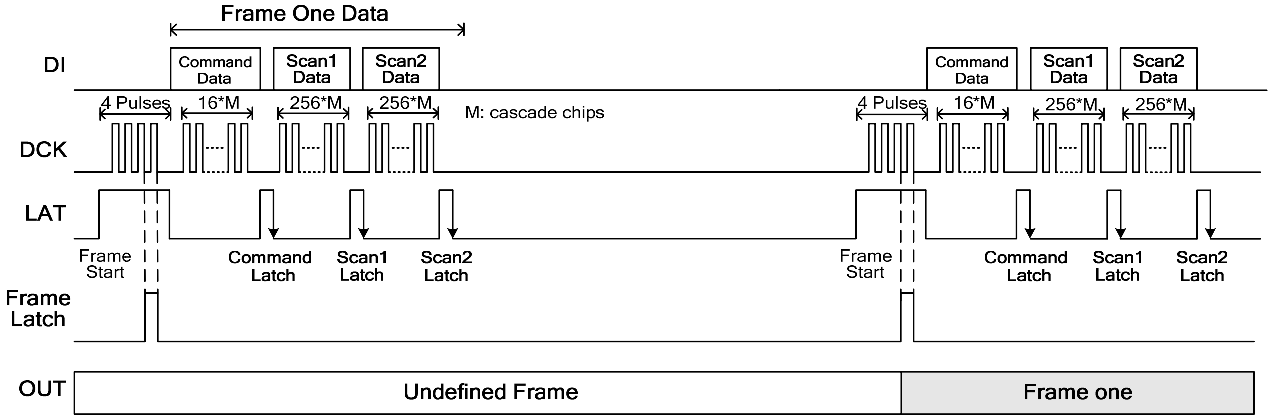
The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the MY9268 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.





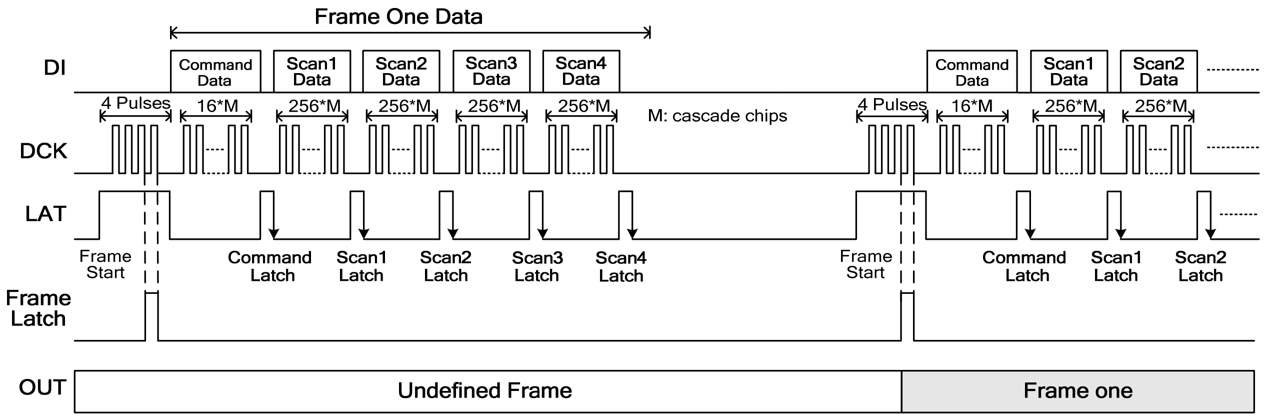
Data Transmitting Protocol

Dynamic 1/2 Scanning Applications (CMD[11:10]=2'b01)



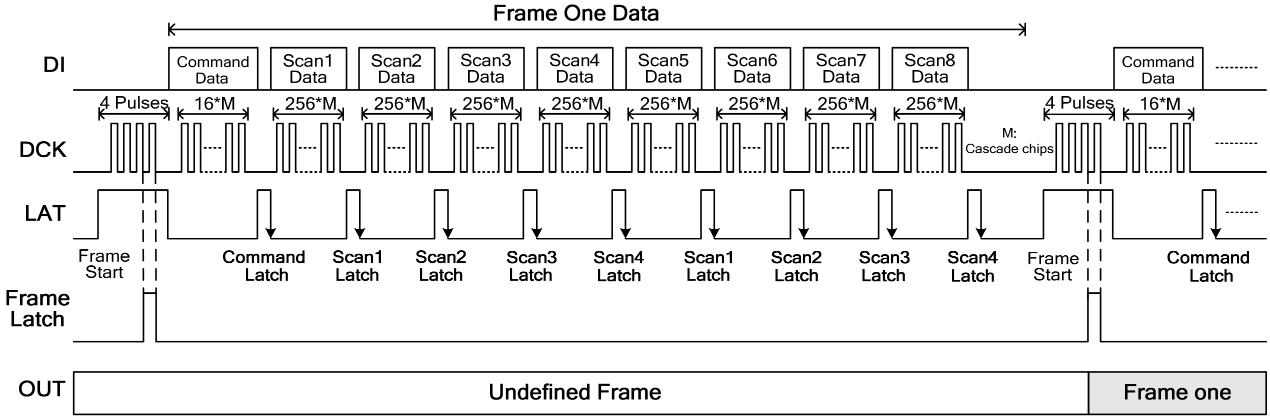
This data transmitting process starts from an initial instruction which is comprised of 4 DCK pulses in high level of LAT signal. This initial instruction would define the start of data transmission and an image frame. Furthermore, it would reset simultaneously the internal grayscale counter in order to synchronize each frame. The first LAT signal after the initial instruction is a command latch which would latch 16bits command data into each device. And the following two LAT signals are ordered from Scan1 latch to Scan2 latch. These Scan latches would latch separately the scanning data into the assigned registers. Finally, the controller must transmit an initial instruction to start this frame.

Dynamic 1/4 Scanning Applications (CMD[11:10]=2'b10)



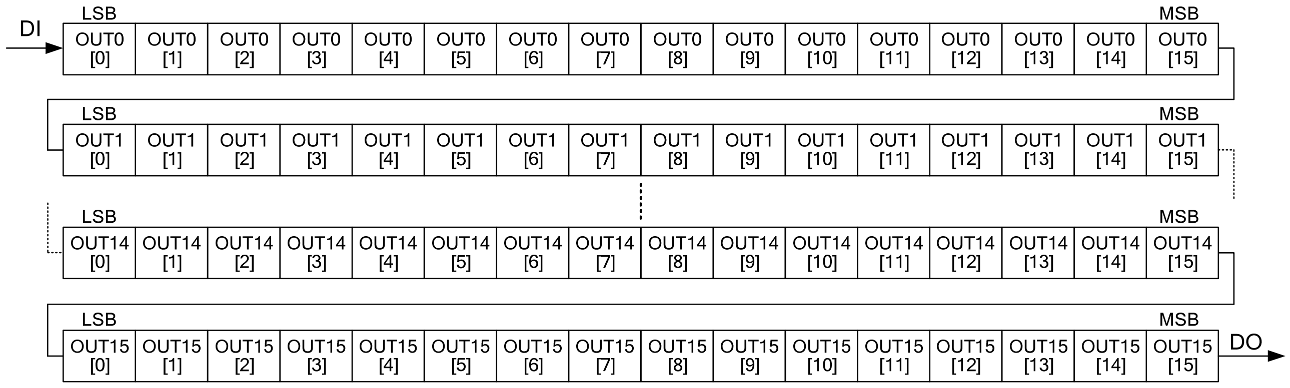
This data transmitting process starts from an initial instruction which is comprised of 4 DCK pulses in high level of LAT signal. This initial instruction would define the start of data transmission and an image frame. Furthermore, it would reset simultaneously the internal grayscale counter in order to synchronize each frame. The first LAT signal after the initial instruction is a command latch which would latch 16bits command data into each device. And the following four LAT signals are ordered from Scan1 latch to Scan4 latch. These Scan latches would latch separately the scanning data into the assigned registers. Finally, the controller must transmit an initial instruction to start this frame.

Dynamic 1/8 Scanning Applications (CMD[11:10]=2'b11)



This data transmitting process starts from an initial instruction which is comprised of 4 DCK pulses in high level of LAT signal. This initial instruction would define the start of data transmission and an image frame. Furthermore, it would reset simultaneously the internal grayscale counter in order to synchronize each frame. The first LAT signal after the initial instruction is a command latch which would latch 16bits command data into each device. And the following eight LAT signals are ordered from Scan1 latch to Scan8 latch. These Scan latches would latch separately the scanning data into the assigned registers. Finally, the controller must transmit an initial instruction to start this frame.

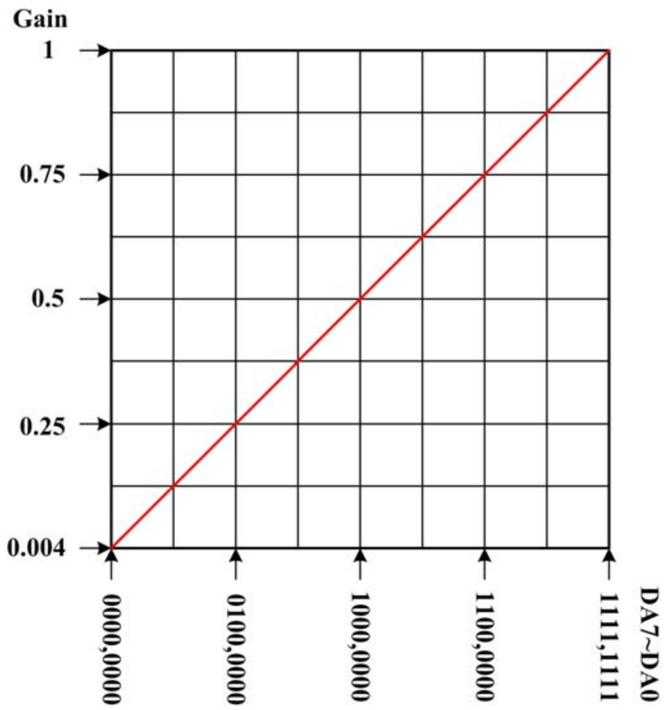
Image Data Format



16x16-bits M-PDM data are transmitted into a device for each scan according to the format illustrated above. The first input bit is the most significant bit of OUT15.

Global Current Control (set CMD[7:0])

MY9268 provides the global current control function, users can use 8-bits command data CMD[7:0] to adjust the output current. The following formula is utilized to calculate the current value:



Iout(mA) = 18 X G.C.C. / Rrext (KΩ)

Where:

$$G.C.C. = (CMD[7]x2^7+CMD[6]x2^6+CMD[5]x2^5+CMD[4]x2^4+CMD[3]x2^3+CMD[2]x2^2+CMD[1]x2^1+CMD[0]x2^0+1) / 256$$

The range of G.C.C is from 1/256 to 256/256 by 256-step linearly.

Command Data Format

DI

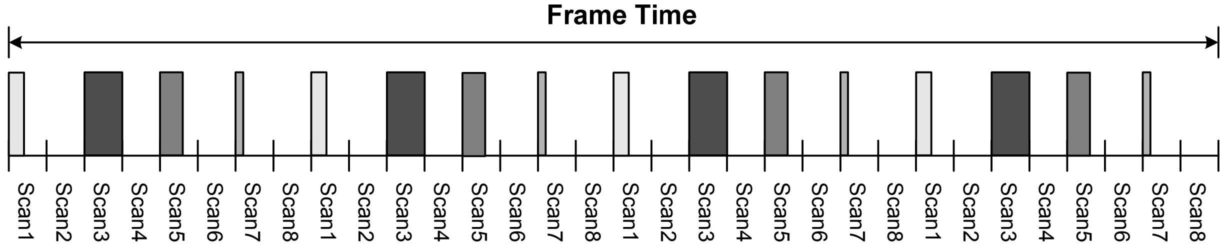
CMD[0]	CMD[1]	CMD[2]	CMD[3]	CMD[4]	CMD[5]	CMD[6]	CMD[7]
DA[0]	DA[1]	DA[2]	DA[3]	DA[4]	DA[5]	DA[6]	DA[7]

CMD[8]	CMD[9]	CMD[10]	CMD[11]	CMD[12]	CMD[13]	CMD[14]	CMD[15]
Refresh Rate	Ghost Abatement	Scan<0>	Scan<1>	Reserved	Reserved	Reserved	Reserved (first input bit)

DO

CMD Bit	Initial Value	Value	Function	Description
CMD[15:12]	4'b0000	4'b0000	Reserved	Reserved bits
CMD[11:10]	2'b00	2'b00	Reserved	Set the scanning mode CMD[11:10]=2'b01 => 1/2 scanning mode (one channel supports 2 strings of LEDs) CMD[11:10]=2'b10 => 1/4 scanning mode (one channel supports 4 strings of LEDs) CMD[11:10]=2'b11 => 1/8 scanning mode (one channel supports 8 strings of LEDs)
		2'b01	Dynamic 1/2 scan (N=2)	
		2'b10	Dynamic 1/4 scan (N=4)	
		2'b11	Dynamic 1/8 scan (N=8)	
CMD[9]	1'b0	1'b0	Ghost image abatement	Output ports pull to VDD when they are turned off for ghost image abatement when CMD[9]=1'b0 => disable when CMD[9]=1'b1 => enable
		1'b1		
CMD[8]	1'b0	1'b0	Low refresh rate (64 segments)	Set the refresh rate of scanning systems when CMD[8]=1'b0, Refresh rate ≒ 64 / (32768*T_{GCK}*N) when CMD[8]=1'b1, Refresh rate ≒ 256 / (32768*T_{GCK}*N) ** N is the parameter of scan mode **
		1'b1	High refresh rate (256 segments)	
CMD[7:0]	8'b00000000	8'b00000000~ 8'b11111111	G.C.C	8bit DA data for global current control (allow 256-step programmable current gain)

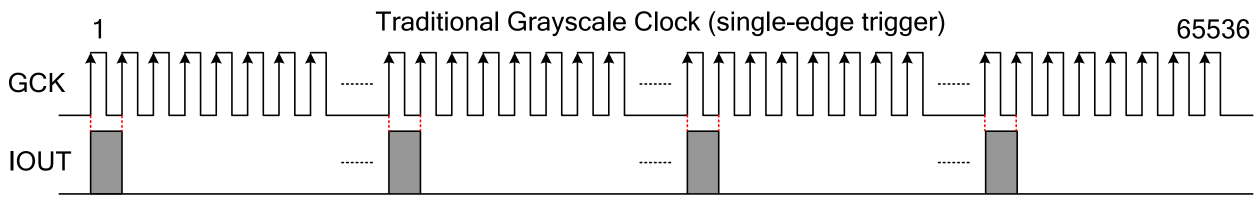
Multiplex Pulse Density Modulation (Multiplex-PDM)

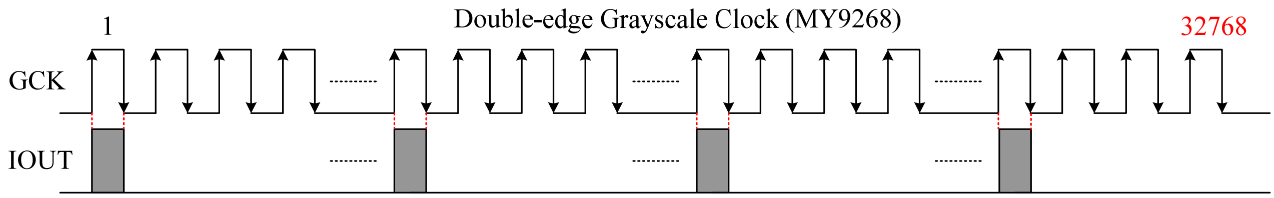


For example,
Scan1=2/5, Scan2=0, Scan3=1, Scan4=0, Scan5=3/5, Scan6=0, Scan7=1/5, Scan8=0

The advanced Multiplex-PDM approach divides the frame time into the designated segments and interlaces Scan images to enhance the refresh rate. By this technique, the frame refresh rate could be improved efficiently by 64 times or 256 times without increasing the frequency of grayscale clock in order to prevent from EMI interference.

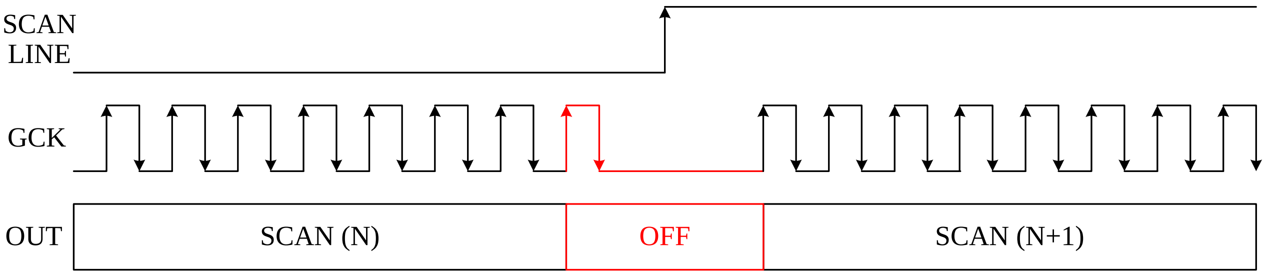
Double-edge Grayscale Clock





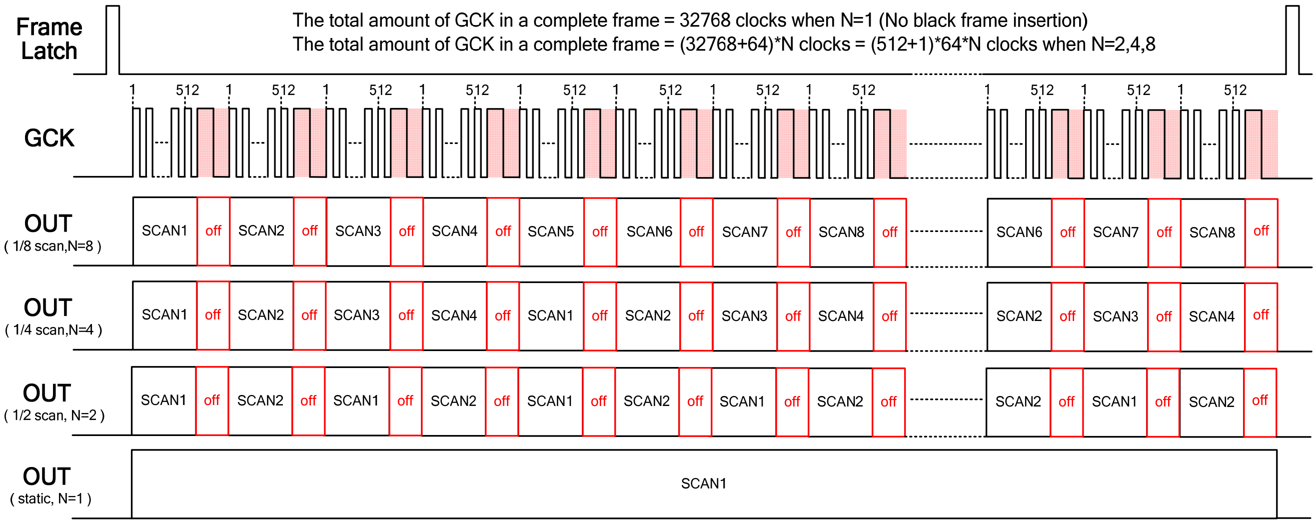
A whole period of 16bits resolution must be composed by 65536 traditional grayscale clocks because constant current outputs only are triggered at the rising edge of clocks. Therefore, a controller has to transmit fast grayscale clocks in order to accomplish high refresh rate when users adopt traditional PWM chips. MY9268 supports a specific mode of double-edge grayscale clocks which trigger both at rising and falling edges of clocks. By this approach, a whole period of 16bits resolution is composed by only 32768 double-edge grayscale clocks and the electromagnetic interference would be decreased substantially due to slow grayscale clocks.

Automatic Black Frame Insertion



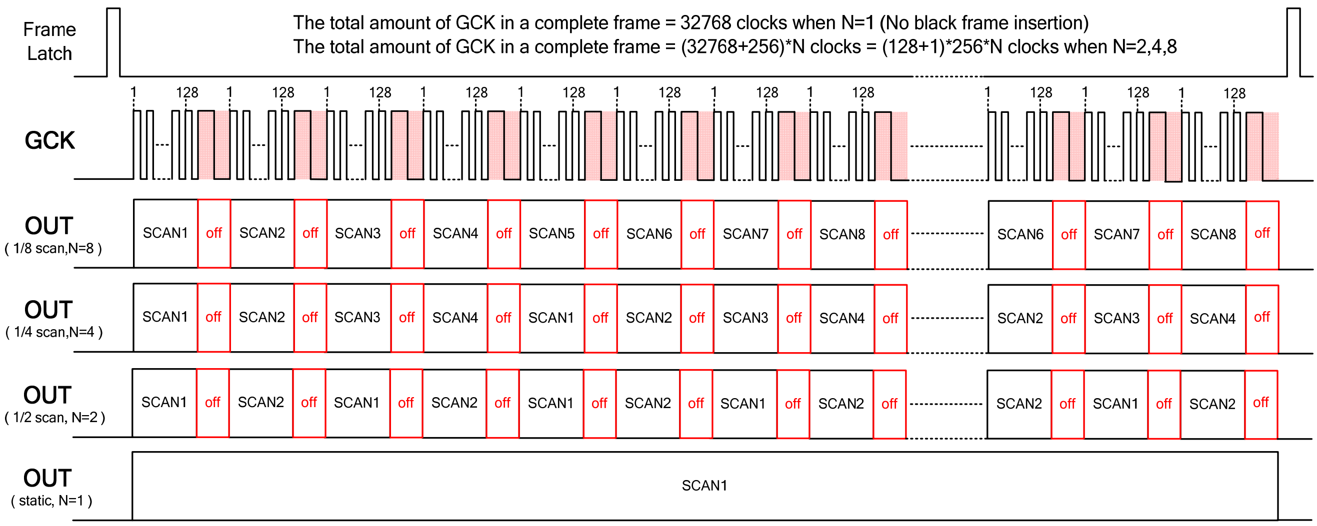
In the process of scan switching, constant current outputs have to be turned off in order to avoid that LEDs of the preceding and the present scanning lines are turned on simultaneously. MY9268 supports a specific technique of automatic black frame insertion to solve this problem by a double-edge grayscale clock. All constant current outputs are turned off during this double-edge grayscale clock.

Low Refresh Rate Frame (set CMD[8]=1’b0)



When the mode of low refresh rate is assigned, MY9268 would divide equally 32768 double-edge grayscale clocks of one frame into 64 groups. Therefore, each segment of M-PDM waveform is comprised of 512 double-edge grayscale clocks. This advanced M-PDM approach enhances the refresh rate by 64 times in comparison with a traditional one. Meanwhile, the distinctive technique of automatic black frame insertion would produce a black frame between two M-PDM segments by one double-edge grayscale clocks in order to abate the interference of blurs. Users could modify the period of double-edge grayscale clocks to set the black frame time according to the switch time of external scan MOS. The total amount of grayscale clocks in a complete frame is (32768+64)*N clocks in a scanning system which N=2,4,8.

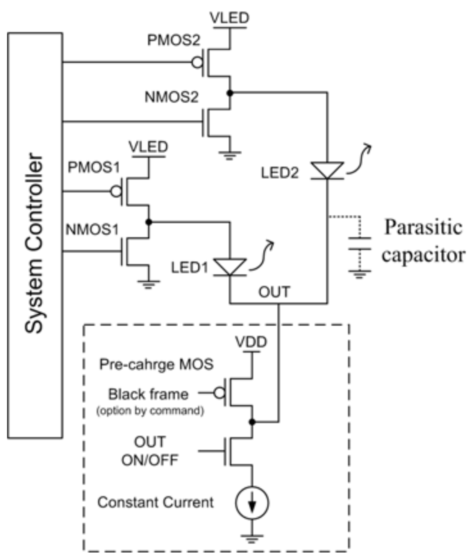
High Refresh Rate Frame (set CMD[8]=1'b1)



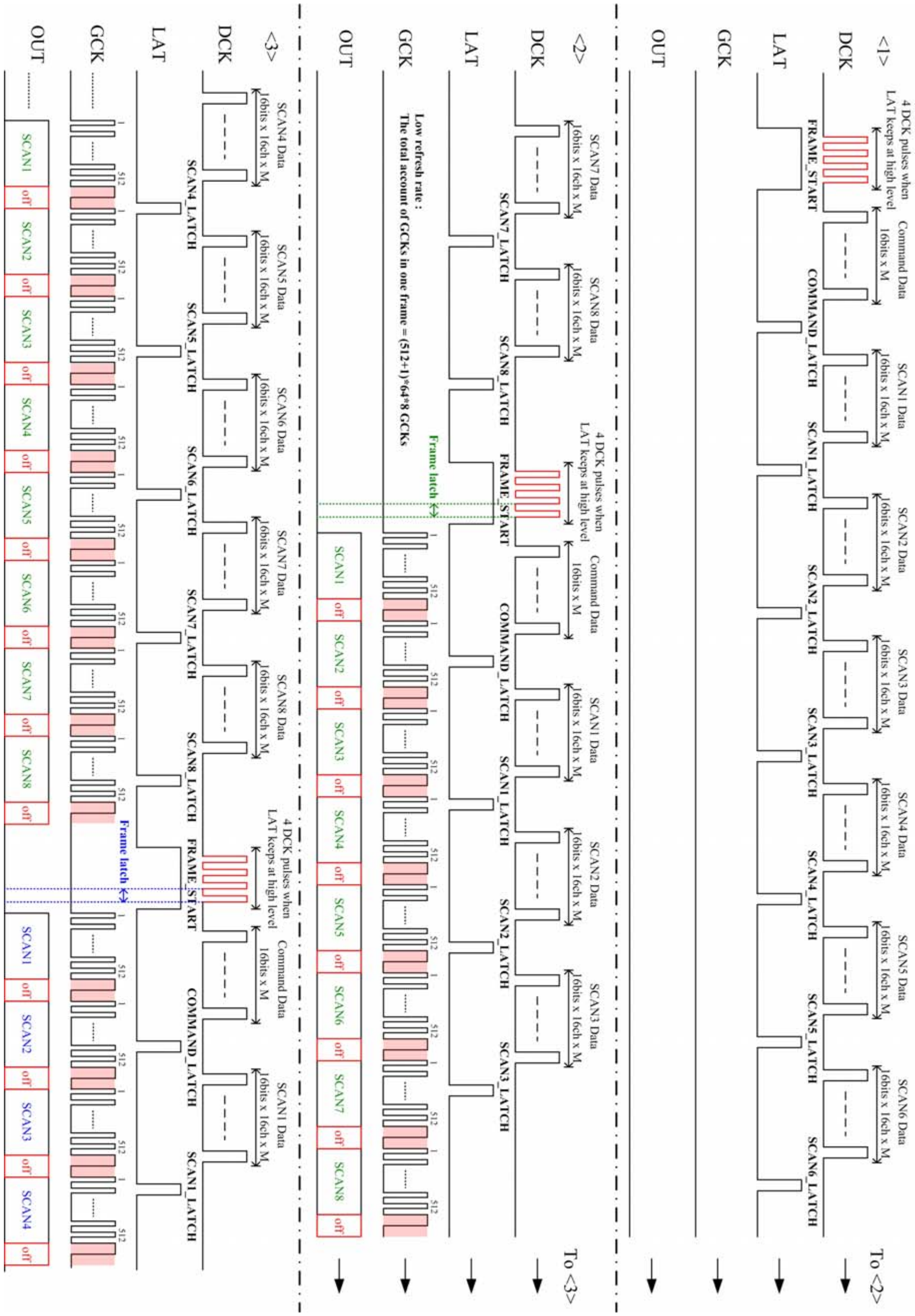
When the mode of high refresh rate is assigned, MY9268 would divide equally 32768 double-edge grayscale clocks of one frame into 256 groups. Therefore, each segment of M-PDM waveform is comprised of 128 double-edge grayscale clocks. This advanced M-PDM approach enhances the refresh rate by 256 times in comparison with a traditional one. Meanwhile, the distinctive technique of automatic black frame insertion would produce a black frame between two M-PDM segments by one double-edge grayscale clocks in order to abate the interference of blurs. Users could modify the period of double-edge grayscale clocks to set the black frame time according to the switch time of external scan MOS. The total amount of grayscale clocks in a complete frame is (32768+256)*N clocks in a scanning system which N=2,4,8.

Ghost Image Abatement (set CMD[9])

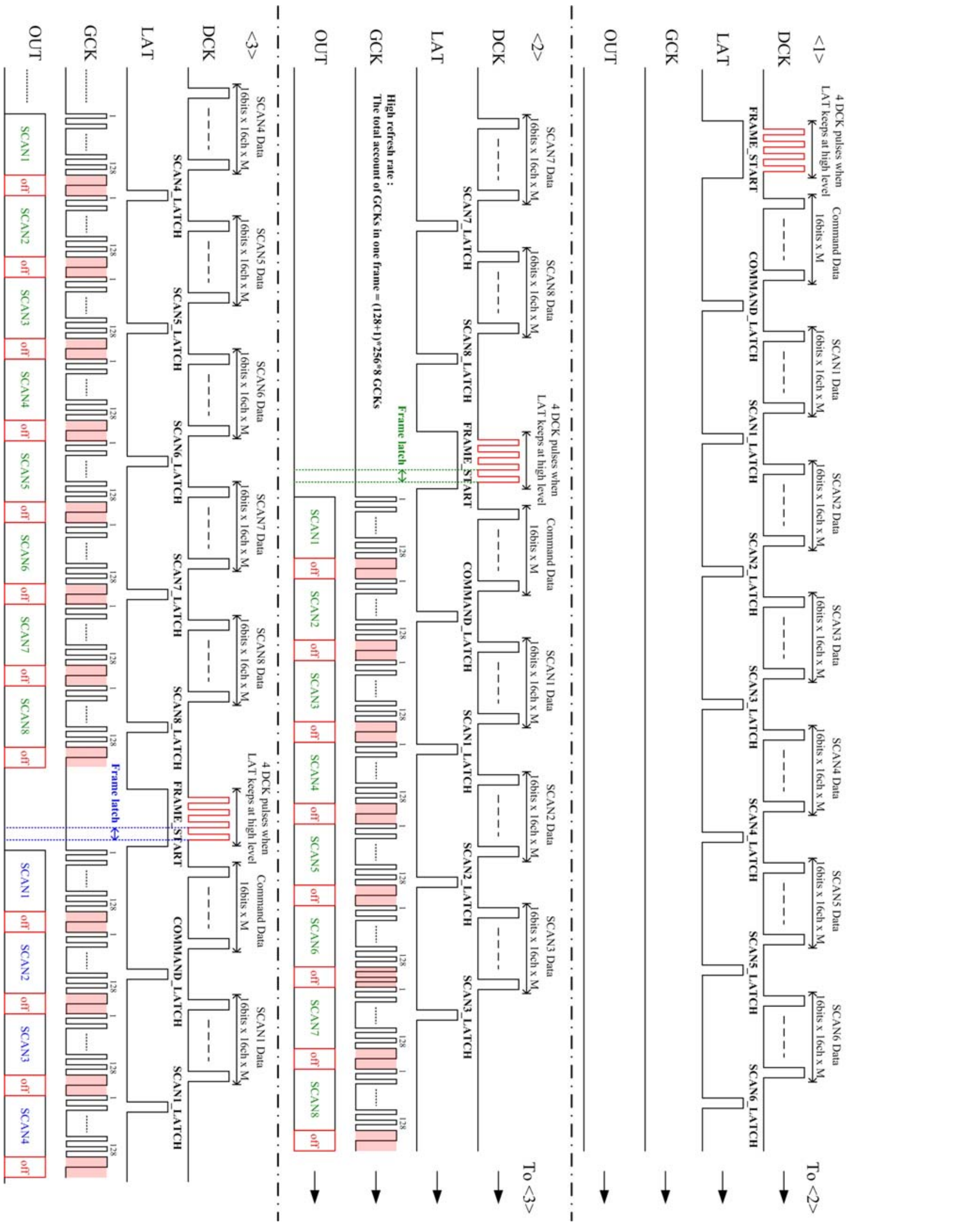
The ghost image abatement is an optional instruction designed to eliminate ghosting of multiplexed LED modules due to parasitic capacitors. When this instruction is active, output pins of constant current would be pulled high to VDD in the automatic black frame by an internal pre-charge MOS. The VDD voltage on the parasitic capacitor prevents the inrush current resulting from turning on the switching PMOS of next scan line. This function is valid when VLED is close to VDD.



Data Timing Diagram (Dynamic 1/8 Scanning Mode, Low Refresh Rate)



Data Timing Diagram (Dynamic 1/8 Scanning Mode, High Refresh Rate)



Power Dissipation

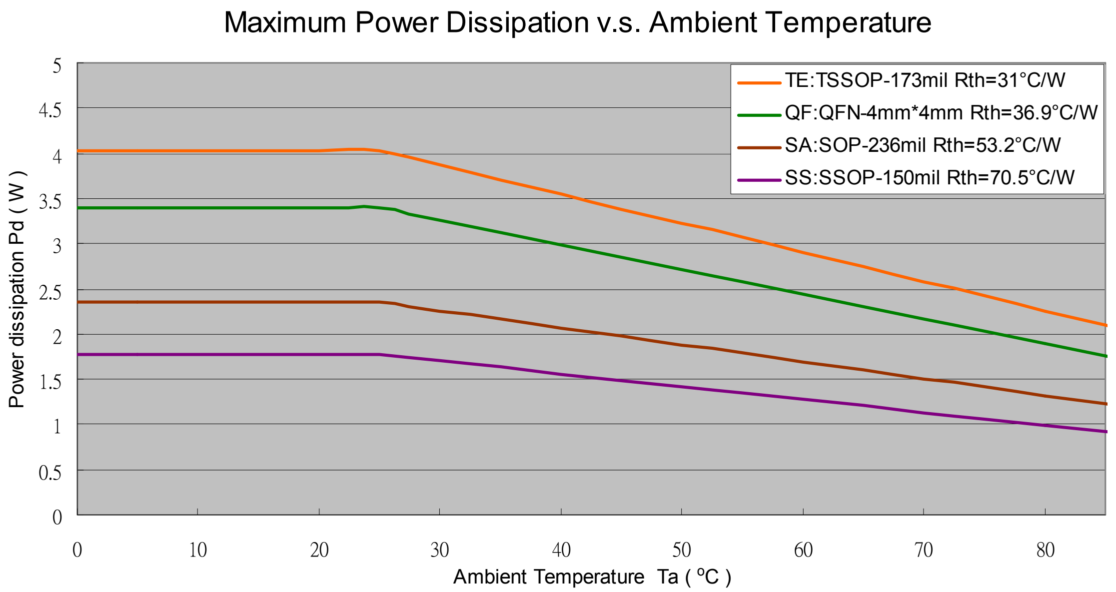
When the 16 output channels are turned on, the practical power dissipation is determined by the following equation:

$$PD\ (practical) = V_{DD} \times I_{DD} + Vout_{(0)} \times Iout_{(0)} \times Duty_{(0)} + \cdots + Vout_{(N)} \times Iout_{(N)} \times Duty_{(N)}\ ,\ \text{where } N=1 \text{ to } 15$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

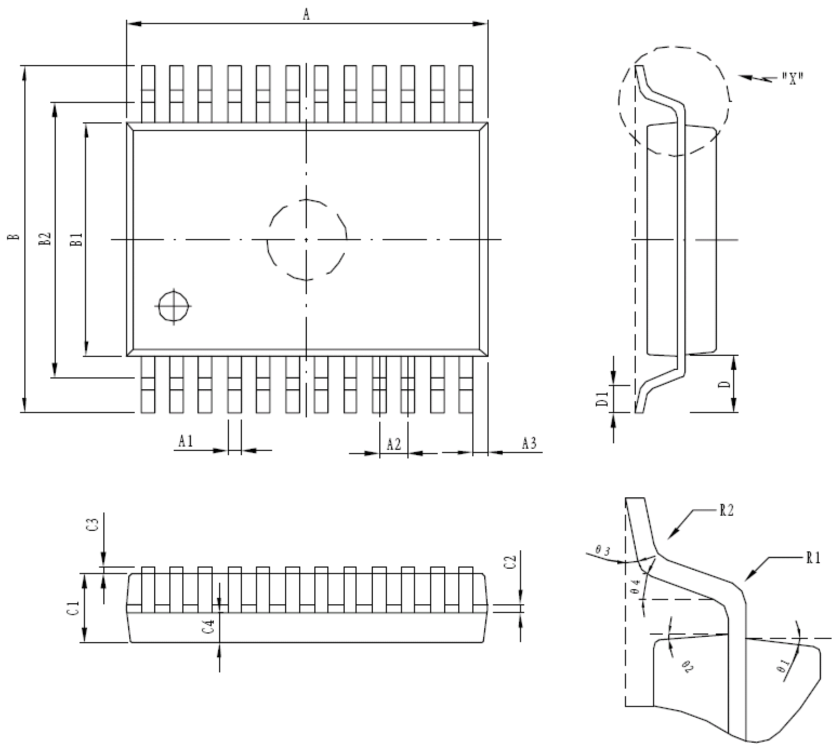
$$PD\ (max) = \frac{Tj(max)(℃) - Ta(℃)}{Rth(j\text{-}a)(℃/Watt)}$$

The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the four different packages.



Package Outline Dimension

SOP-236mil-1.0mm

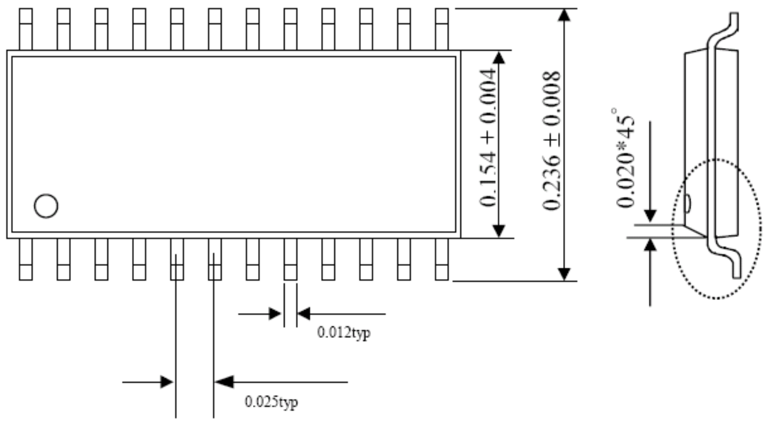


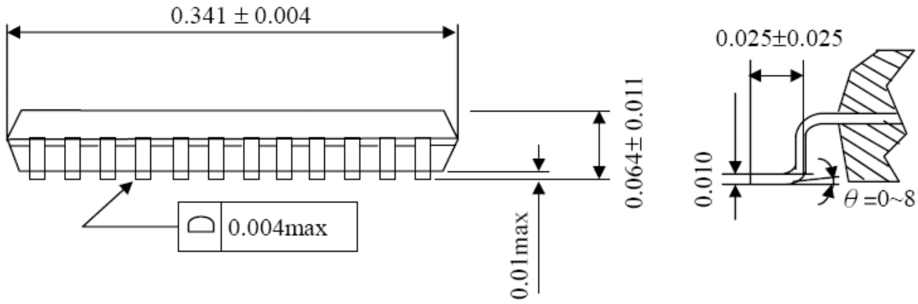
SYMBOL	DIMENSION(mm)		SYMBOL	DIMENSION(mm)	
	MIN.	MAX.		MIN.	MAX.
A	12.9	13.1	**C3**	0.05	0.2
A1	0.30	0.50	**C4**	0.80TYP	
A2	1.00TYP		**D**	0.95TYP	
A3	0.8TYP		**D1**	0.33	0.73
B	7.60	8.20	**R1**	0.2TYP	
B1	5.90	6.10	**R2**	0.2TYP	
B2			**θ1**	8°TYP	
C		2.20	**θ2**	10°TYP	
C1	1.70	1.90	**θ3**	4°TYP	
C2	0.15	0.30	**θ4**	5°TYP	

Package Outline Dimension

SSOP-150mil-0.635mm

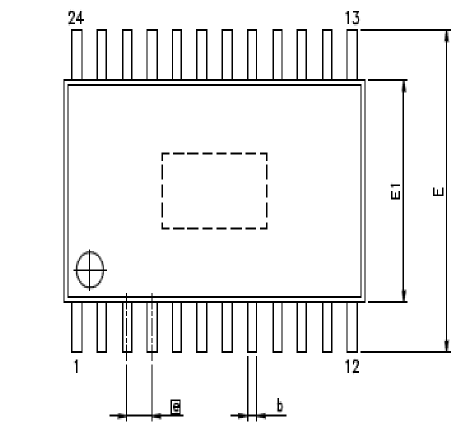
Unit: inch

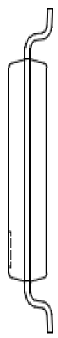


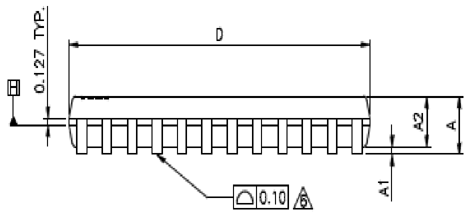


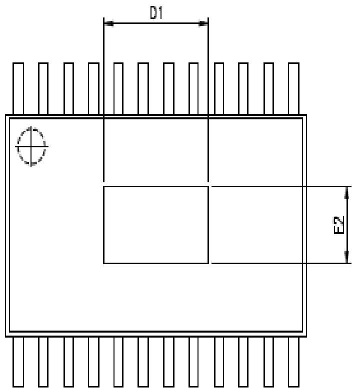
Package Outline Dimension

TSSOP-173mil-0.65mm

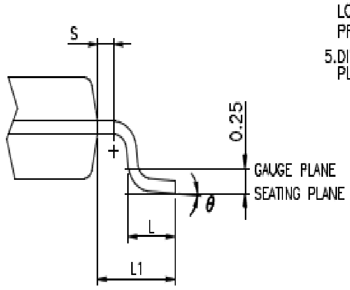








THERMALLY ENHANCED VARIATIONS ONLY



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
112X18E	2.28	2.85	3.70	4.62

NOTES:

1.JEDEC OUTLINE :
STANDARD : MO-153 AD REV.F
THERMALLY ENHANCED : MO-153 ADT REV.F

2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

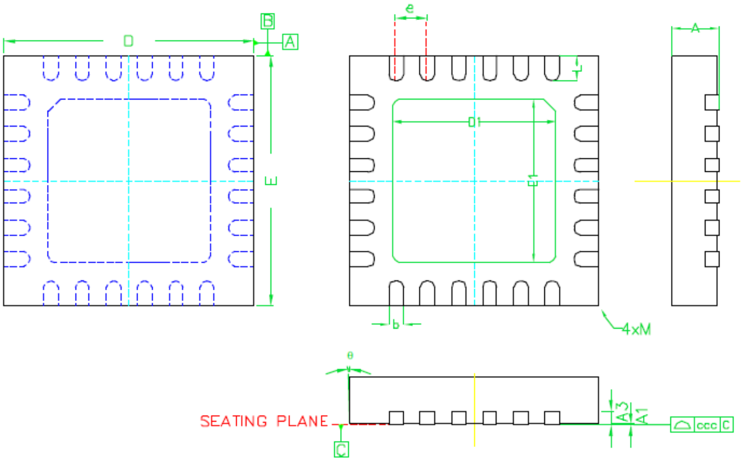
3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

4.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.

5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

Package Outline Dimension

QFN24-4mm x 4mm



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.010	0.030
A3	——	0.20REF.	——
b	0.18	0.23	0.28
D	3.95	4.00	4.03
D1	——	2.60BSC	——
E	3.95	4.00	4.03
E1	——	2.60BSC	——
e	——	0.50BSC	——
L	0.35	0.40	0.45
θ	-12	——	0
ccc	——	0.08	——
M	——	——	0.05
Burr	0	0.030	0.060

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
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