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Serial NOR Flash Memory
MYXN25Q256A13ESF*

***Advanced information. Subject to change without notice.**

256Mb, 3V, Multiple I/O, 4KB Sector Erase

Features

- SPI-compatible serial bus interface
- Double transfer rate (DTR) mode
- 2.7–3.6V single supply voltage
- 108 MHz (MAX) clock frequency supported for all protocols in single transfer rate (STR) mode
- 54 MHz (MAX) clock frequency supported for all protocols in DTR mode
- Dual/quad I/O instruction provides increased throughput up to 54 MB/s
- Supported protocols
  - Extended SPI, dual I/O, and quad I/O
  - DTR mode supported on all
- Execute-in-place (XIP) mode for all three protocols
  - Configurable via volatile or nonvolatile registers
  - Enables memory to work in XIP mode directly after power-on
- PROGRAM/ERASE SUSPEND operations
- Continuous read of entire memory via a single command
  - Fast read
  - Quad or dual output fast read
  - Quad or dual I/O fast read
- Flexible to fit application
  - Configurable number of dummy cycles
  - Output buffer configurable
- Software reset
- 3-byte and 4-byte addressability mode supported
- 64-byte, user-lockable, one-time programmable (OTP) dedicated area
- Erase capability
  - Subsector erase 4KB uniform granularity blocks
  - Sector erase 64KB uniform granularity blocks
  - Full-chip erase
- Write protection
  - Software write protection applicable to every 64KB sector via volatile lock bit
  - Hardware write protection: protected area size defined by five nonvolatile bits (BP0, BP1, BP2, BP3, and TB)
  - Additional smart protections, available upon request
- Electronic signature
  - JEDEC-standard 2-byte signature (BA19h)
  - Unique ID of 17 read-only bytes including: additional extended device ID (EDID) to identify device factory options; customized factory data
- Minimum 100,000 ERASE cycles per sector
- More than 20 years data retention

Options	Code
• Packages: TSOPII	DG
▪ SOP2-16/300mils	SF
• Temperature Ranges	
▪ Military (-55°C to +125°C)	XT
• Part Marking: Label (L), Dot (D)	

AS9100 Rev. C REGISTERED

MICROSS COMPONENTS QML CERTIFIED

Form #: CSI-D-685 Document 016

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Contents

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1 Device Description

The MYXN25Q256A13ESF is a high-performance multiple input/output serial Flash memory device manufactured on 65nm NOR technology. It features execute-in-place (XIP) functionality, advanced write protection mechanisms, and a high-speed SPI-compatible bus interface. Innovative, high-performance, dual and quad input/output instructions enable double or quadruple the transfer bandwidth for READ and PROGRAM operations.

1.1 Features

The memory is organized as 1024 (64KB) main sectors that are further divided into 16 subsectors each (16,384 subsectors in total). The memory can be erased one 4KB subsector at a time, 64KB sectors at a time, or single die (256Mb) at a time.

The memory is organized as 512 (64KB) main sectors that are further divided into 16 subsectors each (8192 subsectors in total). The memory can be erased one 4KB subsector at a time, 64KB sectors at a time, or as a whole.

The device has 64 one-time programmable (OTP) bytes that can be read and programmed with the READ OTP and PROGRAM OTP commands. These 64 bytes can also be permanently locked with a PROGRAM OTP command.

The device can also pause and resume PROGRAM and ERASE cycles by using dedicated PROGRAM/ERASE SUSPEND and RESUME instructions.

1.2 3-Byte Address and 4-Byte Address Modes

The device features 3-byte or 4-byte address modes to access memory beyond 128Mb.

When 4-byte address mode is enabled, all commands requiring an address must be entered and exited with a 4-byte address mode command: ENTER 4-BYTE ADDRESS MODE command and EXIT 4-BYTE ADDRESS MODE command. The 4-byte address mode can also be enabled through the nonvolatile configuration register.

1.3 Operating Protocols

The memory can be operated with three different protocols:

- Extended SPI (standard SPI protocol upgraded with dual and quad operations)
- Dual I/O SPI
- Quad I/O SPI

The standard SPI protocol is extended and enhanced by dual and quad operations. In addition, the dual SPI and quad SPI protocols improve the data access time and throughput of a single I/O device by transmitting commands, addresses, and data across two or four data lines.

Each protocol contains unique commands to perform READ operations in DTR mode. This enables high data throughput while running at lower clock frequencies.

1.4 XIP Mode

Execute-in-place (XIP) mode allows the memory to be read by sending an address to the device and then receiving the data on one, two, or four pins in parallel, depending on the customer requirements. XIP mode offers maximum flexibility to the application, saves instruction overhead, and reduces random access time.

XIP mode requires only an address (no instruction) to output data, improving random access time and eliminating the need to shadow code onto RAM for fast execution.

Nonvolatile configuration register bits can set XIP mode as the default mode for applications that must enter XIP mode immediately after powering up.

All protocols support XIP operation. For flexibility, multiple XIP entry and exit methods are available.

1.5 Device Configurability

The N25Q family offers additional features that are configured through the nonvolatile configuration register for default and/or nonvolatile settings. Volatile settings can be configured through the volatile and volatile-enhanced configuration registers. These configurable features include the following:

- Number of dummy cycles for the fast READ commands
- Output buffer impedance
- SPI protocol types (extended SPI, dual SPI, or quad SPI)
- Required XIP mode
- Enabling/disabling HOLD
- Enabling/disabling wrap mode

Figure 1: Logic Diagram

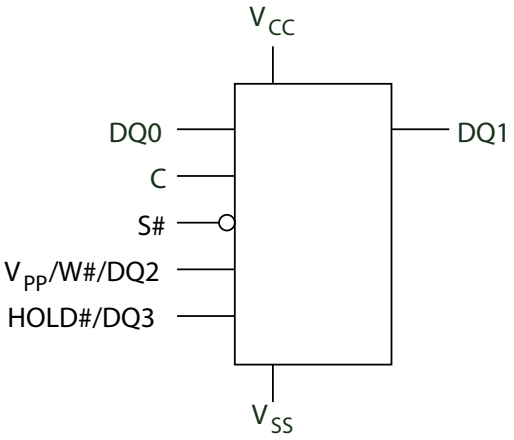
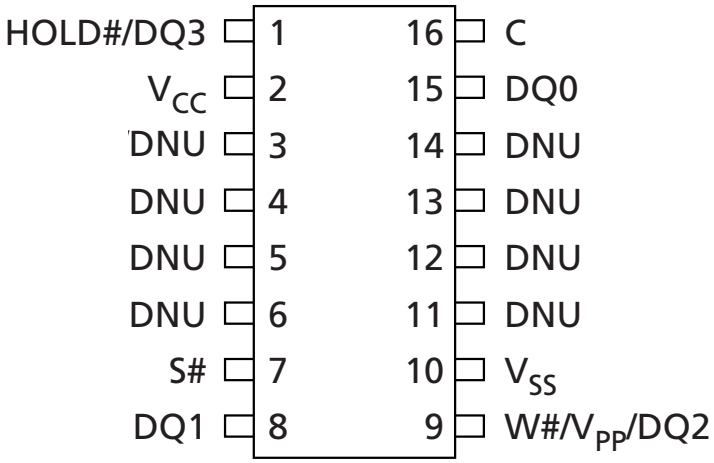


Figure 2: 16-Lead, Plastic Small Outline – SO16 (Top View)



2 Signal Descriptions

The signal description table below is a comprehensive list of signals for the N25 family devices. All signals listed may not be supported on this device.

Table 1: Signal Descriptions

Symbol	Type	Description
C	Input	Clock: Provides the timing of the serial interface. Commands, addresses, or data present at serial data inputs are latched on the rising edge of the clock. Data is shifted out on the falling edge of the clock.
S#	Input	Chip select: When S# is HIGH, the device is deselected and DQ1 is at High-Z. When in extended SPI mode, with the device deselected, DQ1 is tri-stated. Unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress, the device enters standby power mode (not deep power-down mode). Driving S# LOW enables the device, placing it in the active power mode. After power-up, a falling edge on S# is required prior to the start of any command.
DQ0	Input and I/O	Serial data: Transfers data serially into the device. It receives command codes, addresses, and the data to be programmed. Values are latched on the rising edge of the clock. DQ0 is used for input/output during the following operations: DUAL OUTPUT FAST READ, QUAD OUTPUT FAST READ, DUAL INPUT/OUTPUT FAST READ, and QUAD INPUT/OUTPUT FAST READ. When used for output, data is shifted out on the falling edge of the clock. In DIO-SPI, DQ0 always acts as an input/output. In QIO-SPI, DQ0 always acts as an input/output, with the exception of the PROGRAM or ERASE cycle performed with VPP. The device temporarily enters the extended SPI protocol and then returns to QIO-SPI as soon as V_{PP} goes LOW.
DQ1	Output and I/O	Serial data:Transfers data serially out of the device. Data is shifted out on the falling edge of the clock. DQ1 is used for input/output during the following operations: DUAL INPUT FAST PROGRAM, QUAD INPUT FAST PROGRAM, DUAL INPUT EXTENDED FAST PROGRAM, and QUAD INPUT EXTENDED FAST PROGRAM. When used for input, data is latched on the rising edge of the clock. In DIO-SPI, DQ1 always acts as an input/output. In QIO-SPI, DQ1 always acts as an input/output, with the exception of the PROGRAM or ERASE cycle performed with the enhanced program supply voltage (V_{PP}). In this case the device temporarily enters the extended SPI protocol and then returns to QIO-SPI as soon as V_{PP} goes LOW.
DQ2	Input and I/O	DQ2: When in QIO-SPI mode or in extended SPI mode using QUAD FAST READ commands, the signal functions as DQ2, providing input/output. All data input drivers are always enabled except when used as an output. Micross recommends customers drive the data signals normally (to avoid unnecessary switching current) and float the signals before the memory device drives data on them.
DQ3	Input and I/O	DQ3: When in quad SPI mode or in extended SPI mode using quad FAST READ commands, the signal functions as DQ3, providing input/output. HOLD# is disabled and RESET# is disabled if the device is selected.

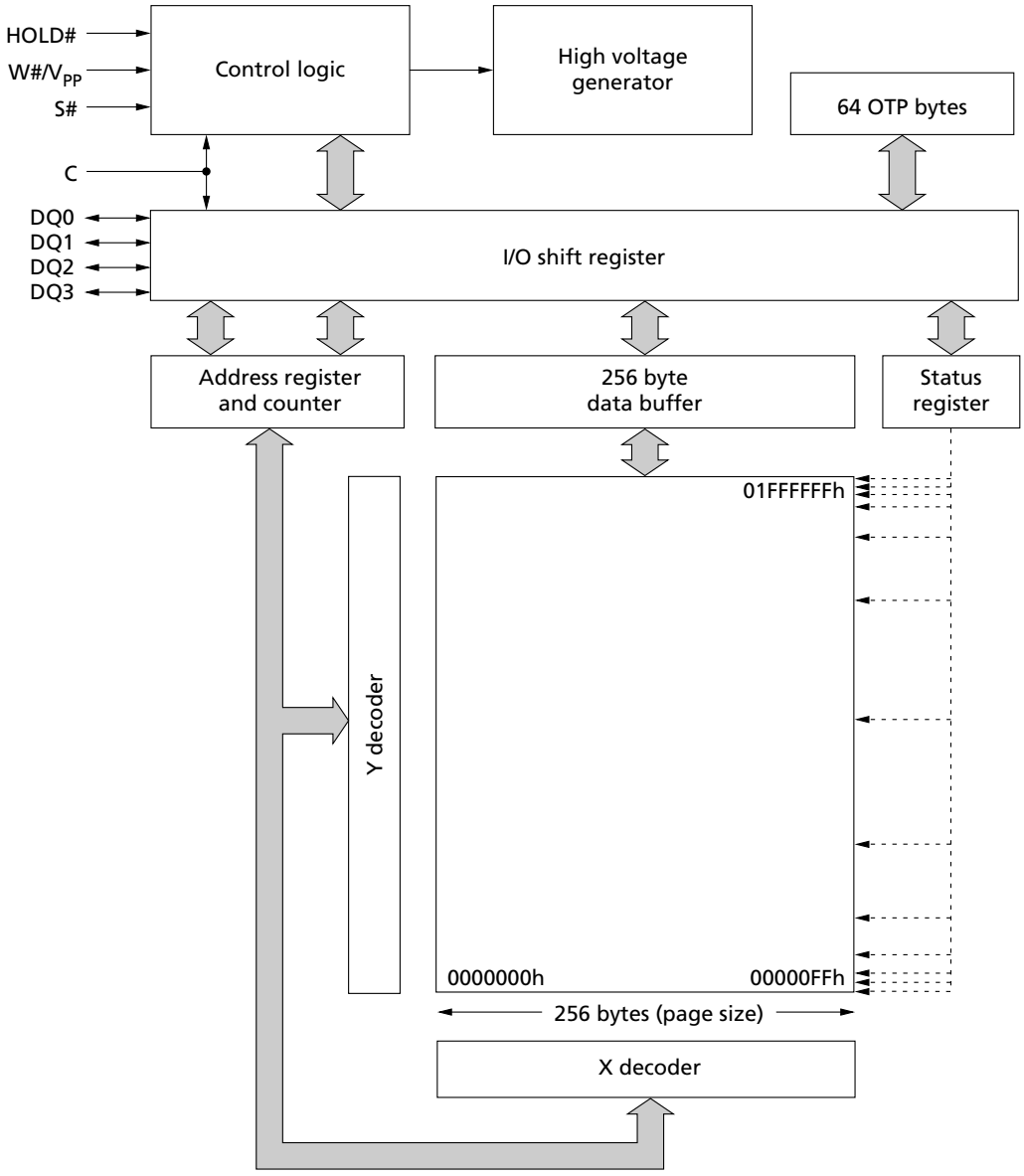
Symbol	Type	Description
HOLD#	Control Input	HOLD: Pauses any serial communications with the device without deselecting the device. DQ1 (output) is High-Z. DQ0 (input) and the clock are Don't Care. To enable HOLD, the device must be selected with S# driven LOW. HOLD# is used for input/output during the following operations: QUAD OUTPUT FAST READ, QUAD INPUT/OUTPUT FAST READ, QUAD INPUT FAST PROGRAM, and QUAD INPUT EXTENDED FAST PROGRAM. In QIO-SPI, HOLD# acts as an I/O (DQ3 functionality), and the HOLD# functionality is disabled when the device is selected. The HOLD# functionality can be disabled using bit 4 of the NVCR or bit 4 of the VECR. On devices that include DTR mode capability, the HOLD# functionality is disabled as soon as a DTR operation is recognized.
W#	Control Input	Write protect: W# can be used as a protection control input or in QIO-SPI operations. When in extended SPI with single or dual commands, the WRITE PROTECT function is selectable by the voltage range applied to the signal. If voltage range is low (0V to V_{CC}), the signal acts as a write protection control input. The memory size protected against PROGRAM or ERASE operations is locked as specified in the status register block protect bits 3:0. W# is used as an input/output (DQ2 functionality) during QUAD INPUT FAST READ and QUAD INPUT/OUTPUT FAST READ operations and in QIO-SPI.
V_{PP}	Power	Supply voltage: If V_{PP} is in the voltage range of V_{PPH}, the signal acts as an additional power supply, as defined in the AC Measurement Conditions table. During QIFP, QIEFP, and QIO-SPI PROGRAM/ERASE operations, it is possible to use the additional V_{PP} power supply to speed up internal operations. However, to enable this functionality, it is necessary to set bit 3 of the VECR to 0. In this case, V_{PP} is used as an I/O until the end of the operation. After the last input data is shifted in, the application should apply V_{PP} voltage to V_{PP} within 200ms to speed up the internal operations. If the V_{PP} voltage is not applied within 200ms, the PROGRAM/ERASE operations start at standard speed. The default value of VECR bit 3 is 1, and the V_{PP} functionality for quad I/O modify operations is disabled.
V_{CC}	Power	Device core power supply: Source voltage.
V_{SS}	Ground	Ground: Reference for the V_{CC} supply voltage.
DNU	–	Do not use.
NC	–	No connect.

3 Memory Organization

3.1 Memory Configuration and Block Diagram

Each page of memory can be individually programmed. Bits are programmed from one through zero. The device is subsector, sector, or bulk erasable, but not page-erasable. Bits are erased from zero through one. The memory is configured as 33,554,432 bytes (8bits each); 512 sectors (64KB each); 8192 subsectors (4KB each); and 131,072 pages (256 bytes each); and 64 OTP bytes are located outside the main memory array.

Figure 3: Block Diagram



4 Memory Map – 256Mb Density

Table 2: Sectors[511:0]

Sector	Subsector	Address Range	
		Start	End
511	8191	01FF F000h	01FF FFFFh
	⋮	⋮	⋮
	8176	01FF 0000h	01FF 0FFFh
⋮	⋮	⋮	⋮
255	4095	00FF F000h	00FF FFFFh
	⋮	⋮	⋮
	4080	00FF 0000h	00FF 0FFFh
⋮	⋮		
127	2047	007F F000h	007F FFFFh
	⋮	⋮	⋮
	2032	007F 0000h	007F 0FFFh
⋮	⋮	⋮	⋮
63	1023	003F F000h	003F FFFFh
	⋮	⋮	⋮
	1008	003F 0000h	003F 0FFFh
⋮	⋮	⋮	⋮
0	15	0000 F000h	0000 FFFFh
	⋮	⋮	⋮
	0	0000 0000h	0000 0FFFh

5 Serial Peripheral Interface Modes

The device can be driven by a microcontroller while its serial peripheral interface is in either of the two modes shown here. The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring data. Input data is latched in on the rising edge of the clock, and output data is available from the falling edge of the clock.

Table 3: SPI Modes

Note 1 applies to the entire table.

SPI Modes	Clock Polarity
CPOL = 0, CPHA = 0	C remains at 0 for (CPOL = 0, CPHA = 0)
CPOL = 1, CPHA = 1	C remains at 1 for (CPOL = 1, CPHA = 1)

Note:

1. The listed SPI modes are supported in extended, dual, and quad SPI protocols.

Shown below is an example of three memory devices in extended SPI protocol in a simple connection to an MCU on an SPI bus. Because only one device is selected at a time, that one device drives DQ1, while the other devices are High-Z.

Resistors ensure the device is not selected if the bus master leaves S# High-Z. The bus master might enter a state in which all input/output is High-Z simultaneously, such as when the bus master is reset. Therefore, the serial clock must be connected to an external pull-down resistor so that S# is pulled HIGH while the serial clock is pulled LOW. This ensures that S# and the serial clock are not HIGH simultaneously and that ^{t}SHCH is met. The typical resistor value of 100kΩ, assuming that the time constant R × Cp (Cp = parasitic capacitance of the bus line), is shorter than the time the bus master leaves the SPI bus in High-Z.

Example: Cp = 50pF, that is R × Cp = 5µs. The application must ensure that the bus master never leaves the SPI bus High-Z for a time period shorter than 5µs. W# and HOLD# should be driven either HIGH or LOW, as appropriate.

Figure 4: Bus Master and Memory Devices on the SPI Bus

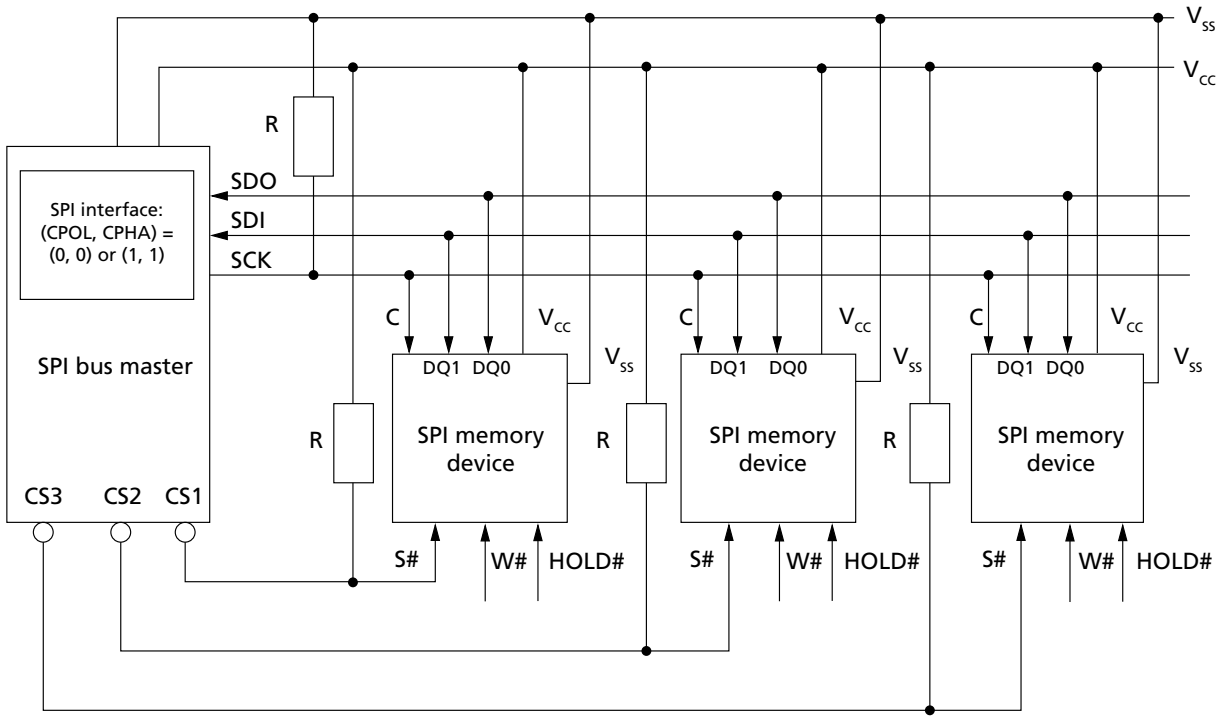
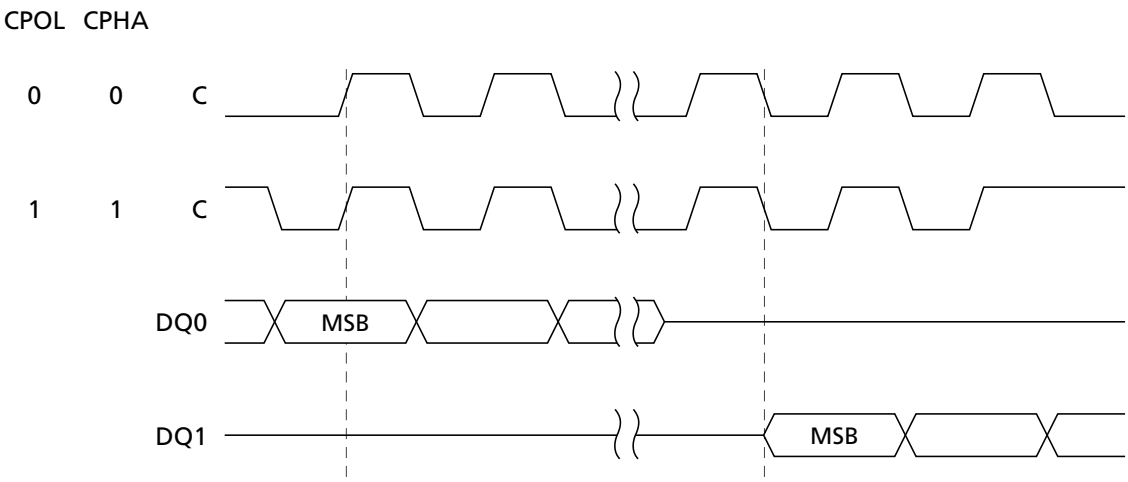


Figure 5: SPI Modes



6 SPI Protocols

Table 4: Extended, Dual, and Quad SPI Protocols

Protocol Name	Command Input	Address Input	Data Input/Output	Description
Extended	DQ0	Multiple DQn lines, depending on the command	Multiple DQn lines, depending on the command	Device default protocol from the factory. Additional commands extend the standard SPI protocol and enable address or data transmission on multiple DQn lines.
Dual	DQ[1:0]	DQ[1:0]	DQ[1:0]	**Volatile selectable**: When the enhanced volatile configuration register bit 6 is set to 0 and bit 7 is set to 1, the device enters the dual SPI protocol immediately after the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command. The device returns to the default protocol after the next power-on. In addition, the device can return to default protocol using the rescue sequence or through new WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command, without power-off or power-on. **Nonvolatile selectable**: When nonvolatile configuration register bit 2 is set, the device enters the dual SPI protocol after the next power-on. Once this register bit is set, the device defaults to the dual SPI protocol after all subsequent power-on sequences until the nonvolatile configuration register bit is reset to 1.
Quad1	DQ[3:0]	DQ[3:0]	DQ[3:0]	**Volatile selectable**: When the enhanced volatile configuration register bit 7 is set to 0, the device enters the quad SPI protocol immediately after the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command. The device re- turns to the default protocol after the next power-on. In addition, the device can return to default protocol using the rescue sequence or through new WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command, without poweroff or power-on. **Nonvolatile selectable**: When nonvolatile configuration register bit 3 is set to 0, the device enters the quad SPI protocol after the next power-on. Once this register bit is set, the device defaults to the quad SPI protocol after all subsequent power-on sequences until the nonvolatile configuration register bit is reset to 1.

Note: 1. In quad SPI protocol, all command/address input and data I/O are transmitted on four lines except during a PROGRAM and ERASE cycle performed with V_{PP}. In this case, the device enters the extended SPI protocol to temporarily allow the application to perform a PROGRAM/ERASE SUSPEND operation or to check the write-in-progress bit in the status register or the program/erase controller bit in the flag status register. Then, when V_{PP} goes LOW, the device returns to the quad SPI protocol.

7 Nonvolatile and Volatile Registers

The device features the following volatile and nonvolatile registers that users can access to store device parameters and operating configurations:

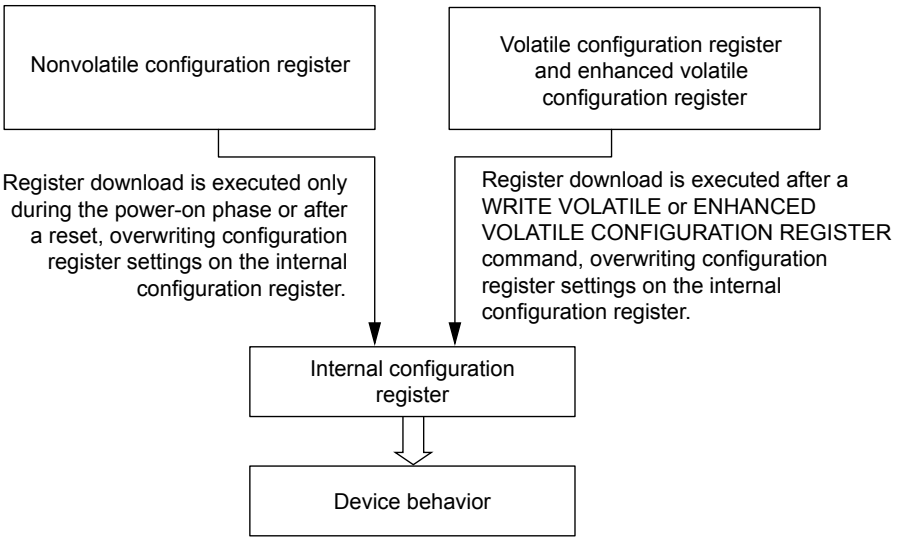
- Status register
- Nonvolatile and volatile configuration registers
- Extended address register
- Enhanced volatile configuration register
- Flag status register
- Lock register

Note: The lock register is defined in READ LOCK REGISTER Command.

The working condition of memory is set by an internal configuration register that is not directly accessible to users. As shown below, parameters in the internal configuration register are loaded from the nonvolatile configuration register during each device boot phase or power-on reset. In this sense, then, the nonvolatile configuration register contains the default settings of memory.

Also, during the life of an application, each time a WRITE VOLATILE or ENHANCED VOLATILE CONFIGURATION REGISTER command executes to set configuration parameters in these respective registers, these new settings are copied to the internal configuration register. Therefore, memory settings can be changed in real time. However, at the next power-on reset, the memory boots according to the memory settings defined in the nonvolatile configuration register parameters.

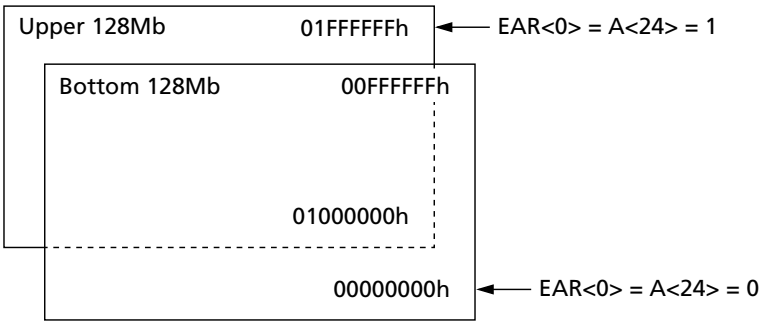
Figure 6: Internal Configuration Register



7.1 Extended Address Register

For devices whose A[MAX:MIN] equals A[23:0], the N25 family includes an extended address register that provides a fourth address byte A[31:24], enabling access to memory beyond 128Mb. Extended address register bit 0 is used to select the upper 128Mb segment or the lower 128Mb segment of the memory array.

Figure 7: Upper and Lower 128Mb Memory Array Segments



The PROGRAM and ERASE operations act upon the 128Mb segment selected in the extended address register.

The BULK ERASE operation erases the entire device.

The READ operation begins reading in the selected 128Mb segment, but is not bound by it. In a continuous READ, when the last byte of the segment is read, the next byte output is the first byte of the other segment as the operation wraps to 0000000h; Therefore, a download of the whole array is possible with one READ operation. The value of the extended address register does not change when a READ operation crosses the selected 128Mb boundary.

8 Command Definitions

Table 5: Command Set

Command	Code	Extended	Dual I/O	Quad I/O	Data Bytes
RESET Operations					
RESET ENABLE	66h	Yes	Yes	Yes	0
RESET MEMORY	99h	Yes	Yes	Yes	0
IDENTIFICATION Operations					
READ ID	9E/9Fh	Yes	No	No	1 to 20
MULTIPLE I/O READ ID	AFh	No	Yes	Yes	1 to 3
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	Yes	Yes	Yes	1 to ∞
READ Operations					
READ	03h	Yes	No	No	1 to ∞
FAST READ	0Bh	Yes	Yes	Yes	1 to ∞
DUAL OUTPUT FAST READ	3Bh	Yes	Yes	No	1 to ∞
DUAL INPUT/OUTPUT FAST READ	0Bh, 3Bh, BBh	Yes	Yes	No	1 to ∞
QUAD OUTPUT FAST READ	6Bh	Yes	No	Yes	1 to ∞
QUAD INPUT/OUTPUT FAST READ	0Bh, 6Bh, EBh	Yes	No	Yes	1 to ∞
FAST READ – DTR	0Dh	Yes	Yes	Yes	1 to ∞
DUAL OUTPUT FAST READ – DTR	3Dh	Yes	Yes	No	1 to ∞
DUAL INPUT/OUTPUT FAST READ – DTR	0Dh, 3Dh, BDh	Yes	Yes	No	1 to ∞
QUAD OUTPUT FAST READ – DTR	6Dh	Yes	No	Yes	1 to ∞
QUAD INPUT/OUTPUT FAST READ – DTR	0Dh, 3Dh, EDh	Yes	No	Yes	1 to ∞
4-BYTE READ	13h	Yes	Yes	Yes	1 to ∞
4-BYTE FAST READ	0Ch	Yes	Yes	Yes	1 to ∞
4-BYTE DUAL OUTPUT FAST READ	3Ch	Yes	Yes	No	1 to ∞
4-BYTE DUAL INPUT/OUTPUT FAST READ	BCh	Yes	Yes	No	1 to ∞
4-BYTE QUAD OUTPUT FAST READ	6Ch	Yes	No	Yes	1 to ∞
4-BYTE QUAD INPUT/OUTPUT FAST READ	ECh	Yes	No	Yes	1 to ∞

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Command	Code	Extended	Dual I/O	Quad I/O	Data Bytes
WRITE Operations					
WRITE ENABLE	06h	Yes	Yes	Yes	0
WRITE DISABLE	04h	Yes	Yes	Yes	0
REGISTER Operations					
READ STATUS REGISTER	05h	Yes	Yes	Yes	1 to ∞
WRITE STATUS REGISTER	01h	Yes	Yes	Yes	1
READ LOCK REGISTER	E8h	Yes	Yes	Yes	1 to ∞
WRITE LOCK REGISTER	E5h	Yes	Yes	Yes	1
READ FLAG STATUS REGISTER	70h	Yes	Yes	Yes	1 to ∞
CLEAR FLAG STATUS REGISTER	50h	Yes	Yes	Yes	0
READ NONVOLATILE CONFIGURATION REGISTER	B5h	Yes	Yes	Yes	2
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	Yes	Yes	Yes	2
READ VOLATILE CONFIGURATION REGISTER	85h	Yes	Yes	Yes	1 to ∞
WRITE VOLATILE CONFIGURATION REGISTER	81h	Yes	Yes	Yes	1
READ ENHANCED VOLATILE CONFIGURATION REGISTER	65h	Yes	Yes	Yes	1 to ∞
WRITE ENHANCED VOLATILE CONFIGURATION REGISTER	61h	Yes	Yes	Yes	1
READ EXTENDED ADDRESS REGISTER	C8h	Yes	Yes	Yes	0
WRITE EXTENDED ADDRESS REGISTER	C5h	Yes	Yes	Yes	0
PROGRAM Operations					
PAGE PROGRAM	02h	Yes	Yes	Yes	1 to 256
DUAL INPUT FAST PROGRAM	A2h	Yes	Yes	No	1 to 256
EXTENDED DUAL INPUT FAST PROGRAM	02h, A2h, D2h	Yes	Yes	No	1 to 256
QUAD INPUT FAST PROGRAM	32h	Yes	No	Yes	1 to 256
EXTENDED QUAD INPUT FAST PROGRAM	02h, 32h, 12h	Yes	No	Yes	1 to 256
ERASE Operations					
SUBSECTOR ERASE	20h	Yes	Yes	Yes	0
SECTOR ERASE	D8h	Yes	Yes	Yes	0
DIE ERASE	C4h	Yes	Yes	Yes	0
PROGRAM/ERASE RESUME	7Ah	Yes	Yes	Yes	0
PROGRAM/ERASE SUSPEND	75h	Yes	Yes	Yes	0

Command	Code	Extended	Dual I/O	Quad I/O	Data Bytes
ONE-TIME PROGRAMMABLE (OTP) Operations					
READ OTP ARRAY	4Bh	Yes	Yes	Yes	1 to 64
PROGRAM OTP ARRAY	42h	Yes	Yes	Yes	1 to 64
4-BYTE ADDRESS MODE Operations					
ENTER 4-BYTE ADDRESS MODE	B7h	Yes	Yes	Yes	0
EXIT 4-BYTE ADDRESS MODE	E9h	Yes	Yes	Yes	0

Note: “Yes” in the protocol columns indicates that the command is supported and has the same functionality and command sequence as other commands marked “Yes.”

9 RESET Operations

Table 6: Reset Command Set

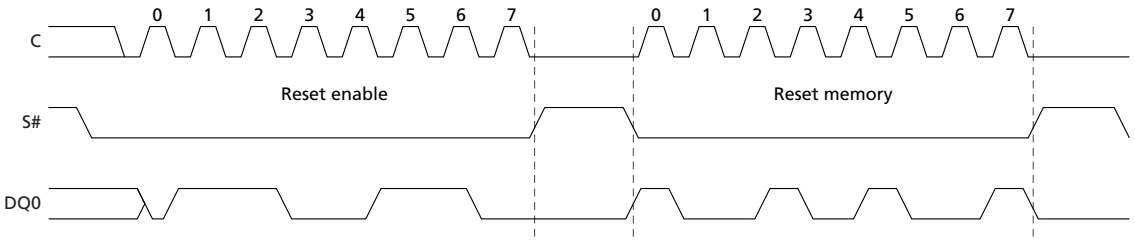
Command	Command Code (Binary)	Command Code (Hex)	Address Bytes
RESET ENABLE	0110 0110	66	0
RESET MEMORY	1001 1001	99	0

9.1 RESET ENABLE and RESET MEMORY Command

To reset the device, the RESET ENABLE command must be followed by the RESET MEMORY command. To execute each command, S# is driven LOW. The command code is input on DQ0. A minimum de-selection time of ^{t}SHSL2 must come between the RESET ENABLE and RESET MEMORY commands or a reset is not guaranteed. When these two commands are executed and S# is driven HIGH, the device enters a power-on reset condition. A time of ^{t}SHSL3 is required before the device can be re-selected by driving S# LOW. It is recommended that the device exit XIP mode before executing these two commands to initiate a reset.

If a reset is initiated while a WRITE, PROGRAM, or ERASE operation is in progress or suspended, the operation is aborted and data may be corrupted.

Figure 8: Figure 35: RESET ENABLE and RESET MEMORY Command



9.2 RESET Conditions

All volatile lock bits, the volatile configuration register, the enhanced volatile configuration register, and the extended address register are reset to the power-on reset default condition. The power-on reset condition depends on settings in the nonvolatile configuration register.

10 ADDRESS MODE Operations: Enter and Exit 4-Byte Address Mode

Both ENTER 4-BYTE ADDRESS MODE and EXIT 4-BYTE ADDRESS MODE commands share the same requirements.

To enter or exit the 4-byte address mode, the WRITE ENABLE command must be executed to set the write enable latch bit to 1.

S# must be driven LOW. The command must be input on DQn. The effect of the command is immediate; after the command has been executed, the write enable latch bit is cleared to 0.

The default address mode is three bytes, and the device returns to the default upon exiting the 4-byte address mode.

11 Power-Up and Power-Down

11.1 Power-Up and Power-Down Requirements

At power-up and power-down, the device must not be selected; that is, S# must follow the voltage applied on V_{CC} until V_{CC} reaches the correct values: $V_{CC,min}$ at power-up and V_{SS} at power-down.

To avoid data corruption and inadvertent WRITE operations during power-up, a power-on reset circuit is included. The logic inside the device is held to RESET while V_{CC} is less than the power-on reset threshold voltage shown here; all operations are disabled, and the device does not respond to any instruction. During a standard power-up phase, the device ignores all commands except READ STATUS REGISTER and READ FLAG STATUS REGISTER. These operations can be used to check the memory internal state. After power-up, the device is in standby power mode; the write enable latch bit is reset; the write in progress bit is reset; and the lock registers are configured as: (write lock bit, lock down bit) = (0,0).

Normal precautions must be taken for supply line decoupling to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor (typically 100nF) close to the package pins. At power-down, when V_{CC} drops from the operating voltage to below the power-on-reset threshold voltage shown here, all operations are disabled and the device does not respond to any command.

When the operation is in progress, the program or erase controller bit of the status register is set to 0. To obtain the operation status, the flag status register must be polled twice, with S# toggled twice in between commands. When the operation completes, the program or erase controller bit is cleared to 1. The cycle is complete after the flag status register outputs the program or erase controller bit to 1 both times.

Note: If power-down occurs while a WRITE, PROGRAM, or ERASE cycle is in progress, data corruption may result. V_{PPH} must be applied only when V_{CC} is stable and in the $V_{CC,min}$ to $V_{CC,max}$ voltage range.

Figure 9: Power-Up Timing

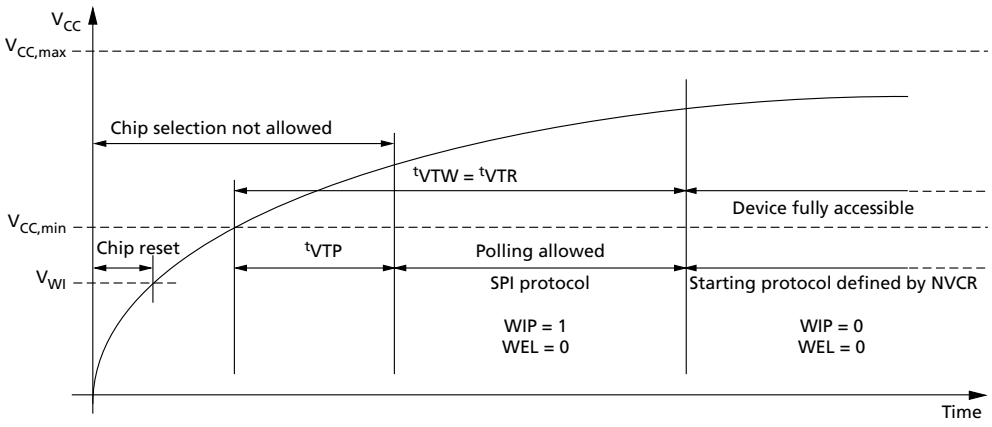


Table 7: Power-Up Timing and VWI Threshold

Parameters listed are characterized only.

Symbol	Parameter	Min	Max	Unit
^{t}VTR	$V_{CC,min}$ to read	–	150	µs
^{t}VTW	$V_{CC,min}$ to device fully accessible	–	150	µs
VWI	Write inhibit voltage	1.5	2.5	V

11.2 Power Loss Recovery Sequence

If a power loss occurs during a WRITE NONVOLATILE CONFIGURATION REGISTER command, after the next power-on, the device might begin in an undetermined state (XIP mode or an unnecessary protocol). If this occurs, until the next power-up, a recovery sequence must reset the device to a fixed state (extended SPI protocol without XIP). After the recovery sequence, the issue should be resolved definitively by running the WRITE NONVOLATILE CONFIGURATION REGISTER command again. The recovery sequence is composed of two parts that must be run in the correct order. During the entire sequence, ^{t}SHSL2 must be at least 50ns. The first part of the sequence is DQ0 (PAD DATA) and DQ3 (PAD HOLD) equal to 1 for the situations listed below:

- 7 clock cycles within S# LOW (S# becomes HIGH before 8th clock cycle)
- + 9 clock cycles within S# LOW (S# becomes HIGH before 10th clock cycle)
- + 13 clock cycles within S# LOW (S# becomes HIGH before 14th clock cycle)
- + 17 clock cycles within S# LOW (S# becomes HIGH before 18th clock cycle)
- + 25 clock cycles within S# LOW (S# becomes HIGH before 26th clock cycle)
- + 33 clock cycles within S# LOW (S# becomes HIGH before 34th clock cycle)

The second part of the sequence is exiting from dual or quad SPI protocol by using the following FFh sequence: DQ0 and DQ3 equal to 1 for 8 clock cycles within S# LOW; S# becomes HIGH before 9th clock cycle.

After this two-part sequence the extended SPI protocol is active.

12 AC Reset Specifications

Table 8: AC RESET Conditions

Note 1 applies to entire table.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reset pulse width	^{t}RLRH2		50	–	–	ns
Reset recovery time	^{t}RHSL	Device deselected (S# HIGH) and is in XIP mode	–	–	40	ns
		Device deselected (S# HIGH) and is in standby mode	–	–	40	ns
		Commands are being decoded, any READ operations are in progress or any WRITE operation to volatile registers are in progress	–	–	40	ns
		Any device array PROGRAM/ERASE/SUSPEND/RESUME, PROGRAM OTP, NONVOLATILE SECTOR LOCK, and ERASE NONVOLATILE SECTOR LOCK ARRAY operations are in progress	–	–	30	µs
		While a WRITE STATUS REGISTER operation is in progress	–	^{t}W	–	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	–	^{t}WNVCR	–	ms
		On completion or suspension of a SUBSECTOR ERASE operation	–	^{t}SSE	–	s
Software reset recovery time	^{t}SHSL3	Device deselected (S# HIGH) and is in standby mode	–	–	90	ns
		Any Flash array PROGRAM/ERASE/SUSPEND/RESUME, PROGRAM OTP, NONVOLATILE SECTOR LOCK, and ERASE NONVOLATILE SECTOR LOCK ARRAY operations are in progress	–	–	30	µs
		While WRITE STATUS REGISTER operation is in progress	–	^{t}W	–	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	–	^{t}WNVCR	–	ms
		On completion or suspension of a SUBSECTOR ERASE operation	–	^{t}SSE	–	s
S# deselect to reset valid	^{t}SHRV	Deselect to reset valid in quad output or in QIO-SPI	2	–	–	ns

Notes:

1. Values are guaranteed by characterization; not 100% tested.
2. The device reset is possible but not guaranteed if ^{t}RLRH < 50ns.

Figure 10: Reset AC Timing During PROGRAM or ERASE Cycle

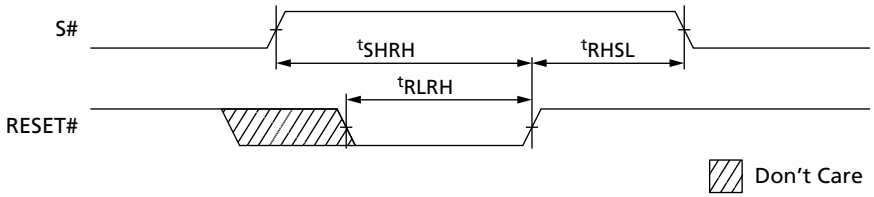


Figure 11: Reset Enable

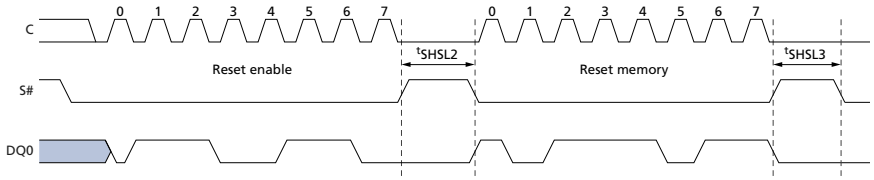


Figure 12: Serial Input Timing

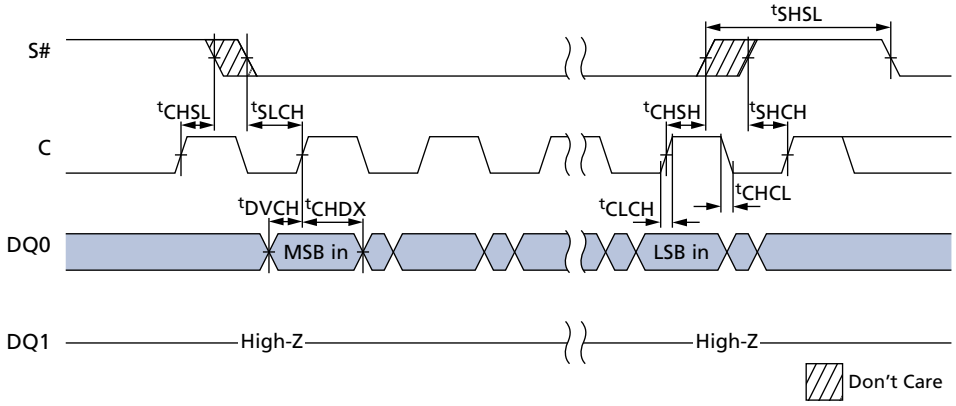


Figure 13: Hold Timing

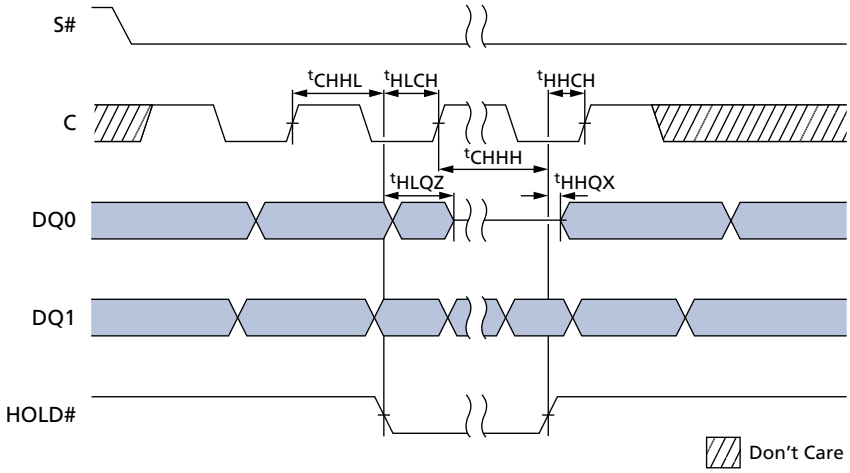


Figure 14: Output Timing

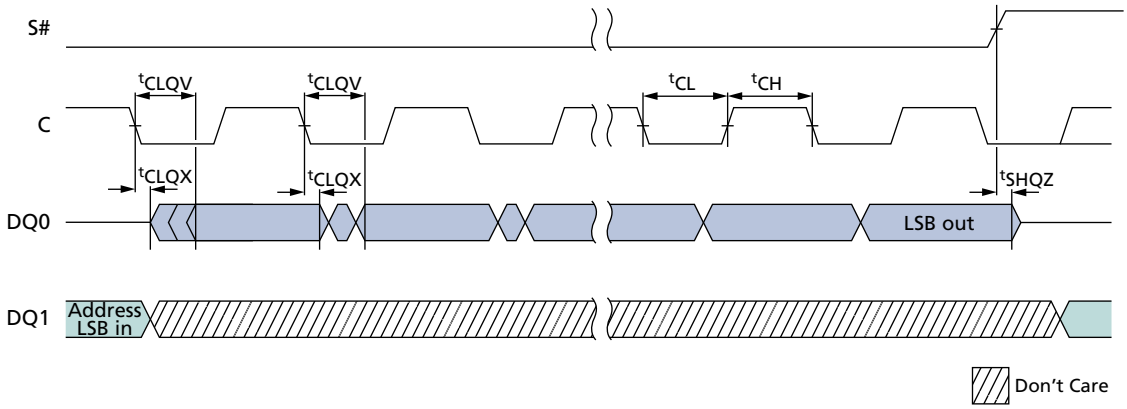
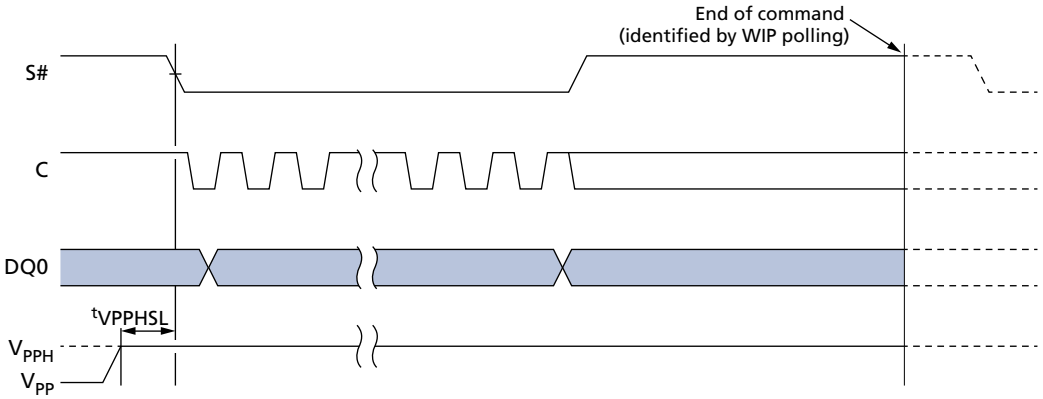


Figure 15: V_{PPH} Timing



13 Absolute Ratings and Operating Conditions

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating for extended periods may adversely affect reliability. Stressing the device beyond the absolute maximum ratings may cause permanent damage.

Table 9: Absolute Ratings

Symbol	Parameter	Min	Max	Units	Notes
T_{STG}	Storage temperature	–65	150	°C	
T_{LEAD}	Lead temperature during soldering	–	See note 1	°C	
V_{CC}	Supply voltage	–0.6	4.0	V	
V_{PP}	Fast program/erase voltage	–0.2	10	V	
V_{IO}	Input/output voltage with respect to ground	–0.6	V_{CC} + 0.6	V	3, 4
V_{ESD}	Electrostatic discharge voltage (human body model)	–2000	2000	V	2

Notes:

1. Compliant with JEDEC Standard J-STD-020C (for small-body, Sn-Pb or Pb assembly), RoHS, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Standard JESD22-A114A (C1 = 100pF, R1 = 1500Ω, R2 = 500Ω).
3. During signal transitions, minimum voltage may undershoot to –1V for periods less than 10ns.
4. During signal transitions, maximum voltage may overshoot to V_{CC} + 1V for periods less than 10ns

Table 10: Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply voltage	2.7	3.6	V
V_{PPH}	Supply voltage on V_{PP}	8.5	9.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 11: Input/Output Capacitance

These parameters are sampled only, not 100% tested. T_A = 25°C at 54 MHz.

Symbol	Description	Test Condition	Min	Max	Units
CIN/OUT	Input/output capacitance (DQ0/DQ1/DQ2/DQ3)	V_{OUT} = 0V	–	8	pF
CIN	Input capacitance (other pins)	V_{IN} = 0V	–	6	pF

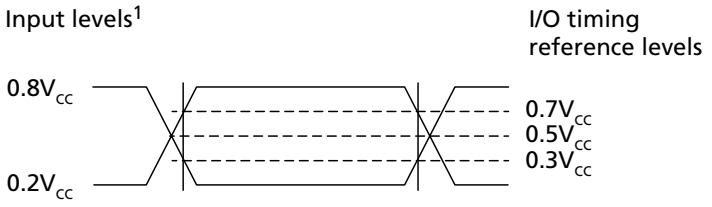
Table 12: AC Timing Input/Output Conditions

Symbol	Description	Min	Max	Units	Notes
CL	Load capacitance	30	30	pF	1
–	Input rise and fall times	–	5	ns	
	Input pulse voltages	0.2V_{CC} to 0.8V_{CC}		V	2
	Input timing reference voltages	0.3V_{CC} to 0.7V_{CC}		V	
	Output timing reference voltages	V_{CC}/2	V_{CC}/2	V	

Notes:

1. Output buffers are configurable by user.
2. For quad/dual operations: 0V to V_{CC}.

Figure 16: AC Timing Input/Output Reference Levels



Note: 0.8VCC = V_{CC} for dual/quad operations; 0.2V_{CC} = 0V for dual/quad operations.

14 DC Characteristics and Operating Conditions

Table 13: DC Current Characteristics and Operating Conditions

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input leakage current	I_{LI}		–	±2	µA
Output leakage current	I_{LO}		–	±2	µA
Standby current	I_{CC1}(1)	S = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	100	µA
Standby current	I_{CC1} (automotive)	S = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	250	µA
Operating current (fast-read extended I/O)	I_{CC3}	C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open	–	15	mA
		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1 = open	–	6	mA
Operating current (fast-read dual I/O)		C = 0.1V_{CC}/0.9V_{CC} at 108 MHz	–	18	mA
Operating current (fast-read quad I/O)		C = 0.1V_{CC}/0.9V_{CC} at 108 MHz	–	20	mA
Operating current (program)	I_{CC4}	S# = V_{CC}	–	20	mA
Operating current (write status register)	I_{CC5}	S# = V_{CC}	–	20	mA
Operating current (erase)	I_{CC6}	S# = V_{CC}	–	20	mA

Note 1: Automotive & Military temperature ranges.

Table 14: DC Voltage Characteristics and Operating Conditions

Parameter	Symbol	Conditions	Min	Max	Unit
Input low voltage	V_{IL}		–0.5	0.3V_{CC}	V
Input high voltage	V_{IH}		0.7V_{CC}	V_{CC} + 0.4	V
Output low voltage	V_{OL}	I_{OL} = 1.6mA	–	0.4	V
Output high voltage	V_{OH}	I_{OH} = –100µA	V_{CC} - 0.2	–	V

15 AC Characteristics and Operating Conditions

Table 15: AC Characteristics and Operating Conditions

Parameter		Symbol	Min	Typ[1]	Max	Unit	Notes
Clock frequency for all commands other than READ (SPI-ER, QIO-SPI protocol)		^{f}C	DC	–	108	MHz	
Clock frequency for READ commands		^{f}R	DC	–	54	MHz	
Clock HIGH time		^{t}CH	4	–	–	ns	2
Clock LOW time		^{t}CL	4	–	–	ns	1
Clock rise time (peak-to-peak)		$^{t}CLCH$	0.1	–	–	V/ns	3, 4
Clock fall time (peak-to-peak)		$^{t}CHCL$	0.1	–	–	V/ns	3, 4
S# active setup time (relative to clock)		$^{t}SLCH$	4	–	–	ns	
S# not active hold time (relative to clock)		$^{t}CHSL$	4	–	–	ns	
Data in setup time		$^{t}DVCH$	2	–	–	ns	
Data in hold time		$^{t}CHDX$	3	–	–	ns	
S# active hold time (relative to clock)		$^{t}CHSH$	4	–	–	ns	
S# not active setup time (relative to clock)		$^{t}SHCH$	4	–	–	ns	
S# deselect time after a READ command		$^{t}SHSL1$	20	–	–	ns	
S# deselect time after a nonREAD command		$^{t}SHSL2$	50	–	–	ns	
Output disable time		$^{t}SHQZ$	–	–	8	ns	3
Clock LOW to output valid under 30pF	STR	$^{t}CLQV$	–	–	7	ns	
	DTR		–	–	8	ns	
Clock LOW to output valid under 10pF	STR		–	–	5	ns	
	DTR		–	–	6	ns	
Output hold time (clock LOW)		$^{t}CLQX$	1	–	–	ns	
Output hold time (clock HIGH)		$^{t}CHQX$	1	–	–	ns	
HOLD command setup time (relative to clock)		$^{t}HLCH$	4	–	–	ns	
HOLD command hold time (relative to clock)		$^{t}CHHH$	4	–	–	ns	
HOLD command setup time (relative to clock)		$^{t}HHCH$	4	–	–	ns	
HOLD command hold time (relative to clock)		$^{t}CHHL$	4	–	–	ns	
HOLD command to output Low-Z		$^{t}HHQX$	–	–	8	ns	3
HOLD command to output High-Z		$^{t}HLQZ$	–	–	8	ns	3

***Advanced information. Subject to change without notice.**

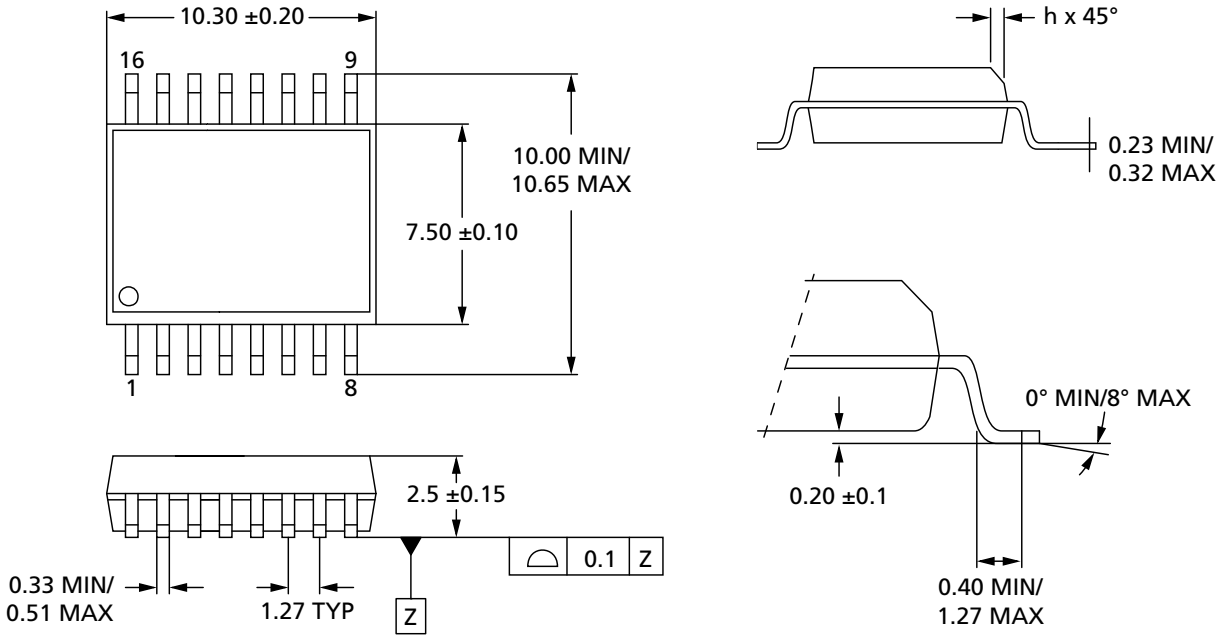
Parameter	Symbol	Min	Typ[1]	Max	Unit	Notes
Write protect setup time	^{t}WHSL	20	–	–	ns	5
Write protect hold time	^{t}SHWL	100	–	–	ns	5
Enhanced V_{PPH} HIGH to S# LOW for extended and dual I/O page program	^{t}VPPHSL	200	–	–	ns	6
WRITE STATUS REGISTER cycle time	^{t}W	–	1.3	8	ms	
Write NONVOLATILE CONFIGURATION REGISTER cycle time	tWNVCR	–	0.2	3	s	
CLEAR FLAG STATUS REGISTER cycle time	^{t}CFSR	–	40	–	ns	
WRITE VOLATILE CONFIGURATION REGISTER cycle time	^{t}WVCR	–	40	–	ns	
WRITE VOLATILE ENHANCED CONFIGURATION REGISTER cycle time	^{t}WRVECR	–	40	–	ns	
WRITE EXTENDED ADDRESS REGISTER cycle time	^{t}WREAR	–	40	–	ns	
PAGE PROGRAM cycle time (256 bytes)	^{t}PP	–	0.5	5	ms	7
PAGE PROGRAM cycle time (*n* bytes)		–	int(n/8) × 0.0158	5	ms	7
PAGE PROGRAM cycle time, $V_{PP} = V_{PPH}$ (256 bytes)		–	0.4	5	ms	7
PROGRAM OTP cycle time (64 bytes)		–	0.2	–	ms	7
Subsector ERASE cycle time	^{t}SSE	–	0.25	0.8	s	
Sector ERASE cycle time	^{t}SE	–	0.7	3	s	
Sector ERASE cycle time (with $V_{PP} = V_{PPH}$)		–	0.6	3	s	
Bulk ERASE cycle time	^{t}BE	–	240	480	s	
Bulk ERASE cycle time (with $V_{PP} = V_{PPH}$)		–	200	480	s	

Notes:

1. Typical values given for T_A = 25 °C.
2. ^{t}CH + ^{t}CL must add up to 1/^{f}C.
3. Value guaranteed by characterization; not 100% tested.
4. Expressed as a slew-rate.
5. Only applicable as a constraint for a WRITE STATUS REGISTER command when STATUS REGISTER WRITE is set to 1.
6. V_{PPH} should be kept at a valid level until the PROGRAM or ERASE operation has completed and its result (success or failure) is known.
7. When using the PAGE PROGRAM command to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes (1 < n < 256).
8. int(A) corresponds to the upper integer part of A. For example int(12/8) = 2, int(32/8) = 4 int(15.3) =16.

16 Package Dimensions

Figure 17: SOP2-16/300 mils



Note: All dimensions are in millimeters.

17 Ordering Information

Table 16: Ordering Information

Part Number	Device Grade
MYXN25Q256A13ESFDG-XT	Military

Please contact a Micross sales representative for IBIS or thermal models at sales@micross.com.

Document Title

256MB, 3V, Multiple I/O, 4KB Sector Erase - Serial NOR Flash Memory

Revision History

Revision #	History	Release Date	Status
1.0	Initial Release	July 8, 2015	Preliminary
1.1	Page 1 (blue box) - removed Industrial temperature range	August 17, 2015	Preliminary