![InnoLux 群創光電]

PRODUCT SPECIFICATION

Doc. Number: DN0383720

☐ Tentative Specification

☐ Preliminary Specification

■ Approval Specification

MODEL NO.: N080ICE
SUFFIX: GB0

Customer: ASUS

APPROVED BY   SIGNATURE

Name / Title

Note :

Only for reference

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Henry Chien	Tsoyu Chu	Julin Huang

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	Jan, 17, 2014	All	Spec Ver.0.0 was first issued.
1.0	Mar, 28, 2014	21 26~29 34~39	OPTICAL SPECIFICATIONS PACKING NT35521 Register setting
2.0	Jun, 05, 2014	32	Update OUTLINE DRAWING (AA to OD)
3.0	Jun, 27, 2014	26	Update MODULE LABEL

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N080ICE-GB0 is a 8" (8" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and **31 pins MIPI** interface. This module supports 800 x 1280 WXGA mode.

1.2 GENERAL SPECIFICATI0NS

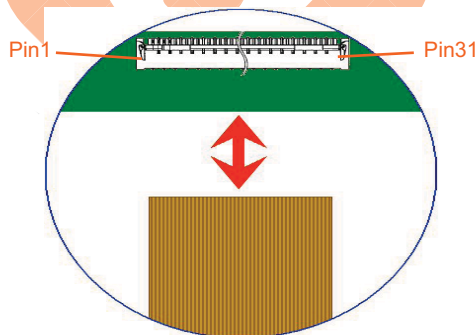| Item	Specification	Unit	Note
Screen Size	8" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	800 x R.G.B. x 1280	pixel	-
Pixel Pitch	0.13455 (H) x 0.13455 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216 (8bit color depth)	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating, Low-Reflection	-	-
Luminance, White	400	Cd/m2	
Power Consumption	*Total 1.65 W (Max.) (panel 0.3 W (Max.), BL 1.35W (Max.))*		(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at **VCI = 3.3 V, VDDI= 1.8V, fv = 60 Hz, Brightness = 400nits, I_{F_LED} = 20mA** and Ta = 25 ± 2 ºC, whereas **white** pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	114.38	114.58	114.78	mm	(1)
	Vertical (V)	183.89	184.09	184.29	mm	
	Thickness (T)			2.2 (w/o PCBA) 4.06 (w/ PCBA)	mm	
CF Polarizer	Horizontal	110.24	110.44	110.64	mm	
	Vertical	175.42	175.62	175.82	mm	
Active Area	Horizontal		107.64		mm	
	Vertical		172.224		mm	
Weight		-	-	77	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: **Hirose FH35W-31S-0.3SHW(50)**

3. ABSOLUTE MAXIMUM RATINGS
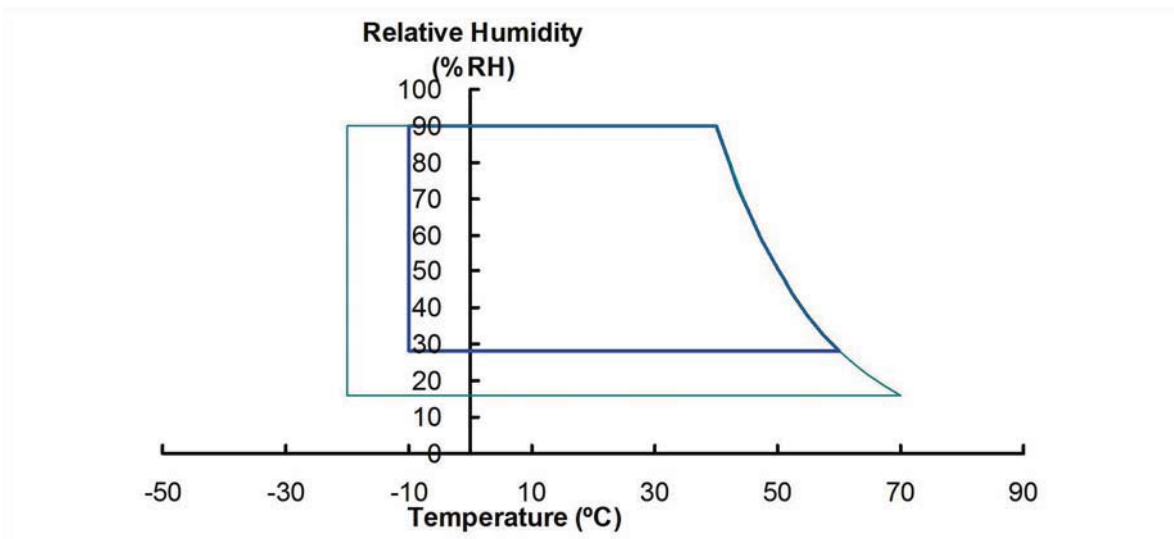
3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value Min.	Value Max.	Unit	Note
Storage Temperature	T_{ST}	-20	+70	°C	(1)
Operating Ambient Temperature	T_{OP}	-10	+60	°C	(1), (2)

Note (1)   (a) 90 %RH Max. (Ta <= 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.

Note (2)   The temperature of panel surface should be -10 °C min. and 70 °C max.

3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value Min.	Value Max.	Unit	Note
Power Supply Voltage	**VCI**	**-0.3**	**+5.0**	**V**	(1)
	VDDI	**-0.3**	**+2.0**	**V**	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM

4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

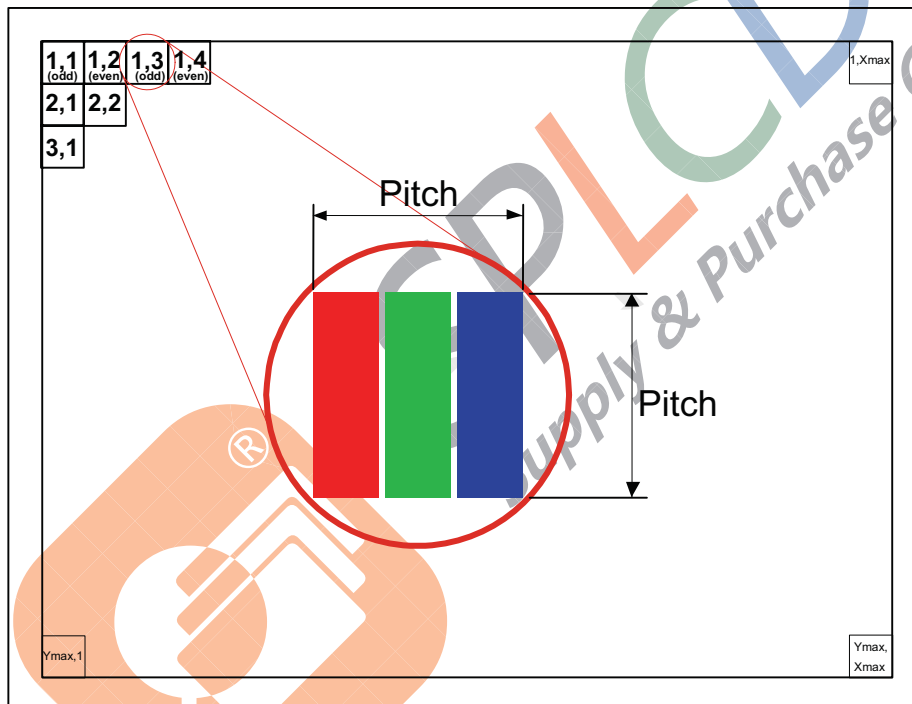| Pin	Symbol	I/O	Description	Remark
1	GND	P	Ground	
2	D3_N	I	MIPI differential data3 input (Negative)	
3	D3_P	I	MIPI differential data3 input (Positive)	
4	GND	P	Ground	
5	D0_N	I	MIPI differential data0 input (Negative)	
6	D0_P	I	MIPI differential data0 input (Positive)	
7	GND	P	Ground	
8	CLK_N	I	MIPI differential clock input (Negative)	
9	CLK_P	I	MIPI differential clock input (Positive)	
10	GND	P	Ground	
11	D1_N	I	MIPI differential data1 input (Negative)	
12	D1_P	I	MIPI differential data1 input (Positive)	
13	GND	P	Ground	
14	D2_N	I	MIPI differential data2 input (Negative)	
15	D2_P	I	MIPI differential data2 input (Positive)	
16	GND	P	Ground	
17	RST	I	Device reset signal	1.7V~1.9V
18	LEDPWM	O	PWM control signal for LED driver (CABC)	
19	GND	P	Ground	
20	ID	P	Ground	
21	VDDI	P	1.8V input	1.7V~1.9V
22	VDDI	P	1.8V input	1.7V~1.9V

23	NC		No connection	
24	VCI	P	3.3V input	3.0V~3.6V
25	VCI	P	3.3V input	3.0V~3.6V
26	NC(MTP)	P	No connection, please keep it floating	
27	LED2	P	Cathode for light bar	
28	LED1	P	Cathode for light bar	
29	NC		No connection	
30	VLED	P	Anode for light bar	
31	VLED	P	Anode for light bar	

Note (1)   The first pixel is odd as shown in the following figure.

Note (2)   Normal operation/BIST pattern selection. (Control by MIPI LP Command)
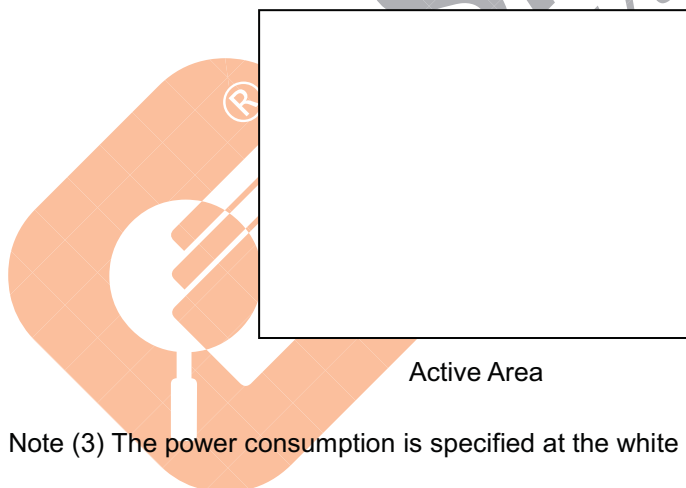
4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Power supply voltage		VCI	3.0	3.3	3.6	V	
		VDDI	1.7	1.8	1.9	V	
VDDI High level input voltage		V_{IH2}	0.7 VDDI	-	VDDI	V	For I/O circuit
VDDI Low level input voltage		V_{IL2}	0	-	0.3 VDDI	V	
Power Supply Current	White	I_{VCI}	-	50	60	mA	Note (2)
		I_{VDDI}	-	45	55	mA	
Power consumption		PLCD	-	-	300	mW	Note (3)

Note (1) The ambient temperature is Ta = 25 ± 2 ℃.

Note (2) The specified power supply current is under the conditions at VCI = 3.3 V, VDDI = 1.8 V, Ta = 25 ± 2 ℃, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

b. White Pattern

Active Area

Note (3) The power consumption is specified at the white pattern with the maximum current

4.3.2 LED CONVERTER SPECIFICATION

N/A

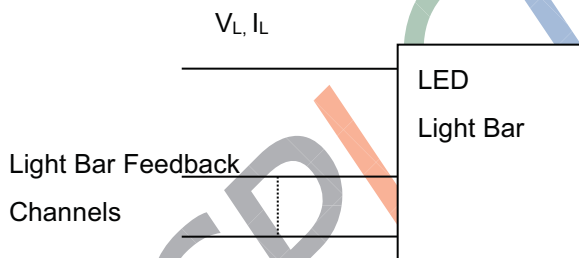### 4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	14	14.5	16	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	80	-	mA	
Power Consumption	P_L	-	1.16	1.35	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :

V_L, I_L

LED
Light Bar
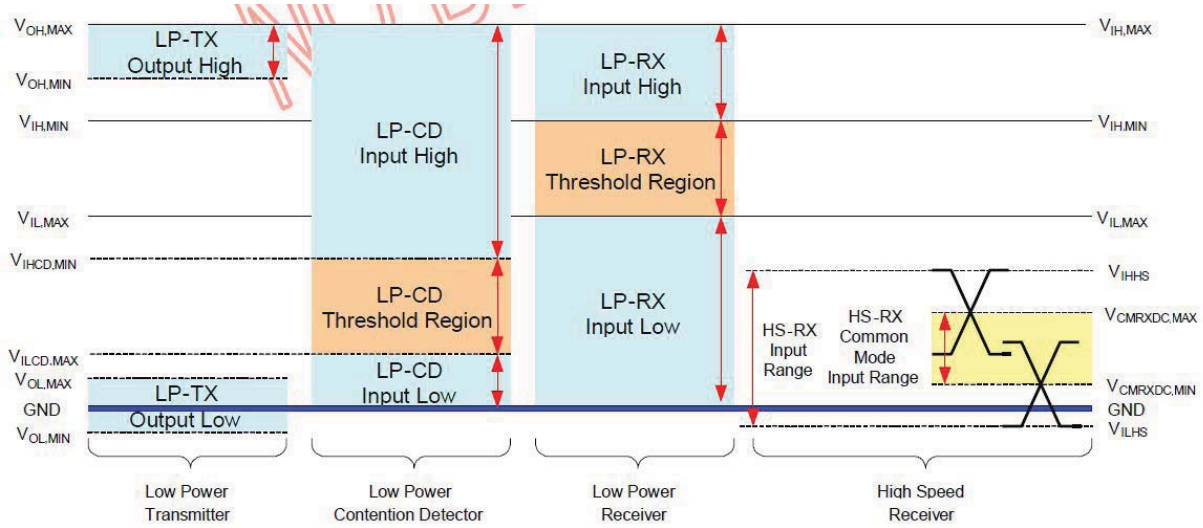
Light Bar Feedback
Channels

Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ºC and I_L = 20 mA(Per EA) until the brightness becomes $\leqq$ 50% of its original value.

4.4 MIPI DSI INPUT SIGNAL TIMING SPECIFICATIONS
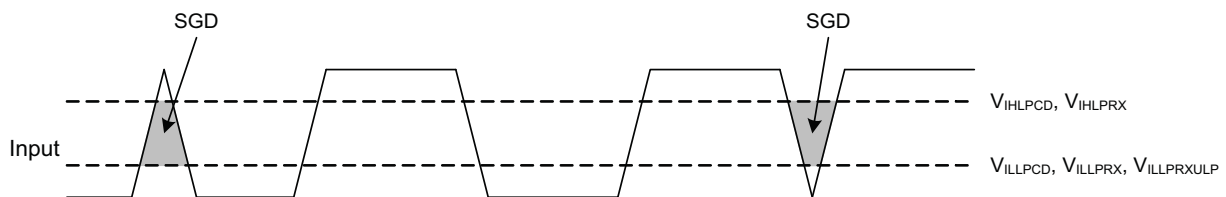

MIPI DC Diagram

4.4.1 DC Electrical Characteristic

4.4.1.1DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	µA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	µA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).

Note 2) DSI high speed is off.

Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

Spike/Glitch rejection-DSI

4.4.1.2 DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V$_{CMCLK}$ V$_{CMDATA}$	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	V$_{CMRCLKL}$ V$_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	V$_{CMRCLKM}$ V$_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V$_{THLCLK}$ V$_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V$_{THHCLK}$ V$_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V$_{ILHS}$	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V$_{IHHS}$	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R$_{TERM}$	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	V$_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C$_{TERM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 °C (to +85 °C no damage).
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without V$_{CMRCLKM}$ / V$_{CMRDATAM}$.
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.

Differential voltage range, termination resistor and Common mode voltage

4.4.2 AC Electrical Characteristics

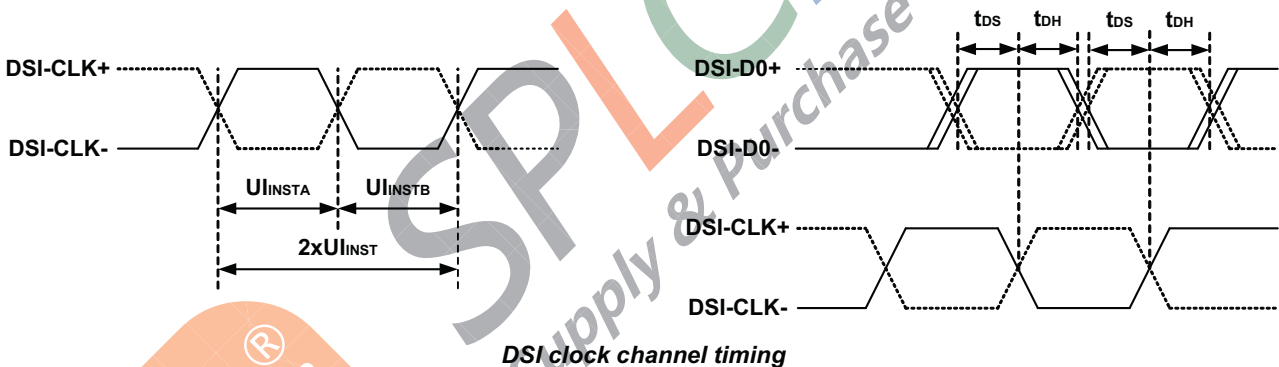### 4.4.2.1 MIPI DSI Timing Characteristics

4.4.2.1.1 High Speed Mode

*(**VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V** ,Ta = -30 to 70°C)*

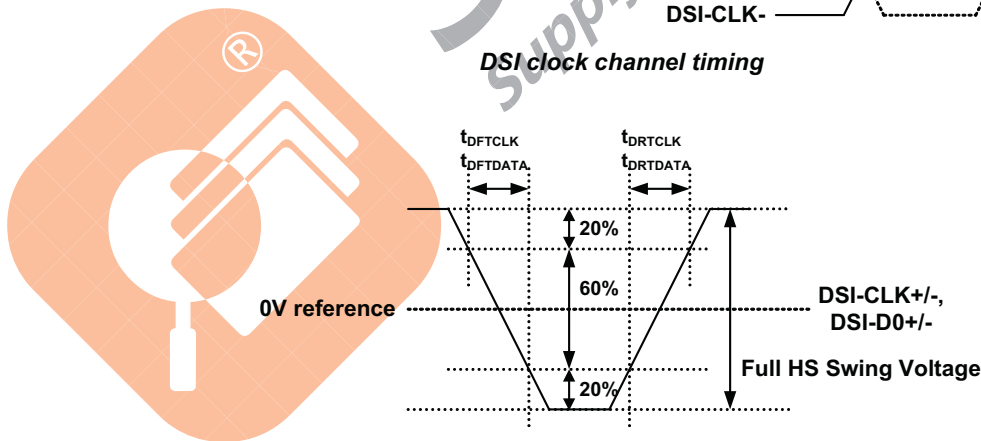| Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2 \times UI_{INST}$	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halves ($UI = UI_{INSTA} = UI_{INSTB}$)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.
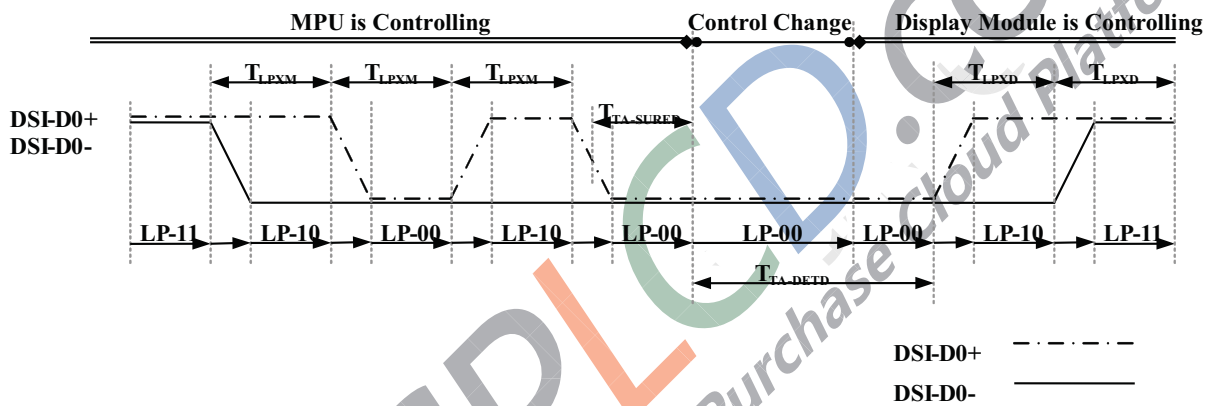

DSI clock channel timing
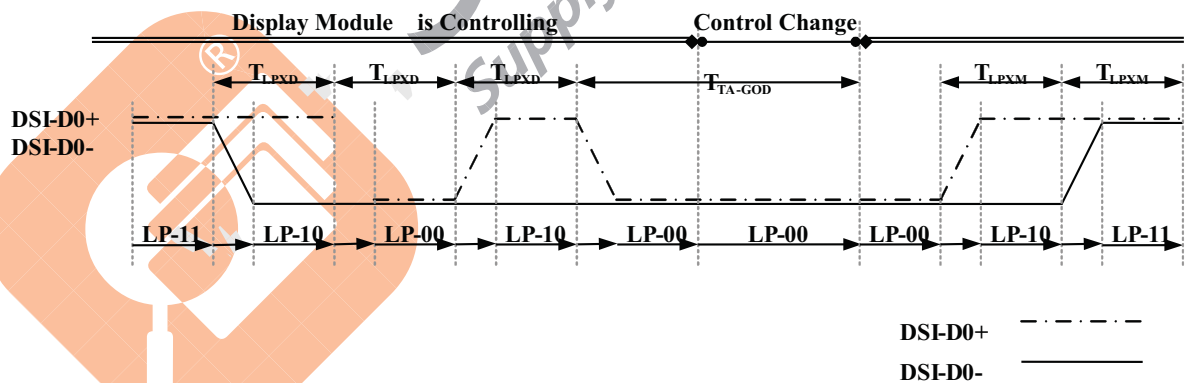

Rising and fall time on clock and data channel

4.4.2.1.2 Low Power Mode

*(**VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V** ,Ta = -30 to 70°C)*

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5 \times T_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4 \times T_{LPXD}$	-	-	ns	Output

Bus Turnaround (BAT) from MPU to display module Timing

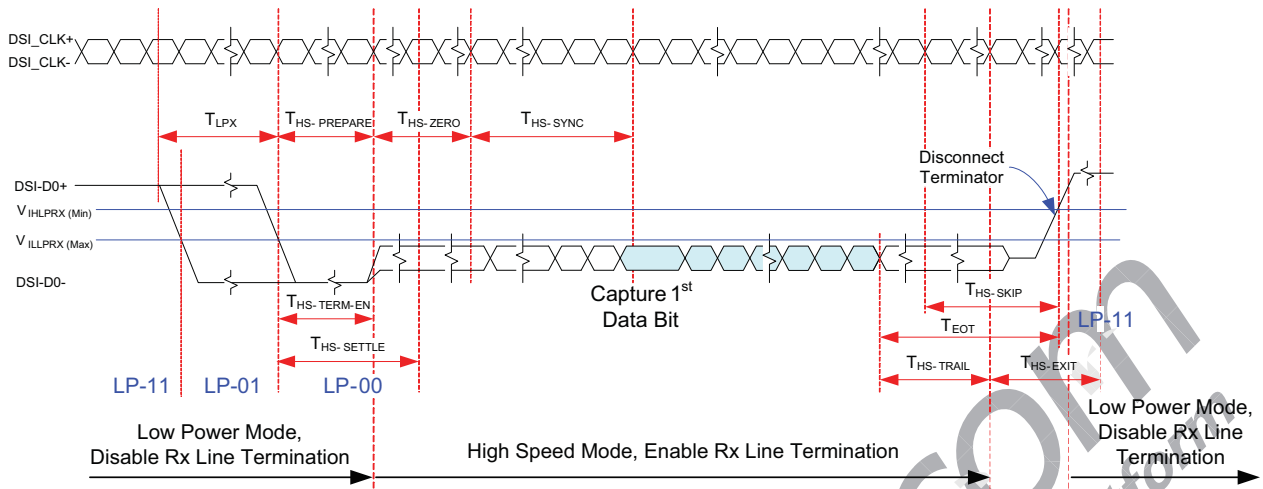*Bus Turnaround (BAT) from display module to MPU Timing*

4.4.2.1.3 DSI Bursts
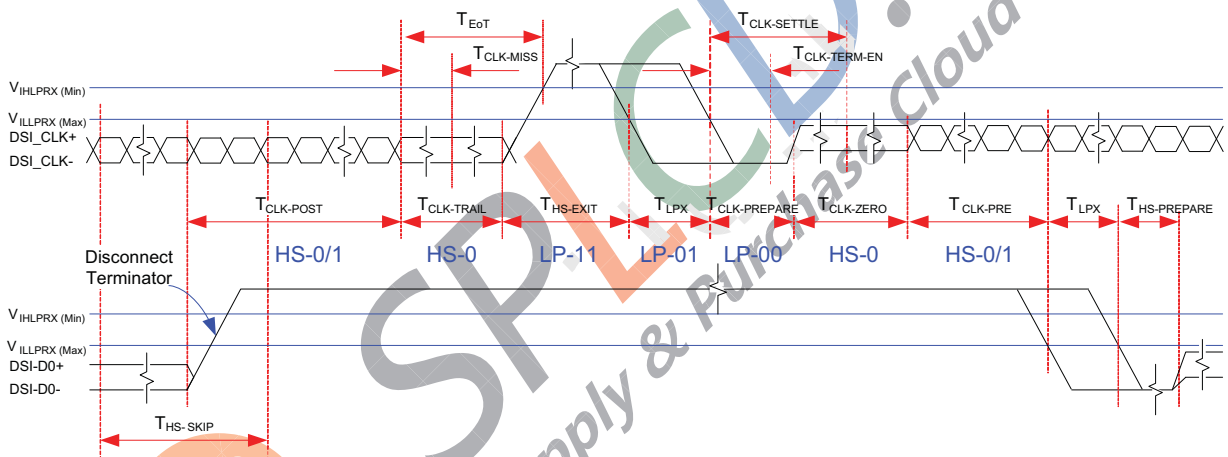
(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,Ta = -30 to 70°C)

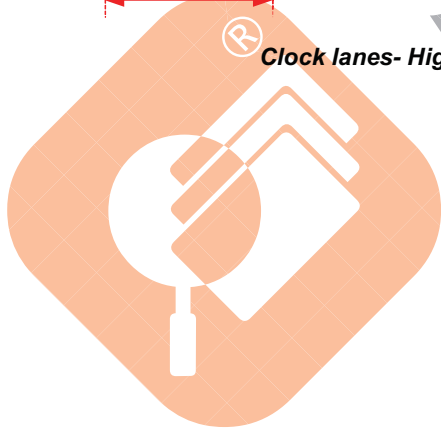| Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
		Low Power Mode to High Speed Mode Timing					
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
		High Speed Mode to Low Power Mode Timing					
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
		High Speed Mode to/from Low Power Mode Timing					
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.
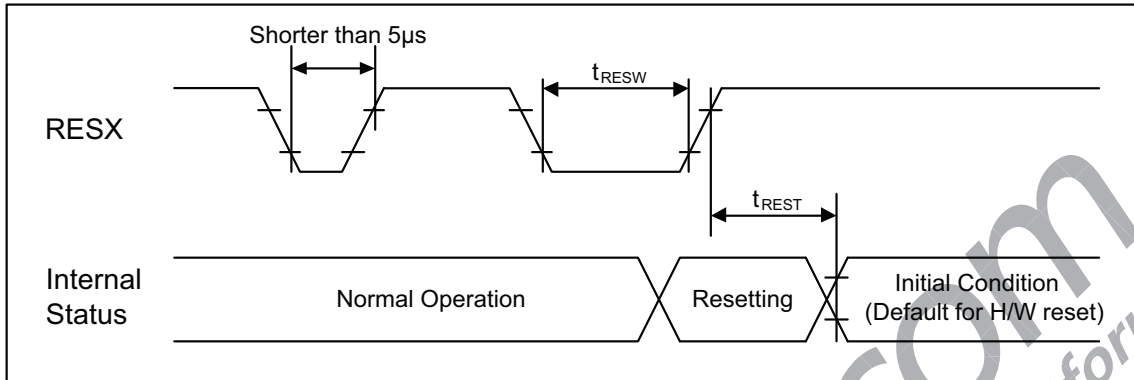
Data lanes-Low Power Mode to/from High Speed Mode Timing

Clock lanes- High Speed Mode to/from Low Power Mode Timing

4.4.2.2 Reset Input Timing

Reset input timing

(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,Ta = -30 to 70°C)

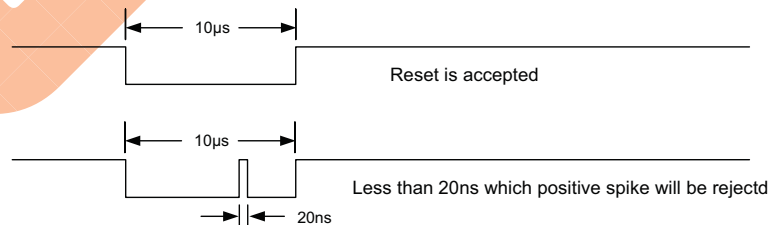| Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_{RESW}	Reset "L" pulse width (Note 1)	10	-	-	µs	
	t_{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.
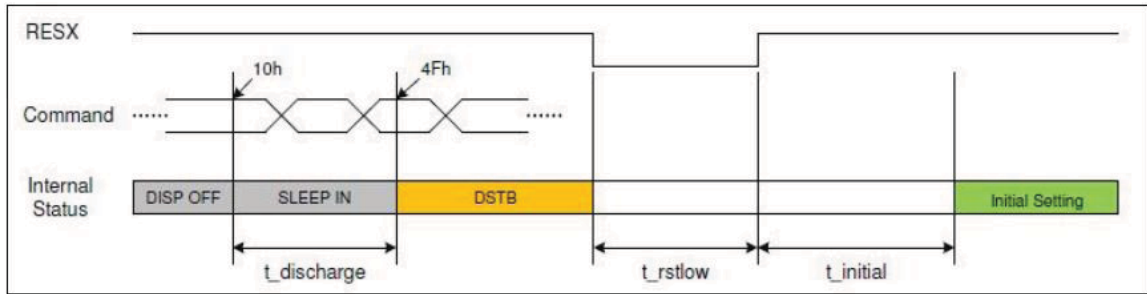
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:

Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

4.4.2.3 Deep Standby Mode Timing

(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,*Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_discharge	*Sleep in into DSTB delay time*	-	-	100	ms	
	t_rstlow	*Reset low pulse*	3	-	-	ms	
	t_initial	*Reset high to initial setting delay time*	-	-	120	ms	

Note 1) t_discharge *suggested delay time over 100ms.*

Note 2) t_initial *suggested delay time over 120ms.*

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4.5 MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

Note: The product only supports Video Mode operation.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

4.5.1 MIPI Lane Configuration

	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

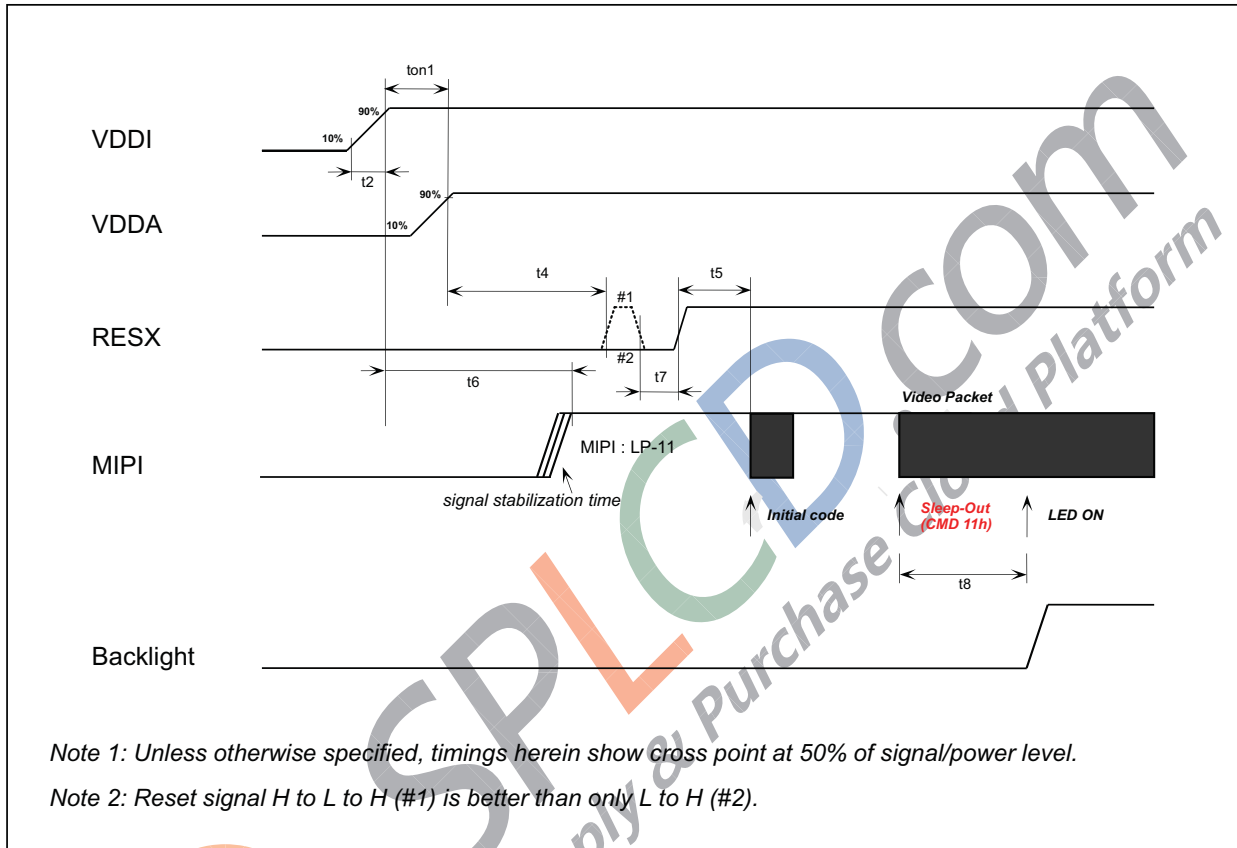The connection between host device and display module is as reference.

Note: Usually, we suggest host can use non-continuous clock mode & non-burst mode with sync events to

transmit the video stream to enhance ESD ability.

4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.
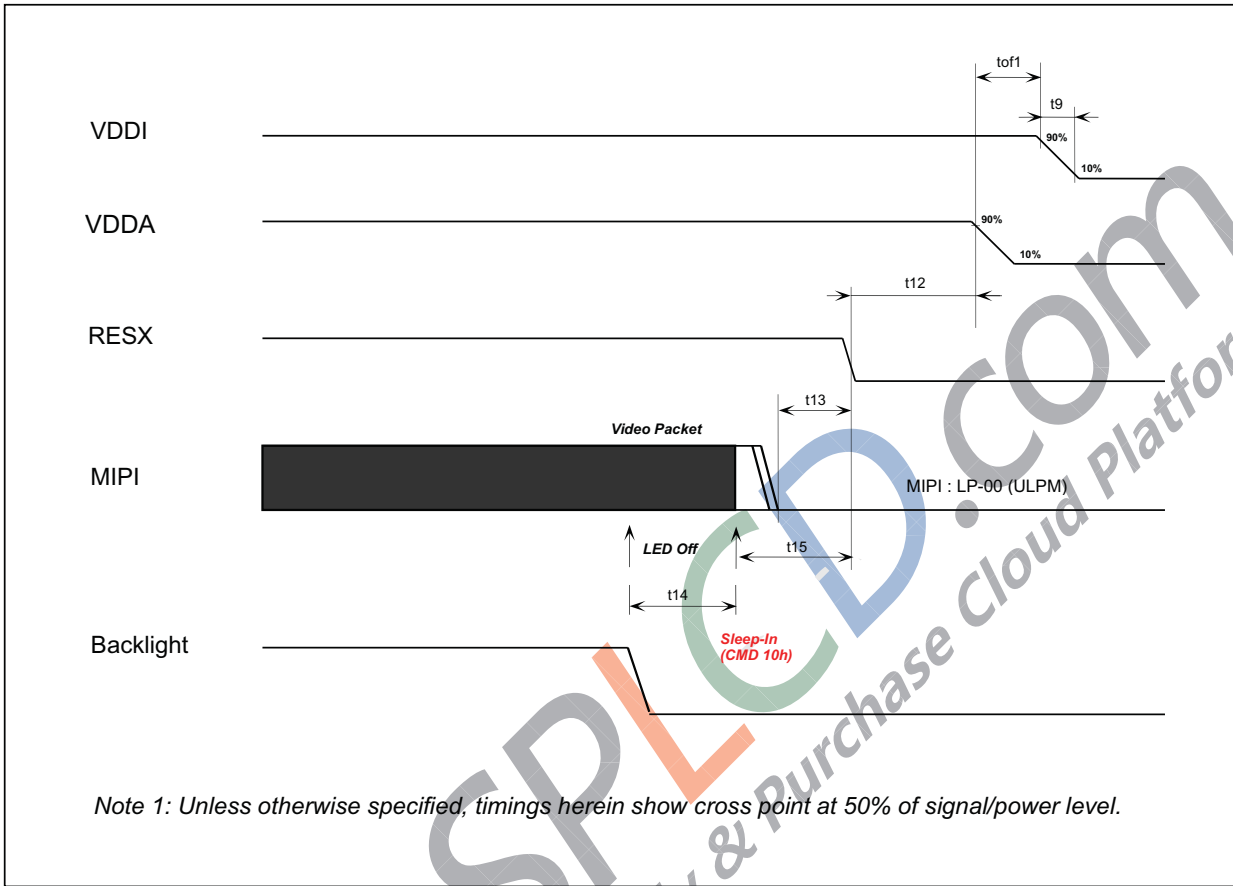
a. Power on:

VDDI=1.7~1.9V, VCI(VDDA)=3.0 to 3.6V,

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note 2: Reset signal H to L to H (#1) is better than only L to H (#2).

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0			ms	
t2		No limit		μs	
t4	40			ms	
t5	20			ms	
t6	0		t4	ms	
t7	10			μs	
t8	8			VS	Keep data more than 8 frames (VS)

b. Power off:

VDDI=1.7~1.9V, VCI=3.0 to 3.6V,

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150	-	-	ms	
tof1	0	-	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	100	-	-	ms	

PRODUCT SPECIFICATION

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VDDI	1.8	V
	VCI	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I$_L$	20	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		600	800	-	-	(2),(5),(7)
Response Time		T$_R$+T$_F$		-	20	25	ms / ms	(3),(7)
CP Luminance of White		L$_{CP}$	θx=0°, θY=0°	340	400	-	Cd/m²	(4),(6),(7)
	White	Wx	CS-2000 R=G=B=255 Gray scale	Typ − 0.03	0.313	Typ + 0.03	-	(4),(6),(7)
		Wy			0.329			
	Red	Rx			0.618			
		Ry			0.340			
	Green	Gx			0.344			
		Gy			0.600			
	Blue	Bx			0.160			
		By			0.074			
NTSC		%		55	60			(2),(5),(7)
White Variation	5 point		θx=0°, θY=0°	80			%	(5),(6),(7)
	13 point			67				
Flicker		dB				-30		(8)
Crosstalk		%				2		(9)
Viewing Angle	Horizontal	θx+	CR > 10	85	89	-	Deg.	(1),(5),(7)
		θx-		85	89			
	Vertical	θx+		85	89	-		
		θx-		85	89			

Note (1) Definition of Viewing Angle (θx, θy`

Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.
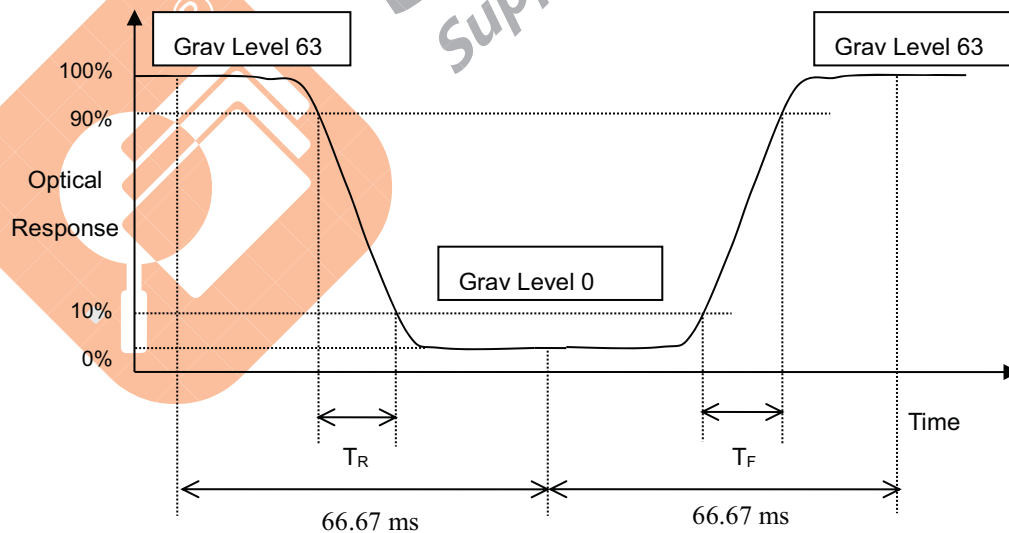
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):

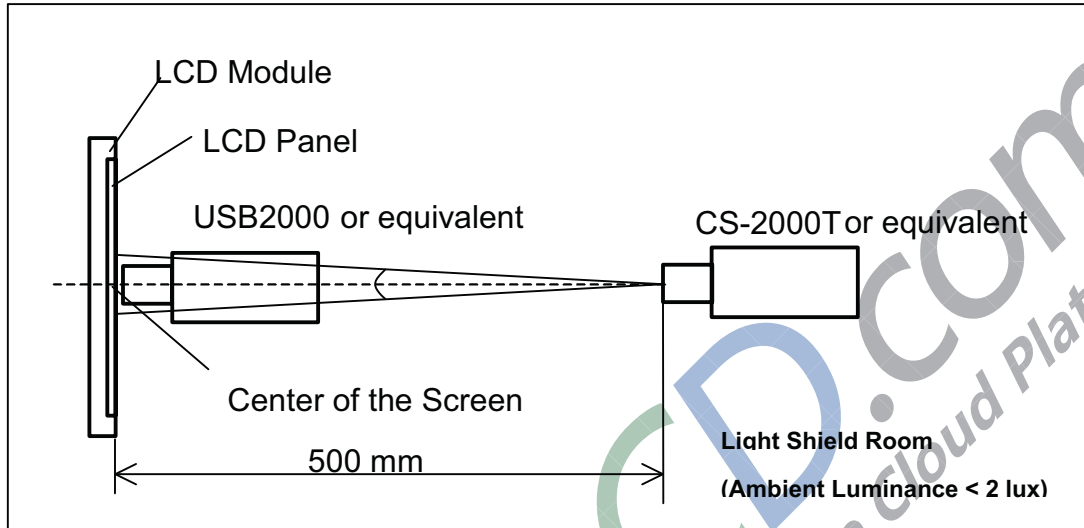
Note (4) Definition of Center Point Luminance of White (L_{CP}):

Measure the luminance of gray level 63 at center point

L_{CP} = L(5)

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5)   Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.
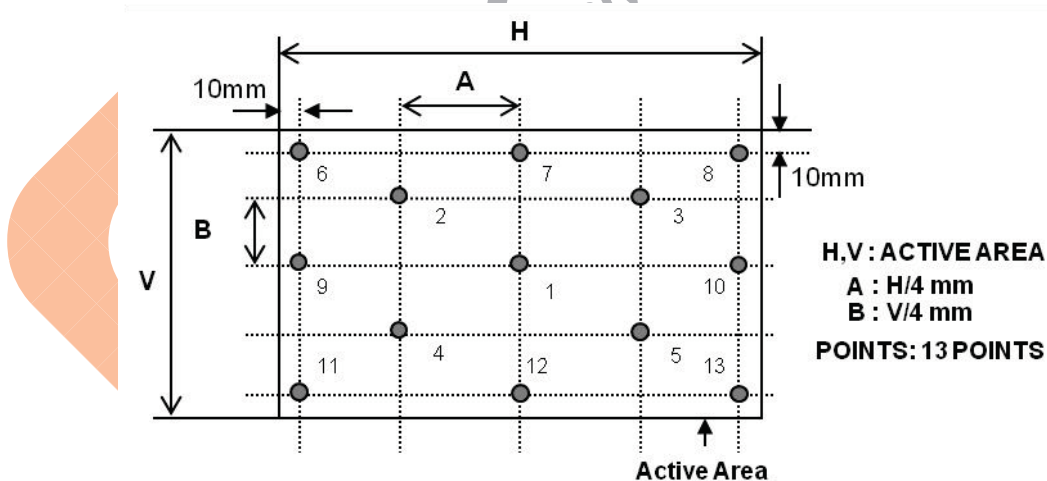

Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 13 points

δW_{9p} = {Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note(8) Flicker

No visual flicker will be allowed. The flicker level should be measured on GS127, The output signal is measured by Minolta CA210 immediately while Vcom is optimized. The flicker is

essentially a ratio of the Amplitude in the frequency spectrum at 30 Hz (A30) and 0 Hz (A0), i.e.,
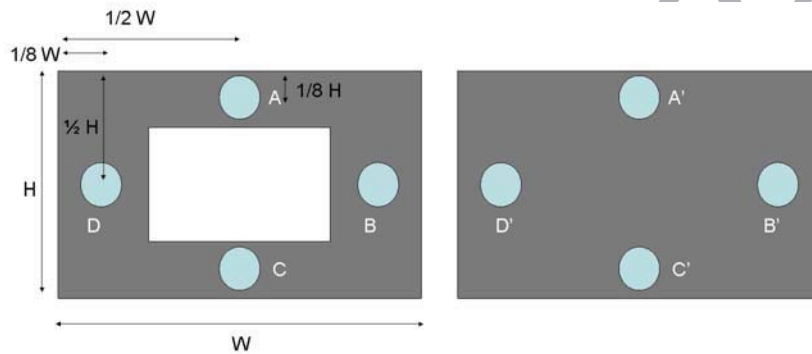
$$F = 20 \log (A30 / A0).$$

Note(9) Crosstalk

No visual cross-talk will be allowed. Two luminance values are measured at the same position (i.e. A and A'). The cross-talk, is defined as,

$$C(A, B, C, D)=| (L(A', B', C', D') - L(A, B, C, D))/L(A, B, C, D) | \cdot 100\%,$$

Where, L(A, B, C, D) = Luminance in Position A, B, C, D

L(A', B', C', D') = Luminance in Position A', B', C', D'

Crosstalk=max (C(A), C(B), C(C), C(D))

Background : GS 127

Center Pattern: GS 255, 50%(W) x 50%(H).

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	70ºC, 240 hours	
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour ⟷ 70℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	60ºC, 240 hours	(1) (2)
Low Temperature Operation Test	-10ºC, 240 hours	
High Temperature & High Humidity Storage Test	60ºC, RH 90%, 240hours	
ESD Test (Operation)	Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±12KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no mura and extra line defect.

(should be checked with 6% ND filter and within 45° viewing angle from vertical)
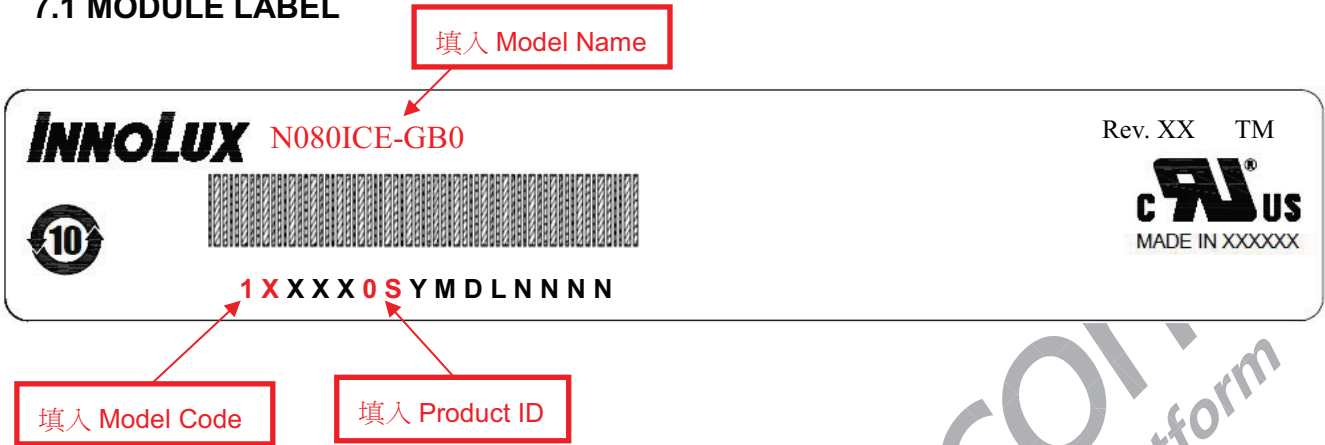
Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough

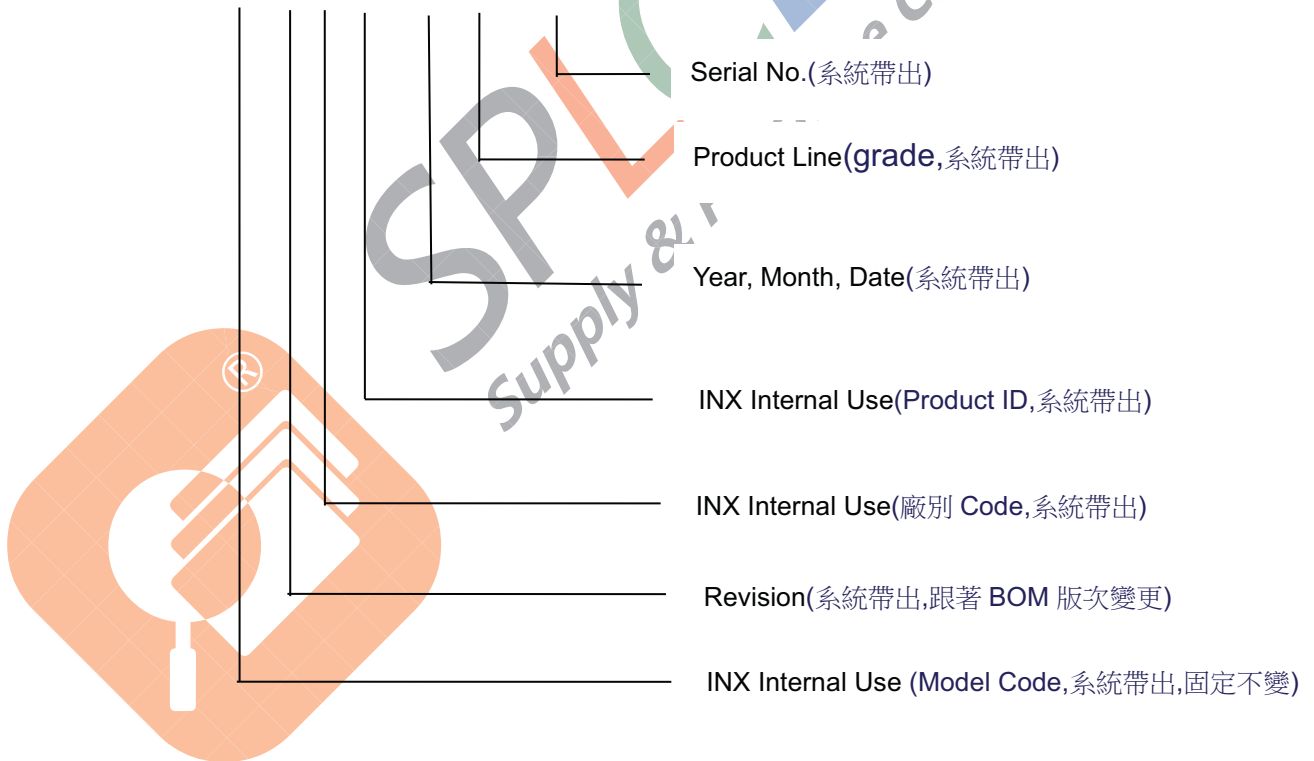so that the module would not be twisted or bent by the fixture.
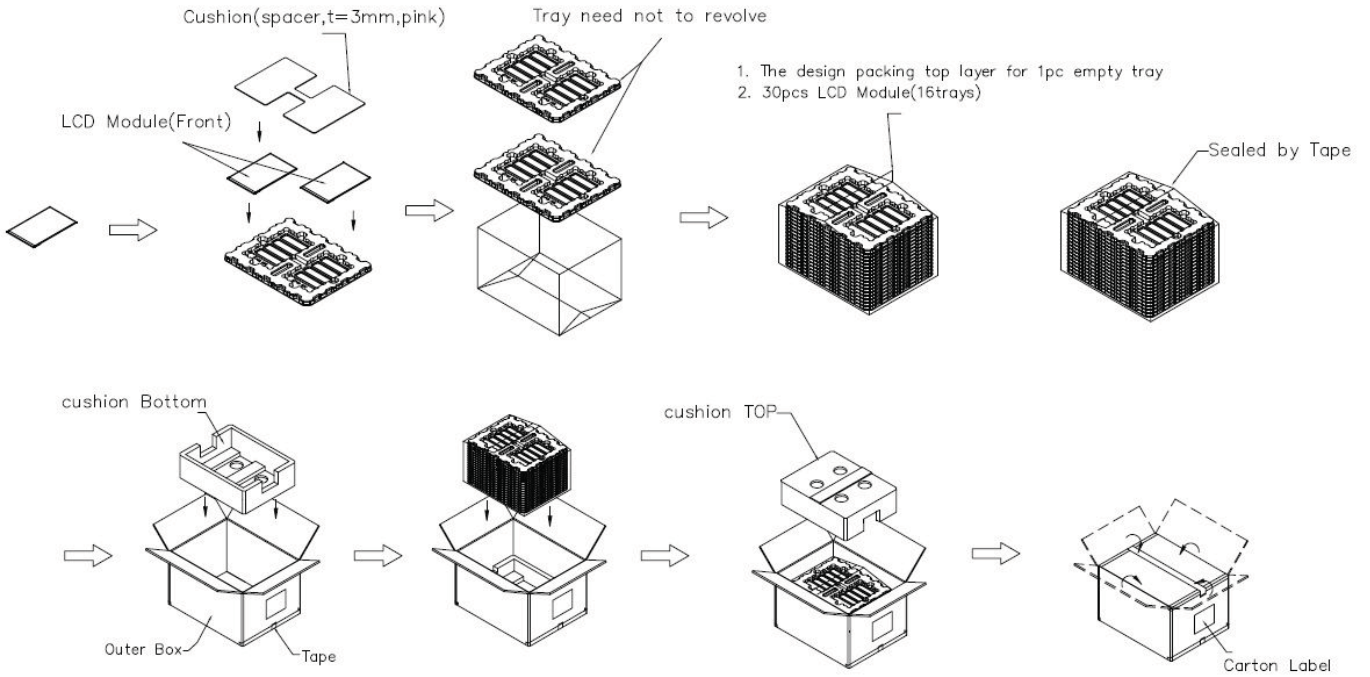
7. PACKING

7.1 MODULE LABEL

填入 Model Name

InnoLux N080ICE-GB0   Rev. XX   TM   MADE IN XXXXX

1 X X X X 0 S Y M D L N N N N

填入 Model Code

填入 Product ID

(a) Model Name: **N080ICE-GB0**

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X X Y M D L N N N N

- Serial No.(系統帶出)
- Product Line(grade,系統帶出)
- Year, Month, Date(系統帶出)
- INX Internal Use(Product ID,系統帶出)
- INX Internal Use(廠別 Code,系統帶出)
- Revision(系統帶出,跟著 BOM 版次變更)
- INX Internal Use (Model Code,系統帶出,固定不變)

(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL factory code stands for panel manufactured by Innolux satisfying UL requirement. Marking as follows rule :

"LEOO" for Ningbo NA
"VIRO" for Ningbo NB,NC
"CANO" for Ningbo ND
"GEMN" for Tainan LCM1,LCM4
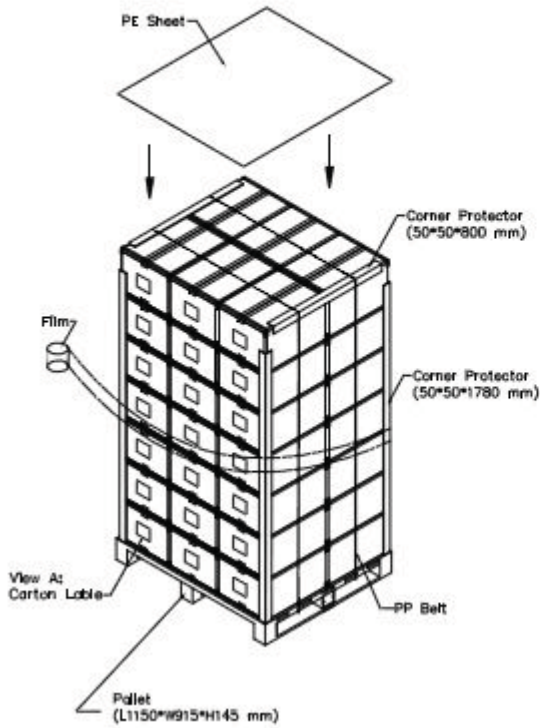"   " for Tainan J001

7.2 CARTON

(1) Box Dimensions : 435(L)*350(W)*275(H)
(2) 30 Modules/Carton

Figure. 7-1 Packing method

7.3 PALLET
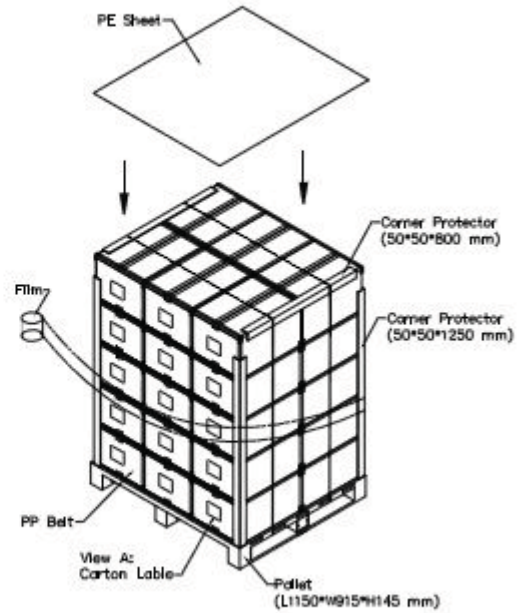
Sea & Land Transportation

Air Transportation

Figure. 7-2 Packing method
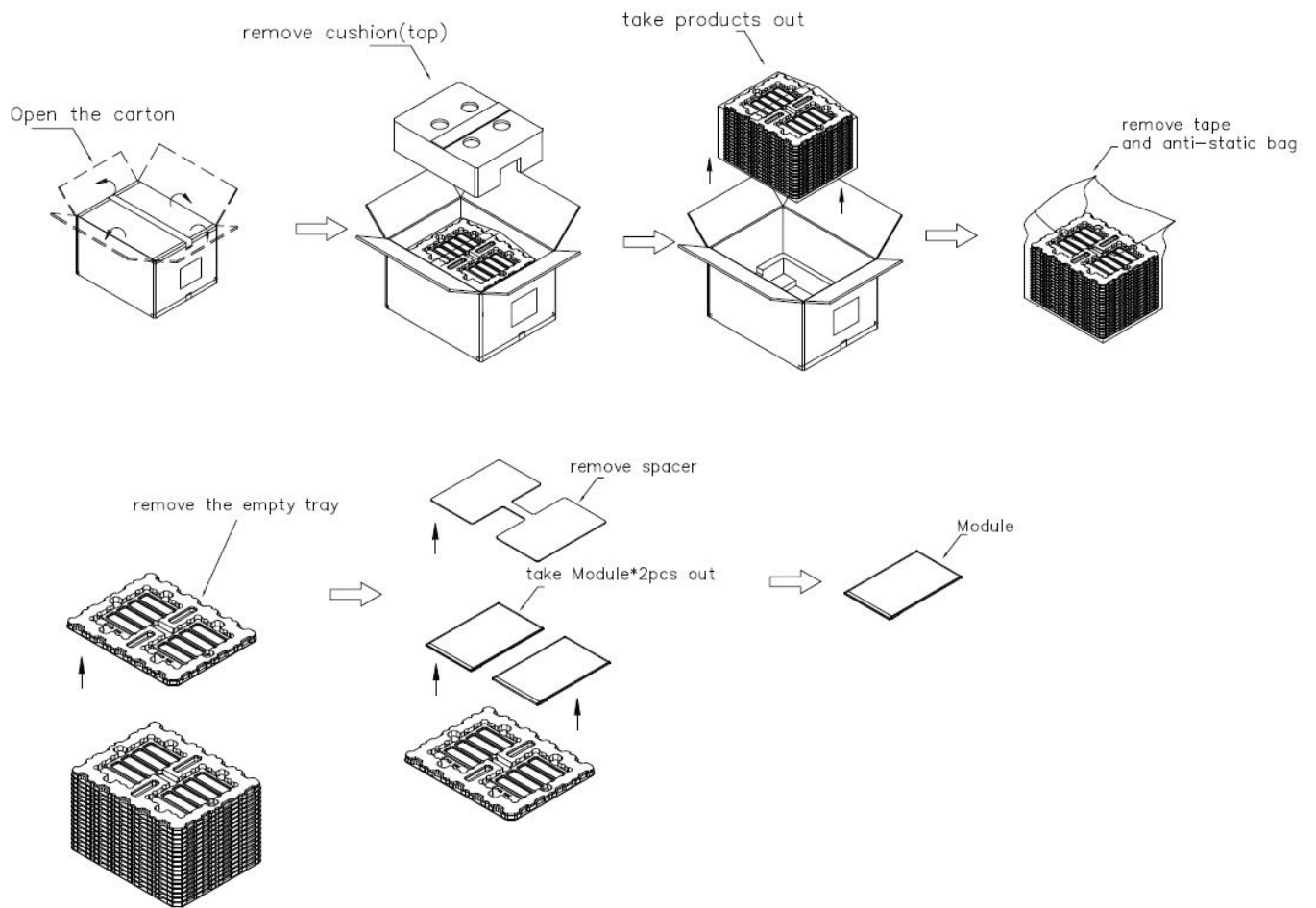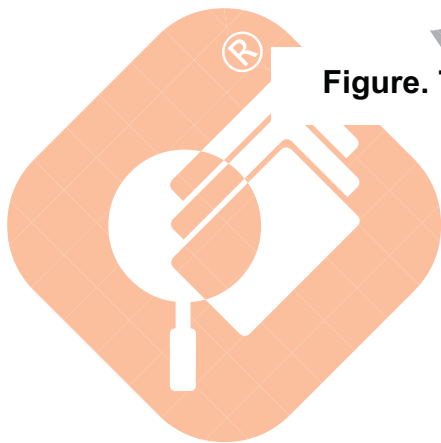
7.4 Un-Packing

Figure. 7-3 Un-Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

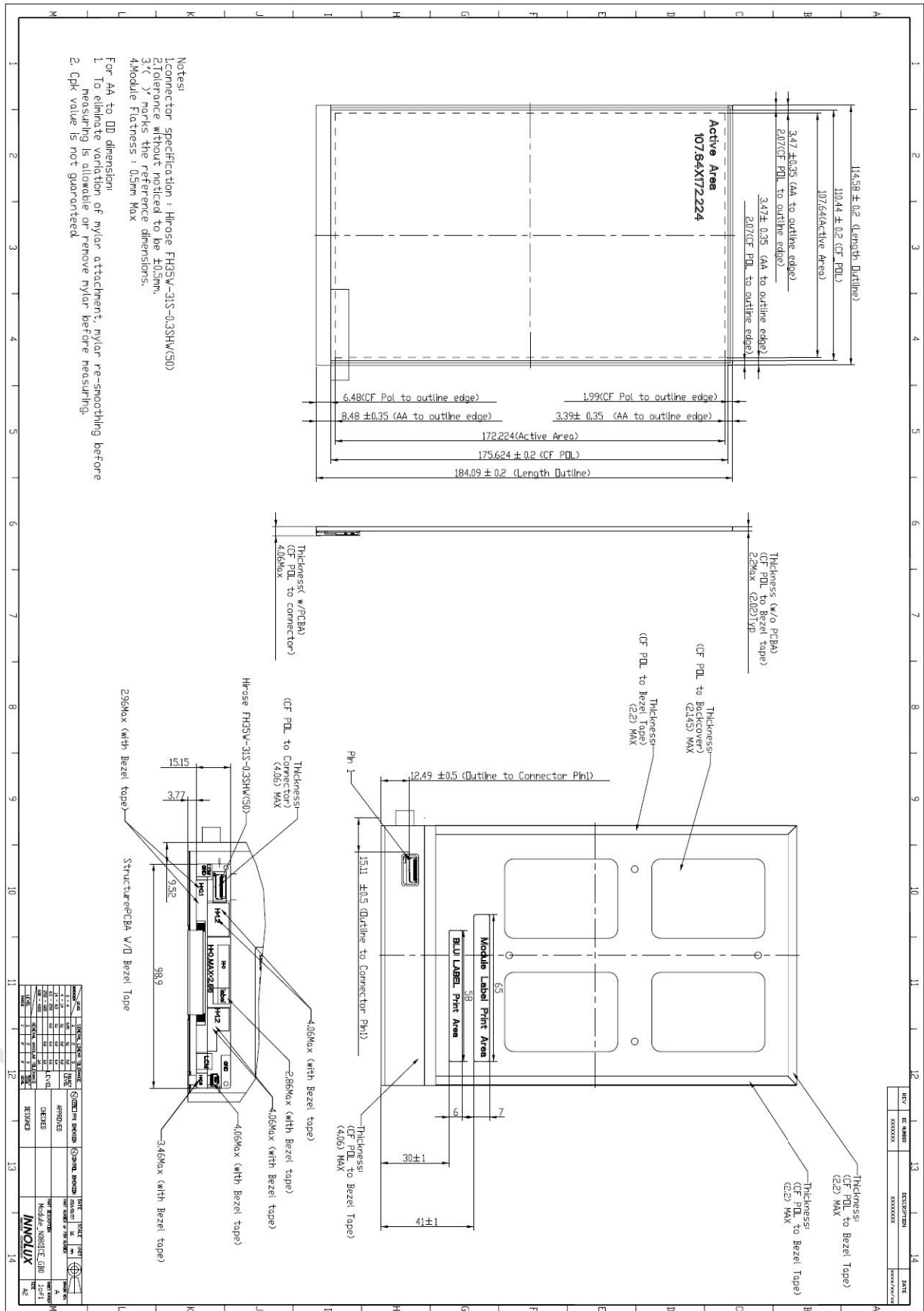(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the backlight unit.

Appendix. OUTLINE DRAWING (Label position will be updated as requirement)

Appendix II. NT35521 REGISTER SETTING

//========== Internal setting ==========
REGW 0xFF,0xAA,0x55,0xA5,0x80

REGW 0x6F,0x11,0x00
REGW 0xF7,0x20,0x00
REGW 0x6F,0x06
REGW 0xF7,0xA0
REGW 0x6F,0x19
REGW 0xF7,0x12

//========== page0 relative ==========
REGW 0xF0,0x55,0xAA,0x52,0x08,0x00
REGW   0xC8, 0x00

REGW 0xB1,0x6C,0x01

REGW 0xB6,0x08

REGW 0x6F,0x02
REGW 0xB8,0x08

REGW 0xBB,0x74,0x44

REGW 0xBC,0x00,0x00

REGW   0xBD, 0x02,0xB0,0x0C,0x0A,0x00

//========== page1 relative ==========
REGW 0xF0,0x55,0xAA,0x52,0x08,0x01

REGW 0xB0,0x05,0x05
REGW 0xB1,0x05,0x05

REGW 0xBC,0x90,0x01
REGW 0xBD,0x90,0x01

REGW 0xCA,0x00

REGW 0xC0,0x04

REGW 0xB3,0x37,0x37
REGW 0xB4,0x19,0x19

REGW 0xB9,0x44,0x44
REGW 0xBA,0x24,0x24

//========== page2 relative ==========
REGW 0xF0,0x55,0xAA,0x52,0x08,0x02

REGW 0xEE,0x02
REGW 0xEF,0x09,0x06,0x15,0x18

regw 0xB0,0x00,0x00,0x00,0x19,0x00,0x31
regw 0x6F,0x06
regw 0xB0,0x00,0x4B,0x00,0x63,0x00,0x95
regw 0x6F,0x0C
regw 0xB0,0x00,0xB4,0x00,0xF3
regw 0xB1,0x01,0x24,0x01,0x70,0x01,0xA6
regw 0x6F,0x06
regw 0xB1,0x01,0xFC,0x02,0x49,0x02,0x4C
regw 0x6F,0x0C
regw 0xB1,0x02,0x96,0x02,0xEC
regw 0xB2,0x03,0x1D,0x03,0x5A,0x03,0x81
regw 0x6F,0x06
regw 0xB2,0x03,0xA2,0x03,0xB6,0x03,0xCB
regw 0x6F,0x0C
regw 0xB2,0x03,0xD9,0x03,0xE8
regw 0xB3,0x03,0xF7,0x03,0xFF

regw 0xBC,0x00,0x00,0x00,0x19,0x00,0x31
regw 0x6F,0x06
regw 0xBC,0x00,0x4B,0x00,0x63,0x00,0x95

regw 0x6F,0x0C

regw 0xBC,0x00,0xB4,0x00,0xF3

regw 0xBD,0x01,0x24,0x01,0x70,0x01,0xA6

regw 0x6F,0x06

regw 0xBD,0x01,0xFC,0x02,0x49,0x02,0x4C

regw 0x6F,0x0C

regw 0xBD,0x02,0x96,0x02,0xEC

regw 0xBE,0x03,0x1D,0x03,0x5A,0x03,0x81

regw 0x6F,0x06

regw 0xBE,0x03,0xA2,0x03,0xB6,0x03,0xCB

regw 0x6F,0x0C

regw 0xBE,0x03,0xD9,0x03,0xE8

regw 0xBF,0x03,0xF7,0x03,0xFF

// PAGE6 : GOUT Mapping, VGLO select

regw   0xF0, 0x55,0xAA,0x52,0x08,0x06

regw   0xB0, 0x00,0x10

regw   0xB1, 0x12,0x14

regw   0xB2, 0x16,0x18

regw   0xB3, 0x1A,0x29

regw   0xB4, 0x2A,0x08

regw   0xB5, 0x31,0x31

regw   0xB6, 0x31,0x31

regw   0xB7, 0x31,0x31

regw   0xB8, 0x31,0x0A

regw   0xB9, 0x31,0x31

regw   0xBA, 0x31,0x31

regw   0xBB, 0x0B,0x31

regw   0xBC, 0x31,0x31

regw   0xBD, 0x31,0x31

regw   0xBE, 0x31,0x31

regw   0xBF, 0x09,0x2A

regw   0xC0, 0x29,0x1B

regw   0xC1, 0x19,0x17

regw   0xC2, 0x15,0x13

regw   0xC3, 0x11,0x01

regw   0xE5, 0x31,0x31

```
regw   0xC4, 0x09,0x1B
regw   0xC5, 0x19,0x17
regw   0xC6, 0x15,0x13
regw   0xC7, 0x11,0x29
regw   0xC8, 0x2A,0x01
regw   0xC9, 0x31,0x31
regw   0xCA, 0x31,0x31
regw   0xCB, 0x31,0x31
regw   0xCC, 0x31,0x0B
regw   0xCD, 0x31,0x31
regw   0xCE, 0x31,0x31
regw   0xCF, 0x0A,0x31
regw   0xD0, 0x31,0x31
regw   0xD1, 0x31,0x31
regw   0xD2, 0x31,0x31
regw   0xD3, 0x00,0x2A
regw   0xD4, 0x29,0x10
regw   0xD5, 0x12,0x14
regw   0xD6, 0x16,0x18
regw   0xD7, 0x1A,0x08
regw   0xE6, 0x31,0x31
regw   0xD8, 0x00,0x00,0x00,0x54,0x00
regw   0xD9, 0x00,0x15,0x00,0x00,0x00
regw   0xE7, 0x00

// PAGE3 :
regw   0xF0, 0x55,0xAA,0x52,0x08,0x03
regw   0xB0, 0x20,0x00
regw   0xB1, 0x20,0x00
regw   0xB2, 0x05,0x00,0x00,0x00,0x00

regw   0xB6, 0x05,0x00,0x00,0x00,0x00
regw   0xB7, 0x05,0x00,0x00,0x00,0x00

regw   0xBA, 0x57,0x00,0x00,0x00,0x00
regw   0xBB, 0x57,0x00,0x00,0x00,0x00
```

```
regw   0xC0, 0x00,0x00,0x00,0x00
regw   0xC1, 0x00,0x00,0x00,0x00

regw   0xC4, 0x60
regw   0xC5, 0x40

// PAGE5 :
regw   0xF0, 0x55,0xAA,0x52,0x08,0x05
regw   0xBD, 0x03,0x01,0x03,0x03,0x03
regw   0xB0, 0x17,0x06
regw   0xB1, 0x17,0x06
regw   0xB2, 0x17,0x06
regw   0xB3, 0x17,0x06
regw   0xB4, 0x17,0x06
regw   0xB5, 0x17,0x06

regw   0xB8, 0x00
regw   0xB9, 0x00
regw   0xBA, 0x00
regw   0xBB, 0x02
regw   0xBC, 0x00

regw   0xC0, 0x07

regw   0xC4, 0x80
regw   0xC5, 0xA4

regw   0xC8, 0x05,0x30
regw   0xC9, 0x01,0x31

regw   0xCC, 0x00,0x00,0x3C
regw   0xCD, 0x00,0x00,0x3C

regw   0xD1, 0x00,0x04,0xFD,0x07,0x10
regw   0xD2, 0x00,0x05,0x02,0x07,0x10

regw   0xE5, 0x06
```

```
regw   0xE6, 0x06
regw   0xE7, 0x06
regw   0xE8, 0x06
regw   0xE9, 0x06
regw   0xEA, 0x06


regw   0xED, 0x30


REGW 0x6F,0x11
REGW 0xF3,0x01


regw   0x35
regw   0x11
regw   0x29
```