

# 8Mb Ultra-Low Power Asynchronous CMOS SRAM

512K × 16 bit

## Overview

The N08L163WC2C is an integrated memory device containing a 8 Mbit Static Random Access Memory organized as 524,288 words by 16 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with two chip enable ( $\overline{CE1}$  and  $\overline{CE2}$ ) controls and output enable ( $\overline{OE}$ ) to allow for easy memory expansion. Byte controls ( $\overline{UB}$  and  $\overline{LB}$ ) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The N08L163WC2C is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to +85°C and is available in JEDEC standard packages compatible with other standard 512Kb x 16 SRAMs

## Features

- **Single Wide Power Supply Range**  
2.2 to 3.6 Volts
- **Very low standby current**  
2.0µA at 3.0V (Typical)
- **Very low operating current**  
1.5mA at 3.0V and 1µs(Typical)
- **Simple memory control**  
Dual Chip Enables ( $\overline{CE1}$  and  $\overline{CE2}$ )  
Byte control for independent byte operation  
Output Enable ( $\overline{OE}$ ) for memory expansion
- **Low voltage data retention**  
V<sub>CC</sub> = 1.5V
- **Very fast output enable access time**  
25ns  $\overline{OE}$  access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **Ultra Low Power Sort Available**

## Product Family

Part Number	Package Type	Operating Temperature	Power Supply (V <sub>CC</sub> )	Speed	Standby Current (I <sub>SB</sub> ), Typical	Operating Current (I <sub>CC</sub> ), Typical
N08L163WC2CZ1	VFBGA Pb-Free	-40°C to +85°C	2.2V - 3.6V	55ns	2 µA	1.5 mA @ 1MHz

## Pin Configuration

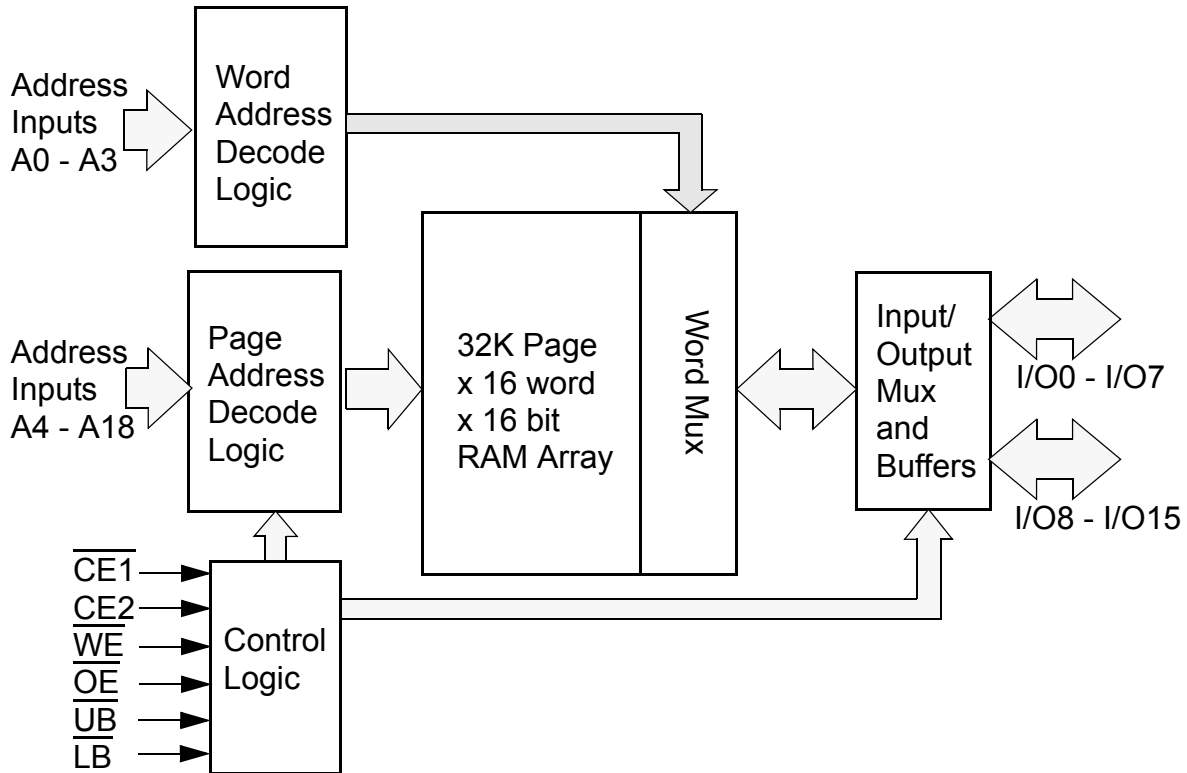
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	CE2
B	I/O <sub>8</sub>	$\overline{UB}$	A <sub>3</sub>	A <sub>4</sub>	$\overline{CE1}$	I/O <sub>0</sub>
C	I/O <sub>9</sub>	I/O <sub>10</sub>	A <sub>5</sub>	A <sub>6</sub>	I/O <sub>1</sub>	I/O <sub>2</sub>
D	V <sub>SS</sub>	I/O <sub>11</sub>	A <sub>17</sub>	A <sub>7</sub>	I/O <sub>3</sub>	V <sub>CC</sub>
E	V <sub>CC</sub>	I/O <sub>12</sub>	DNU	A <sub>16</sub>	I/O <sub>4</sub>	V <sub>SS</sub>
F	I/O <sub>14</sub>	I/O <sub>13</sub>	A <sub>14</sub>	A <sub>15</sub>	I/O <sub>5</sub>	I/O <sub>6</sub>
G	I/O <sub>15</sub>	NC	A <sub>12</sub>	A <sub>13</sub>	$\overline{WE}$	I/O <sub>7</sub>
H	A <sub>18</sub>	A <sub>8</sub>	A <sub>9</sub>	A <sub>10</sub>	A <sub>11</sub>	NC

48 Pin VFBGA (top)  
6 x 8 mm

## Pin Descriptions

Pin Name	Pin Function
A <sub>0</sub> -A <sub>18</sub>	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$ , $\overline{CE2}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O <sub>0</sub> -I/O <sub>15</sub>	Data Inputs/Outputs
V <sub>CC</sub>	Power
V <sub>SS</sub>	Ground
NC	Not Connected

## Functional Block Diagram



## Functional Description

$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$I/O_0 - I/O_{15}^1$	MODE	POWER
H	X	X	X	X	X	High Z	Standby <sup>2</sup>	Standby
X	L	X	X	X	X	High Z	Standby <sup>2</sup>	Standby
X	X	X	X	H	H	High Z	Standby <sup>2</sup>	Standby
L	H	L	X <sup>3</sup>	L <sup>1</sup>	L <sup>1</sup>	Data In	Write <sup>3</sup>	Active
L	H	H	L	L <sup>1</sup>	L <sup>1</sup>	Data Out	Read	Active
L	H	H	H	L <sup>1</sup>	L <sup>1</sup>	High Z	Active	Active

1. When  $\overline{UB}$  and  $\overline{LB}$  are in select mode (low),  $I/O_0 - I/O_{15}$  are affected as shown. When  $\overline{LB}$  only is in the select mode only  $I/O_0 - I/O_7$  are affected as shown. When  $\overline{UB}$  is in the select mode only  $I/O_8 - I/O_{15}$  are affected as shown.

2. When the device is in standby mode, control inputs ( $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{UB}$ , and  $\overline{LB}$ ), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When  $\overline{WE}$  is invoked, the  $\overline{OE}$  input is internally disabled and has no effect on the circuit.

## Capacitance<sup>1</sup>

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0V, f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$		10	pF
I/O Capacitance	$C_{I/O}$	$V_{IN} = 0V, f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$		10	pF

1. These parameters are verified in device characterization and are not 100% tested

**Absolute Maximum Ratings**

Item	Symbol	Rating	Unit
Voltage on any pin relative to $V_{SS}$	$V_{IN,OUT}$	-0.3 to $V_{CC}+0.3$	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-0.3 to 4.5	V
Power Dissipation	$P_D$	500	mW
Storage Temperature	$T_{STG}$	-65 to 150	°C
Operating Temperature	$T_A$	-40 to +85	°C
Soldering Temperature and Time	$T_{SOLDER}$	260°C, 10sec	°C

Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Operating Characteristics (Over Specified Temperature Range)**

Item	Symbol	Test Conditions	Min.	Typ <sup>1</sup>	Max	Unit	
Supply Voltage	$V_{CC}$		2.2	3.0	3.6	V	
Data Retention Voltage	$V_{DR}$	Chip Disabled	1.5			V	
Input High Voltage	$V_{IH}$	$V_{CC} = 2.2V$ to $2.7V$	1.8		$V_{CC}+0.3$	V	
		$V_{CC} = 2.7V$ to $3.6V$	2.2		$V_{CC}+0.3$		
Input Low Voltage	$V_{IL}$	$V_{CC} = 2.2V$ to $2.7V$	-0.3		0.6	V	
		$V_{CC} = 2.7V$ to $3.6V$	-0.3		0.8		
Output High Voltage	$V_{OH}$	$I_{OH} = -0.1mA$ , $V_{CC} = 2.2V$	2.0			V	
		$I_{OH} = -1.0mA$ , $V_{CC} = 2.7V$	2.4				
Output Low Voltage	$V_{OL}$	$I_{OL} = 0.1mA$ , $V_{CC} = 2.2V$			0.4	V	
		$I_{OL} = 2.1mA$ , $V_{CC} = 2.7V$			0.4		
Input Leakage Current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$	-1		1	μA	
Output Leakage Current	$I_{LO}$	$\overline{OE} = V_{IH}$ or Chip Disabled	-1		1	μA	
Read/Write Operating Supply Current @ 1 μs Cycle Time <sup>2</sup>	$I_{CC1}$	$V_{CC}=3.6V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OUT} = 0$			1.5	3	mA
			-L		1.5	3	
Read/Write Operating Supply Current @ fmax	$I_{CC2}$	$V_{CC}=3.6V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OUT} = 0$			12.0	20.0	mA
			-L		12.0	15.0	
Maximum Standby Current	$I_{SB1}$	$V_{IN} = V_{CC}$ or 0V Chip Disabled $t_A = 85^\circ C$ , $V_{CC} = 3.6V$			2.0	20	μA
			-L		2.0	8	
Maximum Data Retention Current	$I_{DR}$	$V_{CC} = 1.5V$ , $CE \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$				10	μA
			-L			4	

1. Typical values are measured at  $V_{CC}=V_{CC}$  Typ.,  $T_A=25^\circ C$  and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

## Timing Test Conditions

Item	
Input Pulse Level	0.1V <sub>CC</sub> to 0.9 V <sub>CC</sub>
Input Rise and Fall Time	1V/ns
Input and Output Timing Reference Levels	0.5 V <sub>CC</sub>
Output Load	CL = 50pF
Operating Temperature	-40 to +85 °C

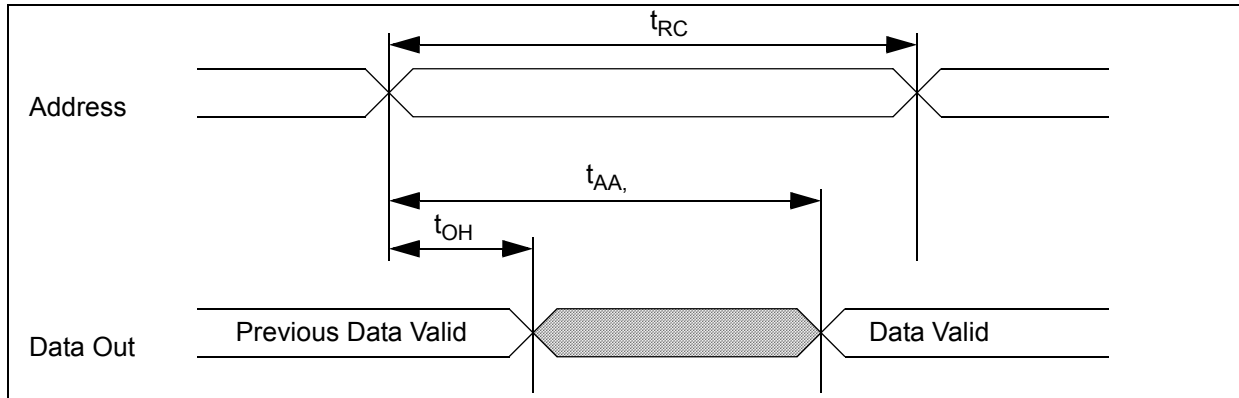
## Timing

Item	Symbol	55		Units
		Min	Max	
Read Cycle Time	t <sub>RC</sub>	55		ns
Address Access Time (Random Access)	t <sub>AA</sub>		55	ns
Chip Enable to Valid Output	t <sub>CO</sub>		55	ns
Output Enable to Valid Output	t <sub>OE</sub>		25	ns
Byte Select to Valid Output	t <sub>LB</sub> , t <sub>UB</sub>		55	ns
Chip Enable to Low-Z output	t <sub>LZ</sub>	10		ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	5		ns
Byte Select to Low-Z Output	t <sub>LBZ</sub> , t <sub>UBZ</sub>	10		ns
Chip Disable to High-Z Output	t <sub>HZ</sub>		20	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>		20	ns
Byte Select Disable to High-Z Output	t <sub>LBHZ</sub> , t <sub>UBHZ</sub>		20	ns
Output Hold from Address Change	t <sub>OH</sub>	10		ns
Write Cycle Time	t <sub>WC</sub>	55		ns
Chip Enable to End of Write	t <sub>CW</sub>	40		ns
Address Valid to End of Write	t <sub>AW</sub>	40		ns
Byte Select to End of Write	t <sub>LBW</sub> , t <sub>UBW</sub>	40		ns
Write Pulse Width	t <sub>WP</sub>	40		ns
Address Setup Time	t <sub>AS</sub>	0		ns
Write Recovery Time	t <sub>WR</sub>	0		ns
Write to High-Z Output	t <sub>WHZ</sub>		20	ns
Data to Write Time Overlap	t <sub>DW</sub>	25		ns
Data Hold from Write Time	t <sub>DH</sub>	0		ns
End Write to Low-Z Output	t <sub>OW</sub>	10		ns

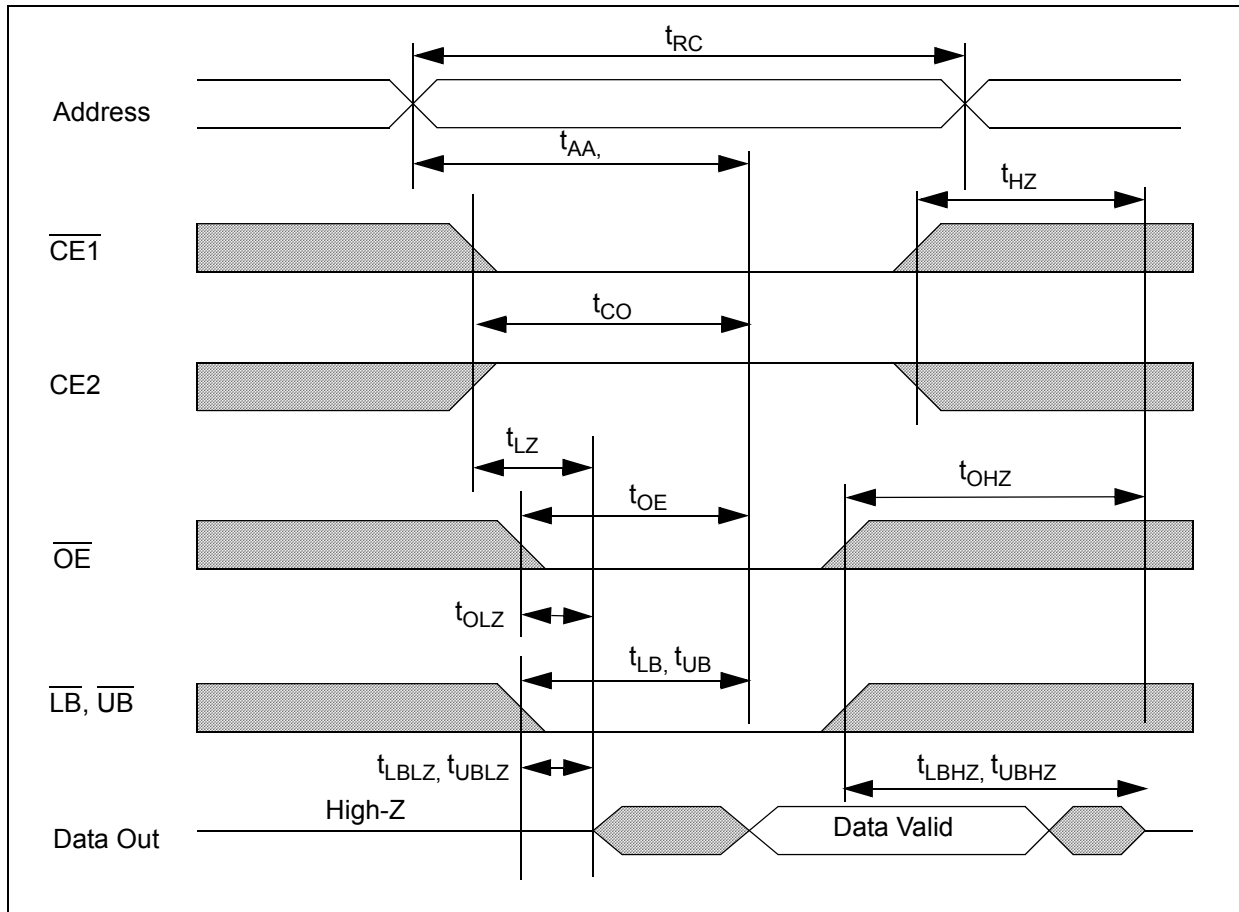
Note:

1. Full device AC operation assumes a 100us ramp time from 0 to V<sub>CC</sub>(min) and 200us wait time after V<sub>CC</sub> stabilization.
2. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC</sub>(min) ≥ 100us or stable at V<sub>CC</sub>(min) ≥ 100us.

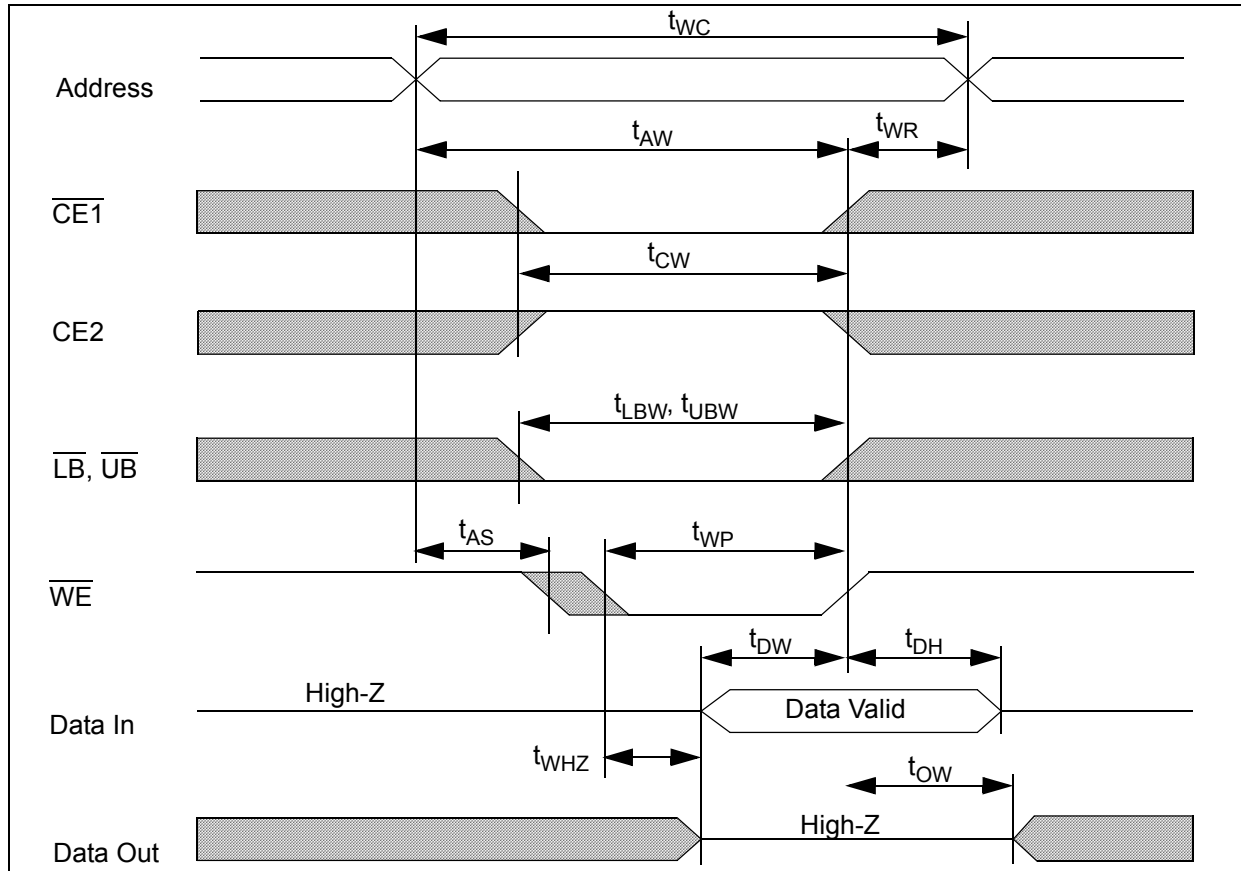
## Timing of Read Cycle ( $\overline{CE1} = \overline{OE} = V_{IL}, \overline{WE} = CE2 = V_{IH}$ )



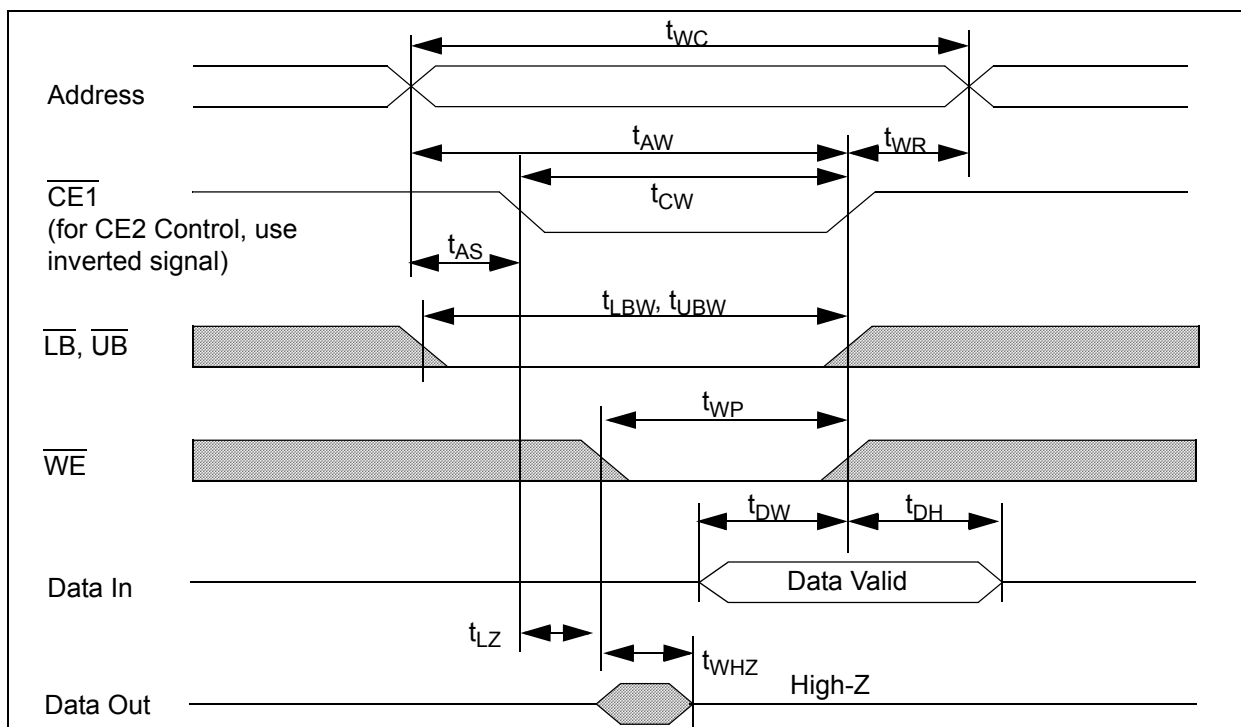
## Timing Waveform of Read Cycle ( $\overline{WE} = V_{IH}$ )



## Timing Waveform of Write Cycle ( $\overline{WE}$ control)



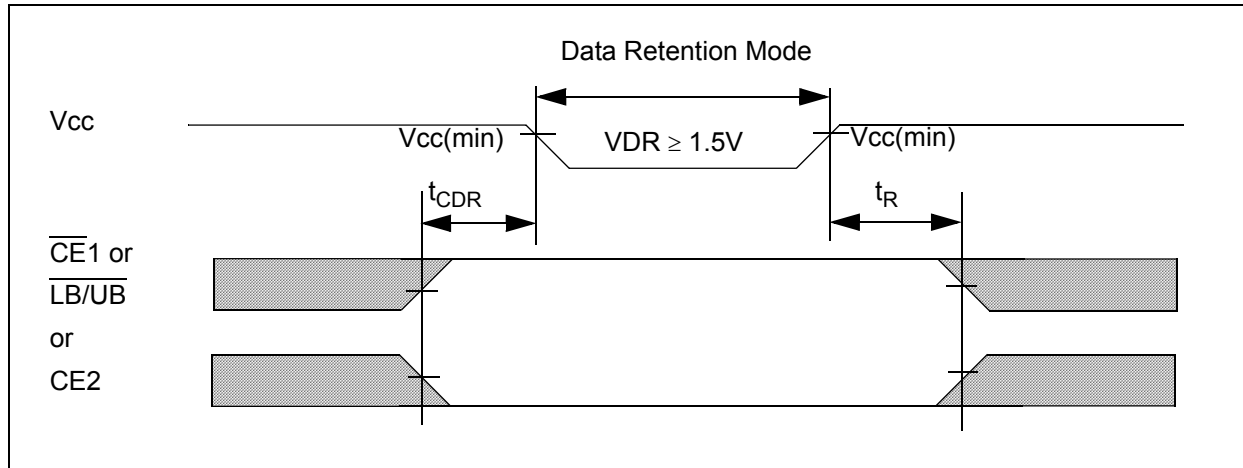
## Timing Waveform of Write Cycle ( $\overline{CE1}$ Control)



## Data Retention Characteristics

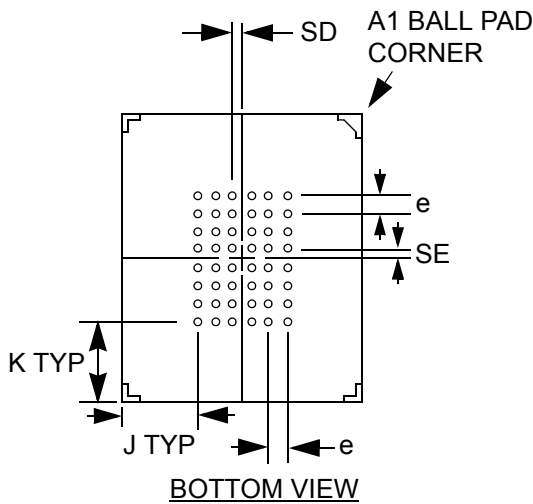
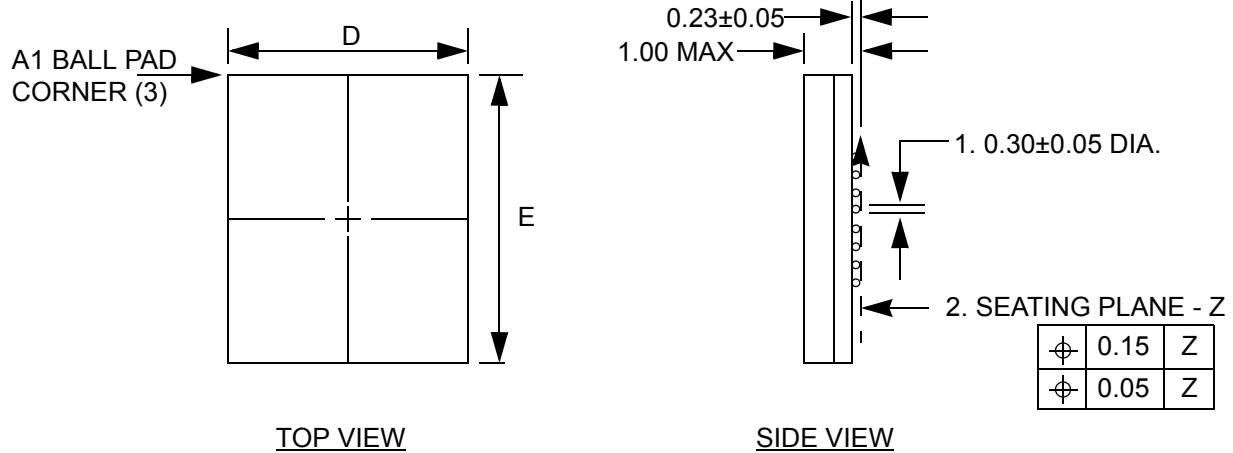
Parameter	Description	Condition	Min	Typ	Max	Unit
$V_{DR}$	Vcc for Data Retention		1.5			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5V, CE \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			10 4	$\mu A$
$t_{CDR}$	Chip Deselect to Data Retention Time		0			ns
$t_R$	Operation Recovery Time		$t_{RC}$			ns

## Data Retention Waveform



Note: Full device operation requires linear Vcc ramp from VDR to Vcc(min) > 100  $\mu s$

## VFBGA Package



1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

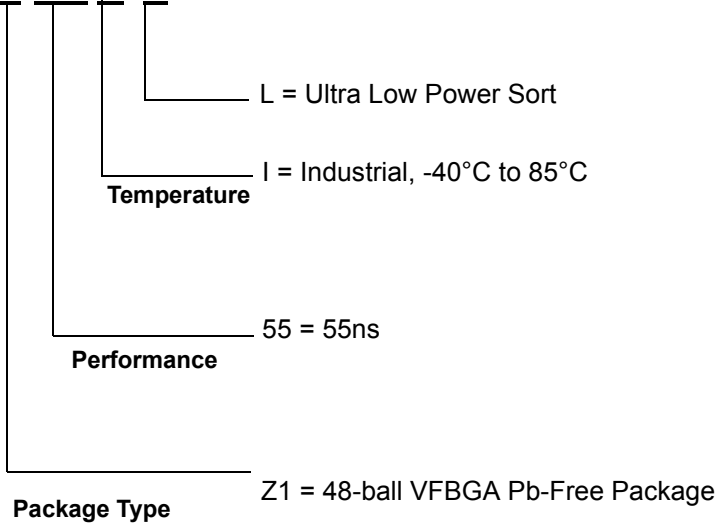
## Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL



## Ordering Information

**N08L163WC2CX-XX X L**



## Revision History

Revision	Date	Change Description
A	Oct 6, 2004	Initial Advance Release
B	Nov 9, 2004	General Update
C	Jan 14, 2005	General Update

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