

Doc. Number:

- Tentative Specification
 Preliminary Specification
 Approval Specification

MODEL NO.: N140BGE
SUFFIX: EA3

Customer: CMI Common Spec

APPROVED BY

SIGNATURE

Name / Title _____

Note :

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REVISION HISTORY

Version	Date	Page	Description
0.0	Aug 28, 2012	All	Tentative Spec Ver.0.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140BGE-EA3 is a 14.0" (14.0" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 30 pins eDP interface. This module supports 1366 x 768 HD mode and can display 262,144 colors.

The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	14.0" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.2265 (H) x 0.2265 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White	200	Cd/m2	
Power Consumption	Total (3.079) W (Max.)@cell (0.75) W (Max.), BL (2.329)W(Max.)		(1)

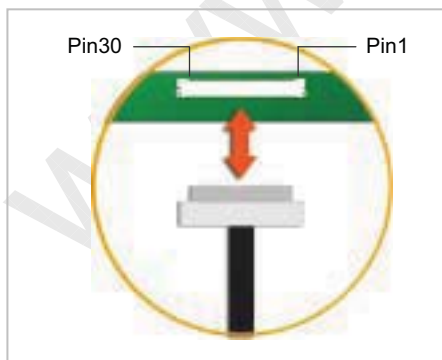
Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 °C, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	319.9	320.4	320.9	mm	(1)
	Vertical (V)	204.6	205.1	205.6	mm	
	Thickness (T)	-	-	3.0	mm	
Active Area	Horizontal		309.4		mm	
	Vertical		173.95		mm	
Weight		-	260	270	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-030E-12 or equivalent

User's connector Part No: IPEX-20453-030T-01 or equivalent

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

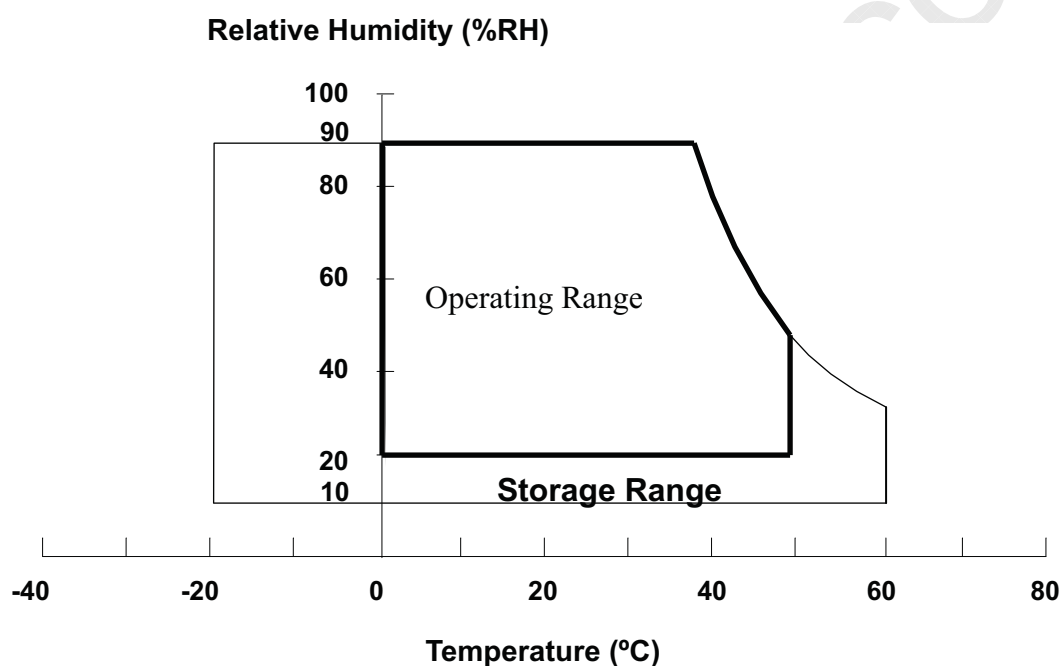
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)

Note (1) (a) 90 %RH Max. (Ta <= 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



3.2 ELECTRICAL ABSOLUTE RATINGS

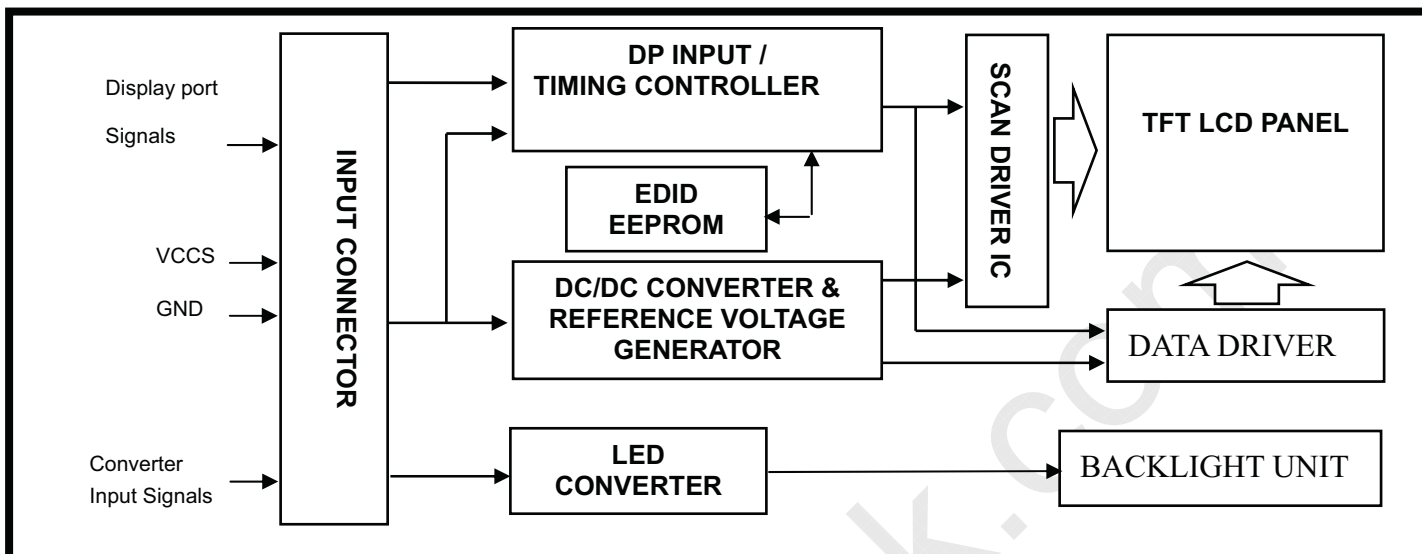
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	+4.0	V	
Converter Input Voltage	LED_VCCS	-0.3	24	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



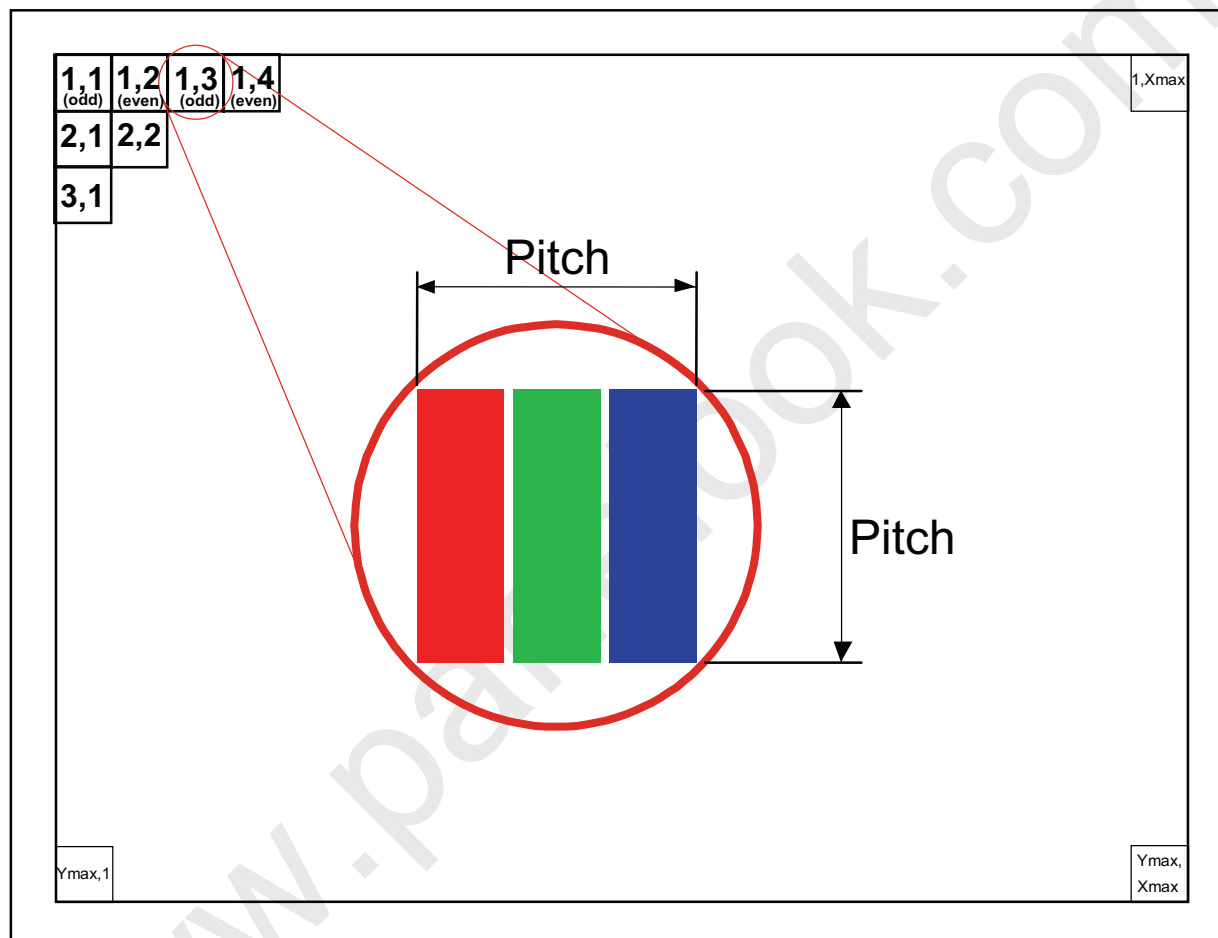
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for CMI test)	
2	NC	No Connection (Reserved)	
3	NC	No Connection (Reserved)	
4	NC	No Connection (Reserved)	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for CMI test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for CMI test)	
25	NC	No Connection (Reserved for CMI test)	

26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for CMI test)	

Note (1) The first pixel is odd as shown in the following figure.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

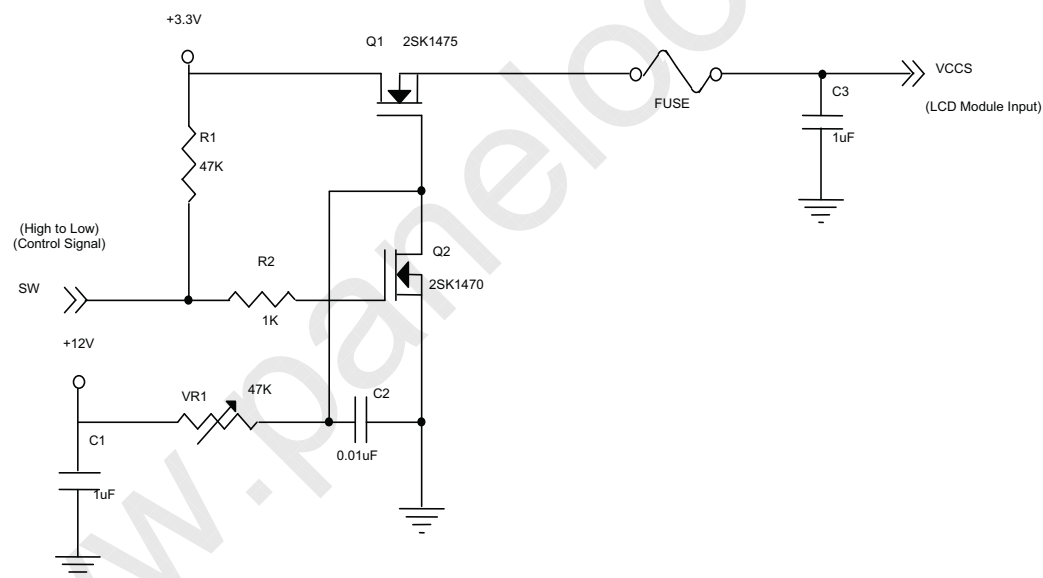
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
HPD	High Level		2.25	-	2.75	V	
	Low Level		0	-	0.4	V	
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I_{CC}		(212)	(227)	mA	(3)a
	Black			(212)	(227)	mA	(3)b

Note (1) The ambient temperature is $T_a = 25 \pm 2 \text{ }^\circ\text{C}$.

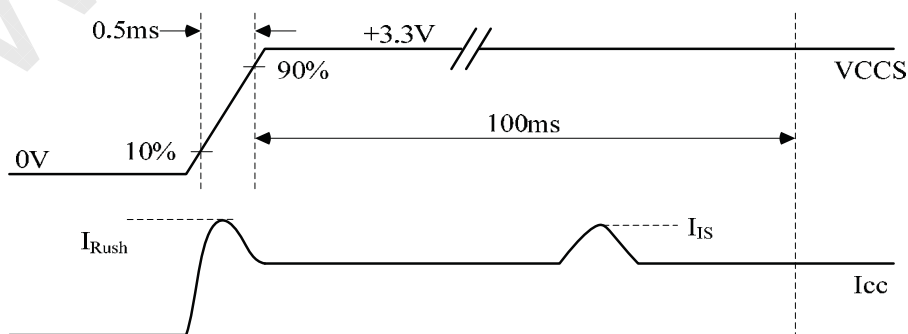
Note (2) I_{RUSH} : the maximum current when VCCS is rising

I_{IS} : the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

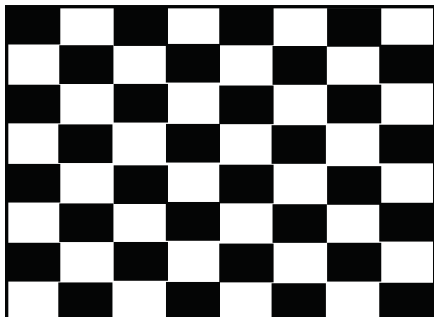


VCCS rising time is 0.5ms



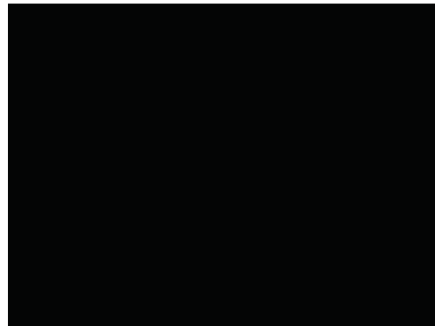
Note (3) The specified power supply current is under the conditions at $V_{CCS} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^\circ\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. Black Pattern



Active Area

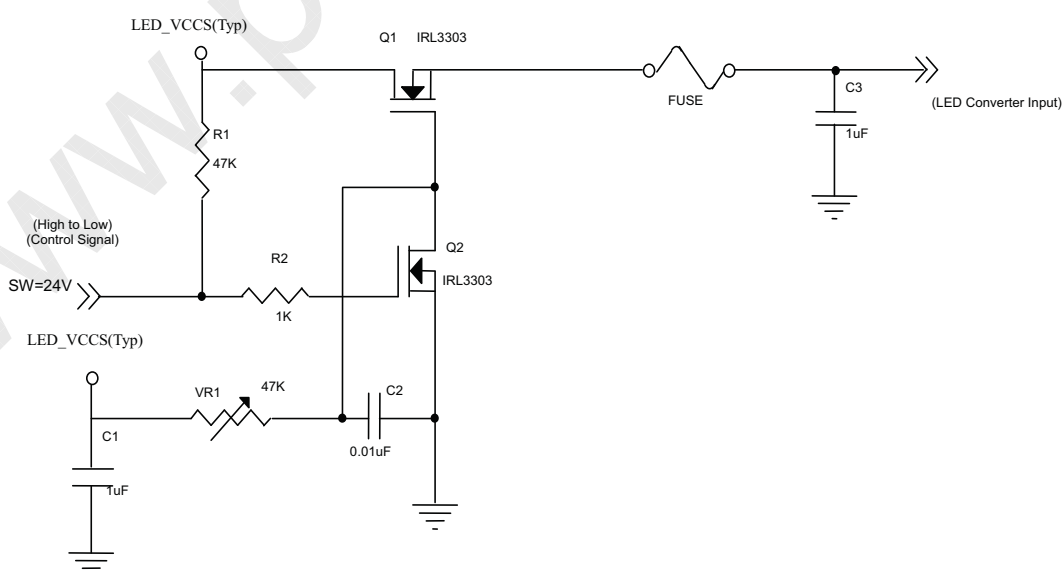
4.3.2 LED CONVERTER SPECIFICATION

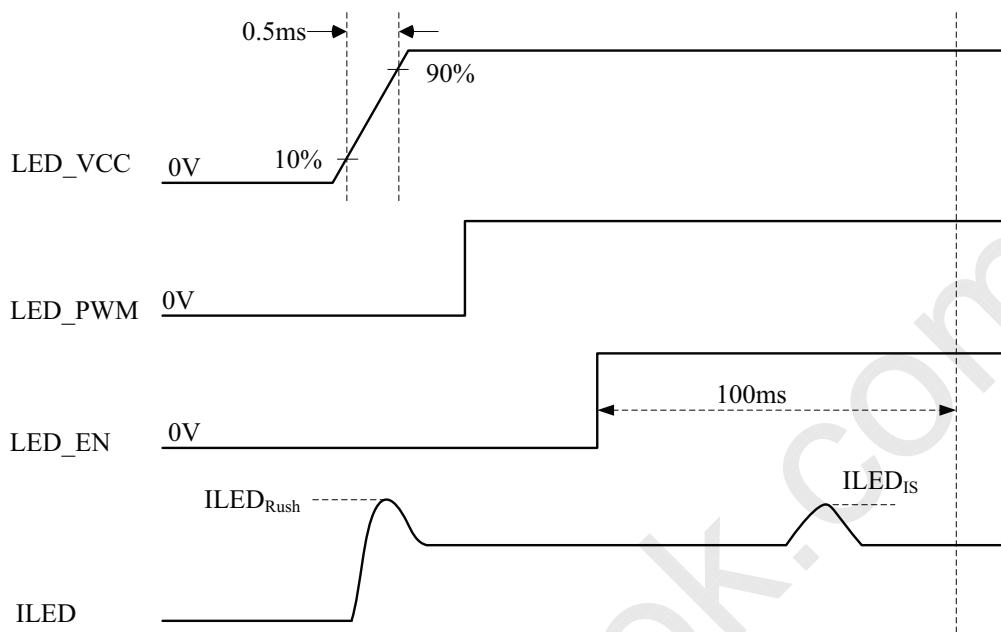
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	(6.0)	(12.0)	(21.0)	V	
Converter Inrush Current		I _{LED_RUSH}	-	-	(1.5)	A	(1)
EN Control Level	Backlight On		2.3	-	5	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	PWM High Level		2.3	-	5	V	
	PWM Low Level		0	-	0.5	V	
PWM Control Duty Ratio			10	-	100	%	
			5	-	100	%	(2)
PWM Control Permissible Ripple Voltage		V _{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f _{PWM}	190	-	2K	Hz	(3)
LED Power Current	LED_VCCS =Typ.	TBD	(145)	(188)	(204)	mA	(4)

Note (1) I_{LED_RUSH}: the maximum current when LED_VCCS is rising,

I_{LED_IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms


Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it’s a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

$$N : \text{Integer } (N \geq 3)$$

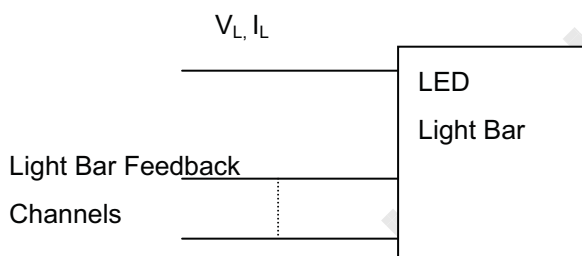
$$f : \text{Frame rate}$$

Note (4) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, $f_{PWM} = 200 \text{ Hz}$, Duty=100%.

4.3.3 BACKLIGHT UNIT
 $T_a = 25 \pm 2 \text{ }^\circ\text{C}$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	25	29	30	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	--	(66)	--	mA	
Power Consumption	P_L	(1.65)	(1.914)	(1.98)	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at $T_a = 25 \pm 2 \text{ }^\circ\text{C}$ and $I_L = 22 \text{ mA(Per EA)}$ until the brightness becomes $\leq 50\%$ of its original value.

4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

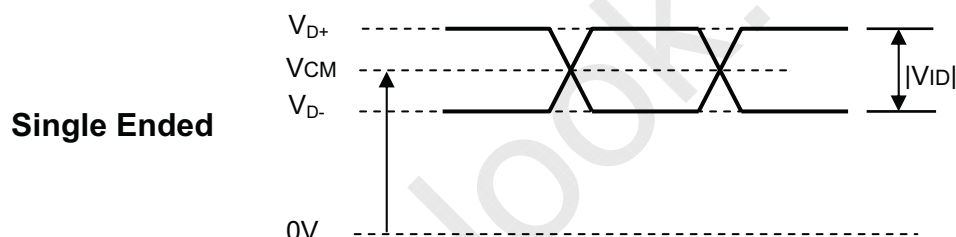
4.4.1 DISPLAY PORT INTERFACE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	V _{CM}	0		2	V	(1)(3)
AUX AC Coupling Capacitor	C _{AUX}	75		200	nF	(2)

Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.1.

(2) The AUX AC Coupling Capacitor should be placed on Source Devices.

(3)The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1



4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

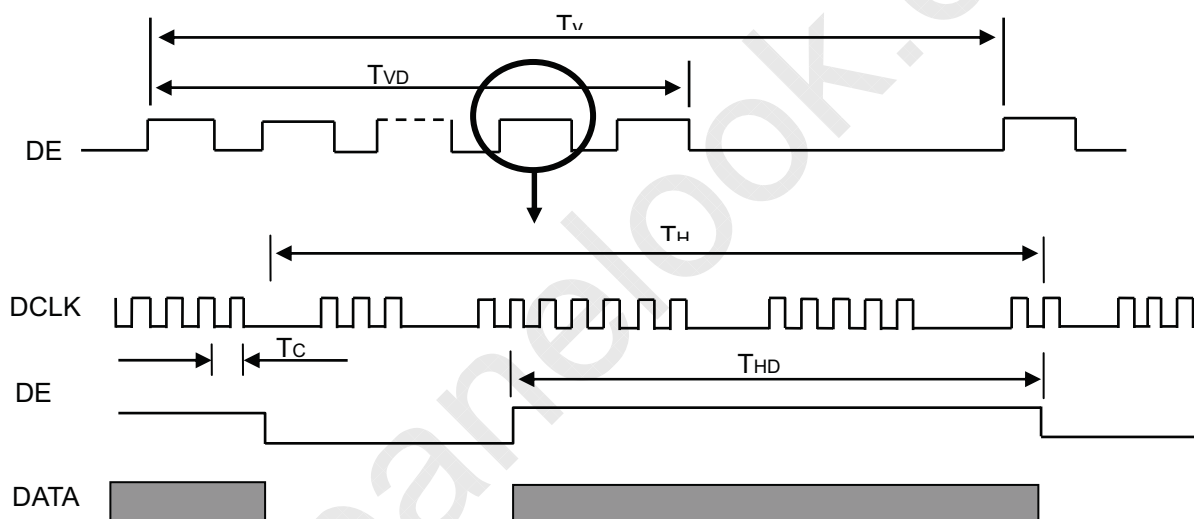
4.5 DISPLAY TIMING SPECIFICATIONS

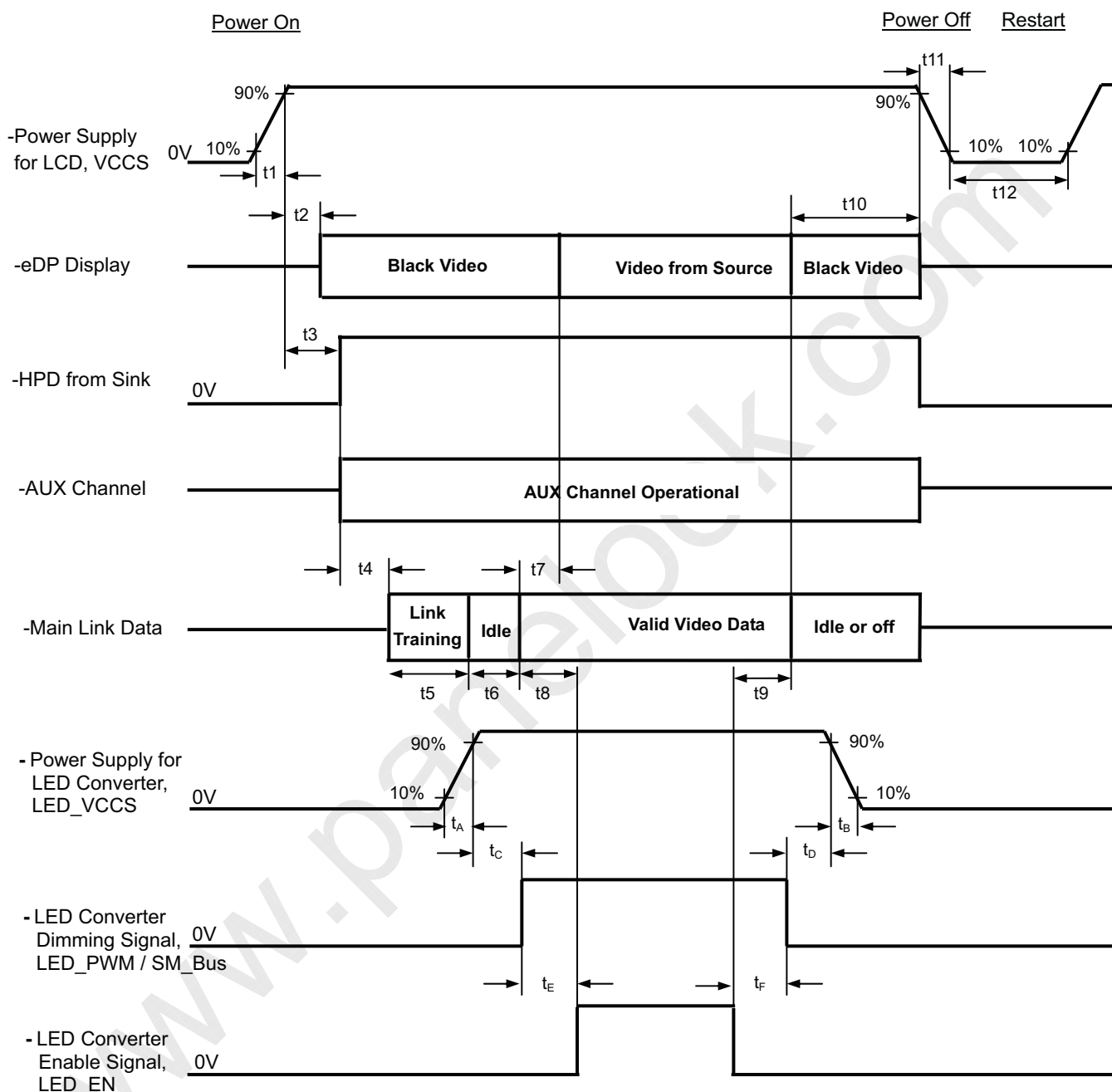
The input signal timing specifications are shown as the following table and timing diagram.

Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	49.61	76.42	78.44	MHz	-
DE	Vertical Total Time	TV	790	800	810	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	32	TV-TVD	TH	-
	Horizontal Total Time	TH	1570	1592	1614	Tc	-
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	226	TH-THD	Tc	-

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE


Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	-
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	-
t4	Delay from HPD high to link training initialization	Source	-	-	ms	-
t5	Link training duration	Source	-	-	ms	-
t6	Link idle	Source	-	-	ms	-
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	-
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	-
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	-
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	-
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t _A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t _C	Delay from LED power rising to LED dimming signal	Source	10	-	ms	-
t _D	Delay from LED dimming signal to LED power falling	Source	10	-	ms	-
t _E	Delay from LED dimming signal to LED enable signal	Source	10	-	ms	-
t _F	Delay from LED enable signal to LED dimming signal	Source	10	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

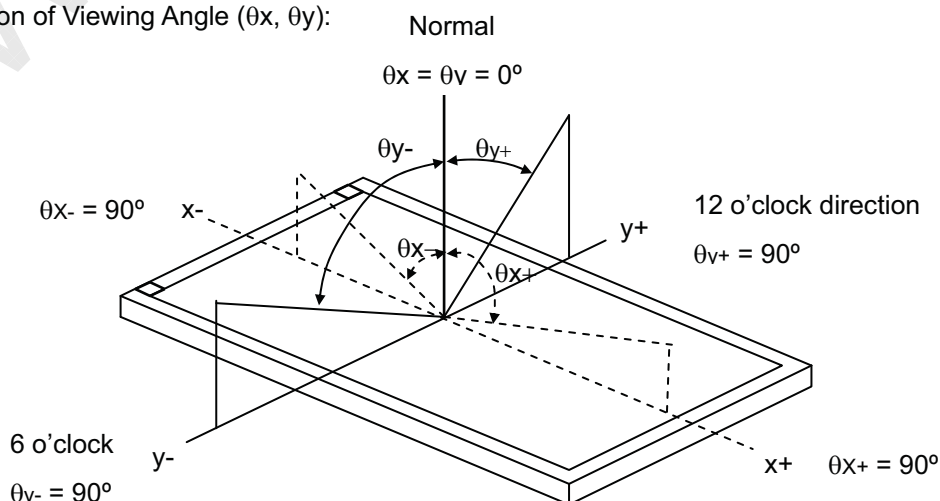
Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	(66)	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio		CR	θ _x =0°, θ _y =0° Viewing Normal Angle	350	500	-	-	(2), (5),(7)	
Response Time		T _R		-	(3)	(8)	ms	(3),(7)	
		T _F		-	(7)	(12)	ms		
Average Luminance of White		L _{Ave}		212	250	-	cd/m ²	(4), (6),(7)	
Color Chromaticity	Red	R _x		CR≥10	Typ - 0.03	(0.580)	Typ + 0.03	-	(1),(7)
		R _y				(0.340)		-	
	Green	G _x				(0.325)		-	
		G _y				(0.565)		-	
	Blue	B _x				(0.159)		-	
		B _y				(0.145)		-	
	White	W _x	0.313			-			
		W _y	0.329			-			
Viewing Angle	Horizontal	θ _{x+}	40	45	-	Deg.	(1),(5), (7)		
		θ _{x-}	40	45	-				
	Vertical	θ _{y+}	15	20	-				
		θ _{y-}	40	45	-				
White Variation of 5 Points		δW _{5p}	θ _x =0°, θ _y =0°	80	-	-	%	(5),(6), (7)	

Note (1) Definition of Viewing Angle (θ_x, θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

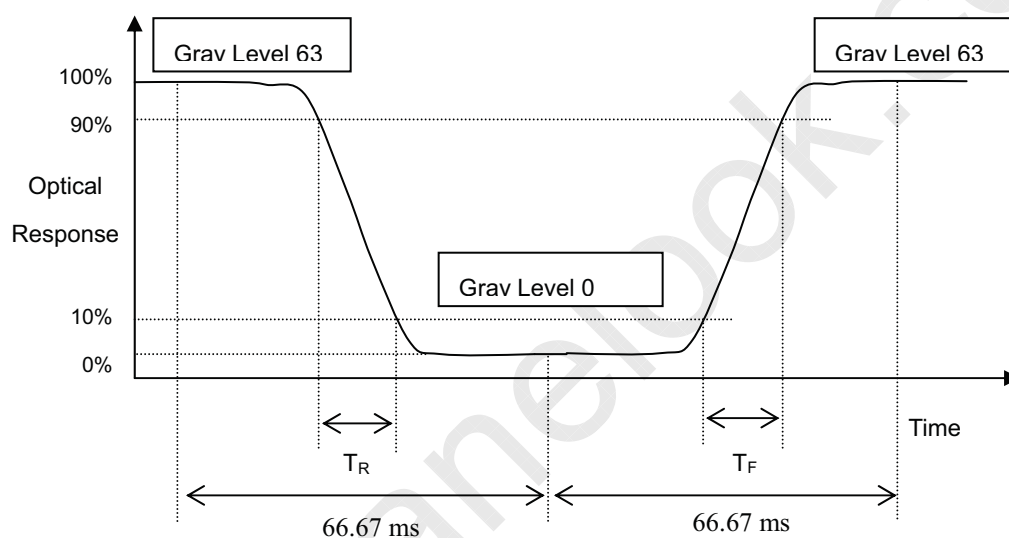
$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

L₆₃: Luminance of gray level 63

L₀: Luminance of gray level 0

$$\text{CR} = \text{CR} (1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):

Note (4) Definition of Average Luminance of White (L_{AVE}):

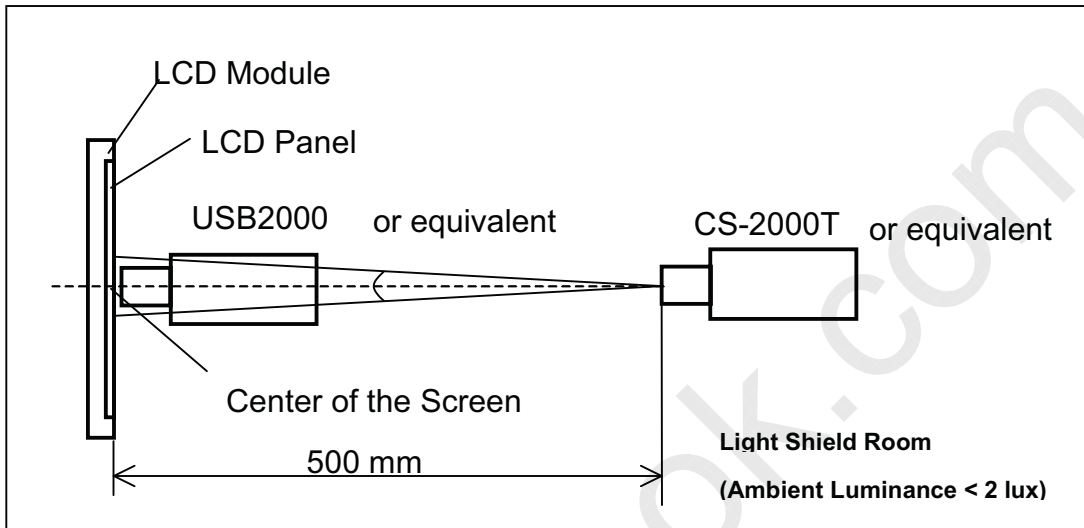
Measure the luminance of White at 5 points

$$L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$$

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

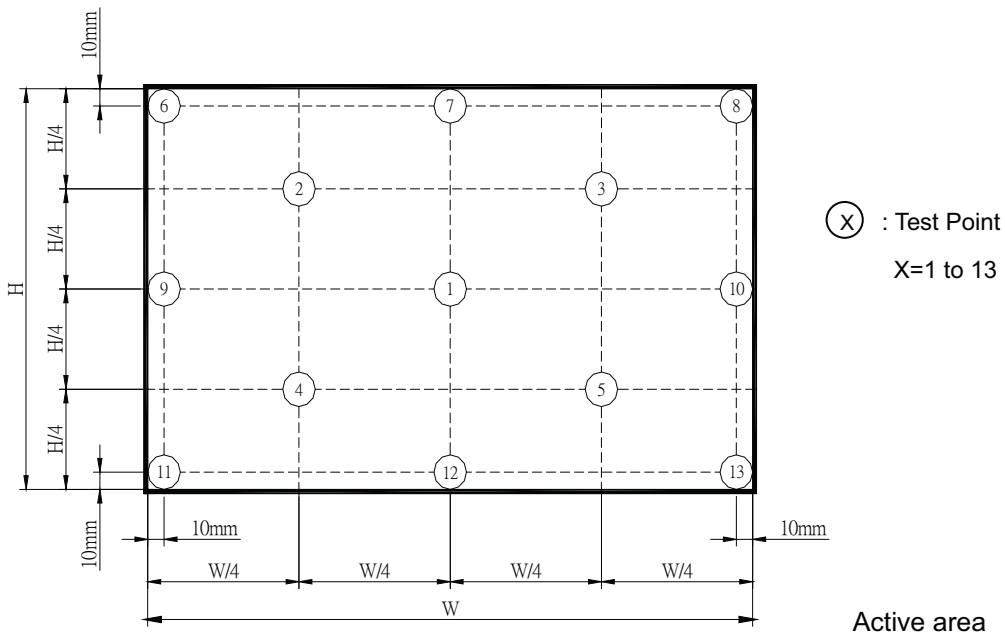
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points

$$\delta W_{5p} = \{ \text{Minimum} [L(1) \sim L(5)] / \text{Maximum} [L(1) \sim L(5)] \} * 100\%$$



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60°C, 240 hours	(1) (2)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour \longleftrightarrow 60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80% RH, 240 hours	
ESD Test (Operation)	150pF, 330 Ω , 1sec/cycle Condition 1 : Contact Discharge, \pm 8KV Condition 2 : Air Discharge, \pm 15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of \pm X, \pm Y, \pm Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

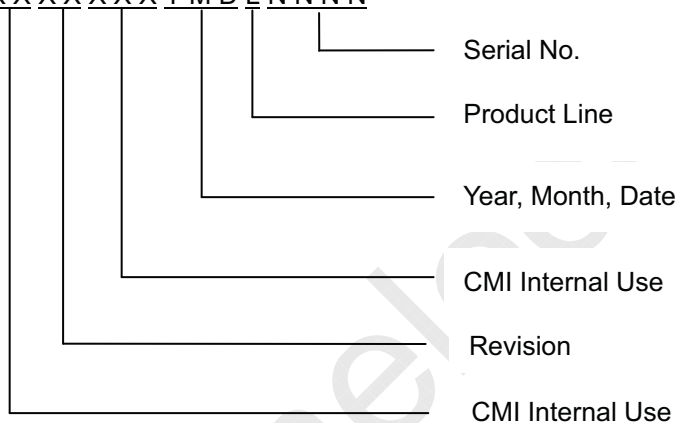
7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N140BGE - EA3
- (b) Revision: Rev. XX, for example: C1, C2 ...etc.
- (c) Serial ID: XXXXXXYMDLNNN



- (d) Production Location: MADE IN XXXX.
- (e) UL/CB logo: XXXX is UL factory ID.

Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

7.2 CARTON

Box Dimensions : 435(L)*350(W)*275(H)
 Weight : Approx. 8.09Kg (20 module .per. 1box)

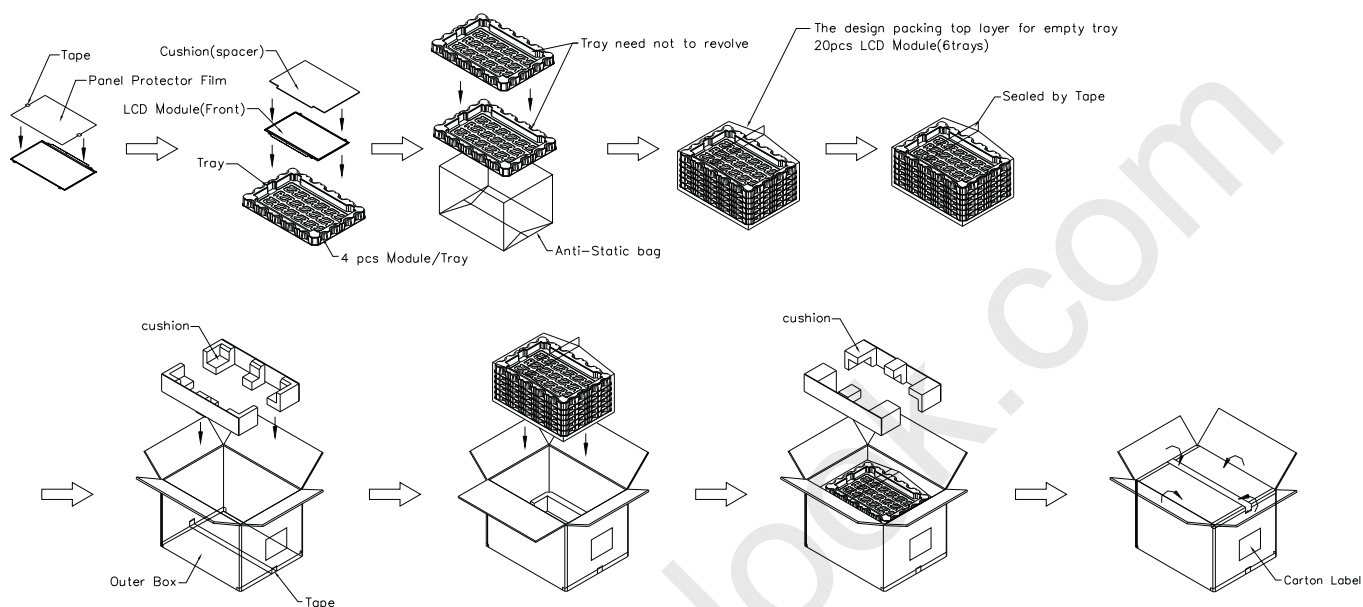


Figure. 7-2 Packing method

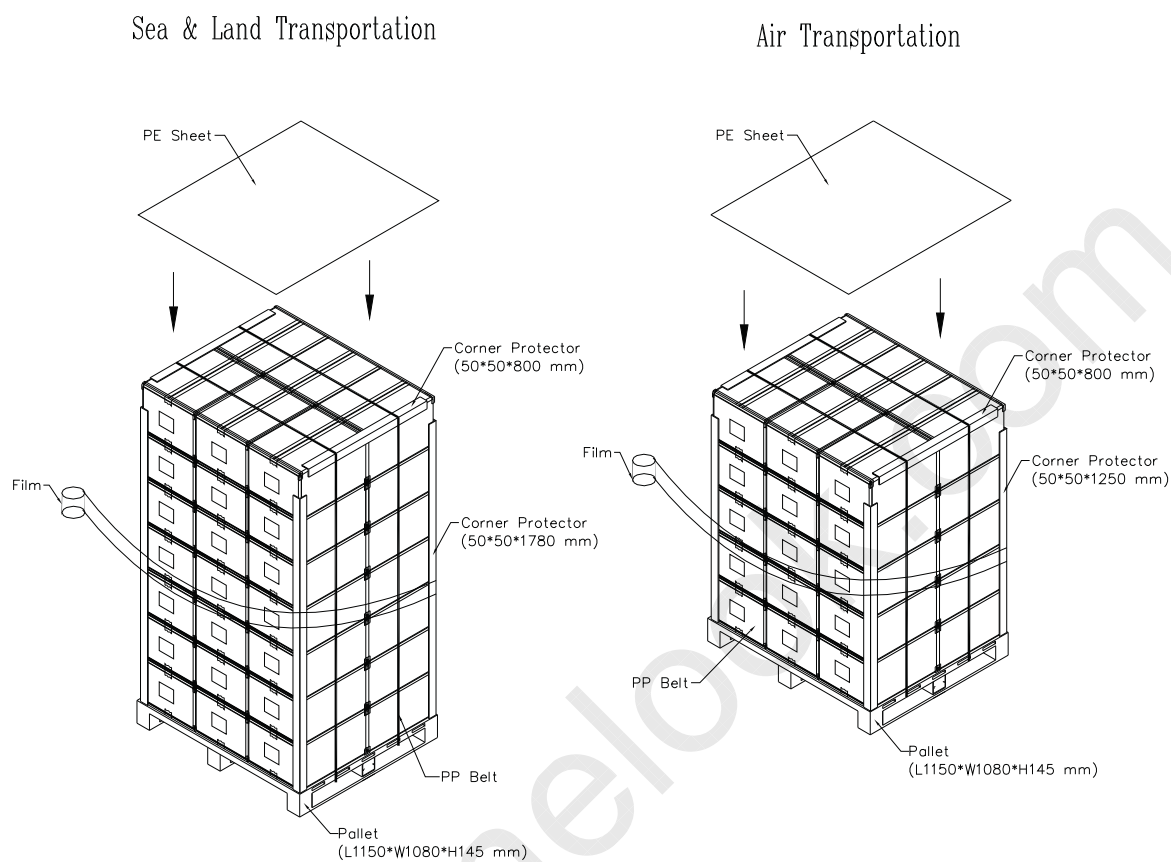
7.3 PALLET

Figure. 7-3 Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMIS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

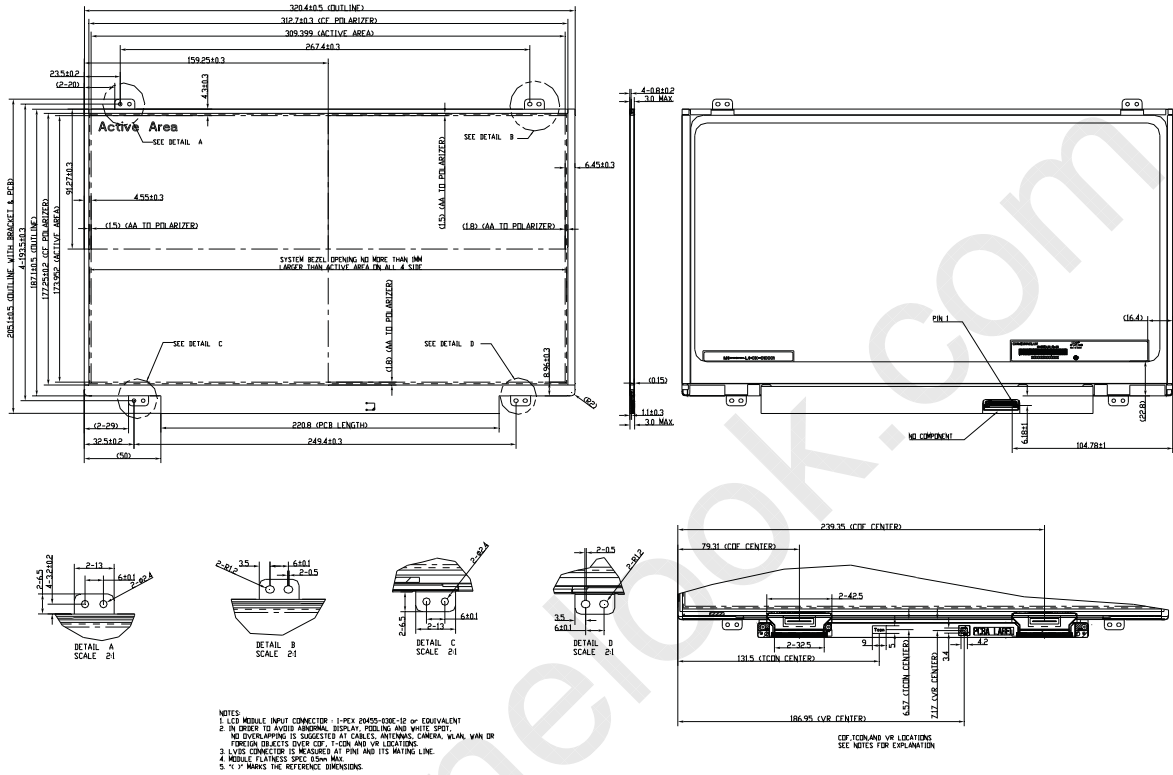
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD1 standards.

Byte # (decimal)	Byte # (hex)	Header	00	00000000
0	0	Header	FF	11111111
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	00	00000000
7	7	EISA ID manufacturer name ("CMN")	0D	00001101
8	8	EISA ID manufacturer name (Compressed ASCII)	AE	10101110
9	9	ID product code (N140BGE-EA3)	90	10010000
10	0A	ID product code (hex LSB first; N140BGE-EA3)	14	00010100
11	0B	ID S/N (fixed "0")	00	00000000
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	Week of manufacture (fixed "00H")	28	00101000
16	10	Year of manufacture (fixed "00H")	16	00010110
17	11	EDID structure version # ("1")	01	00000001
18	12	EDID revision # ("3")	03	00000011
19	13	Video I/P definition ("digital")	80	10000000
20	14	Max H image size ("30.9cm")	1F	00011111
21	15	Max V image size ("17.4cm")	11	00010001
22	16	Display Gamma (Gamma = "2.2")	78	01111000
23	17	Feature support ("Active off, RGB Color")	0A	00001010
24	18	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	2B	00101011
25	19	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	35	00110101
26	1A	Red-x (Rx = "0.59")	97	10010111
27	1B	Red-y (Ry = "0.342")	57	01010111
28	1C	Green-x (Gx = "0.330")	54	01010100
29	1D	Green-y (Gy = "0.562")	8F	10001111
30	1E	Blue-x (Bx = "0.160")	29	00101001
31	1F	Blue-y (By = "0.140")	23	00100011
32	20	White-x (Wx = "0.313")	50	01010000
33	21	White-y (Wy = "0.329")	54	01010100
34	22	Established timings 1	00	00000000
35	23	Established timings 2	00	00000000
36	24	Manufacturer's reserved timings	00	00000000
37	25	Standard timing ID # 1	01	00000001
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 2	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 3	01	00000001

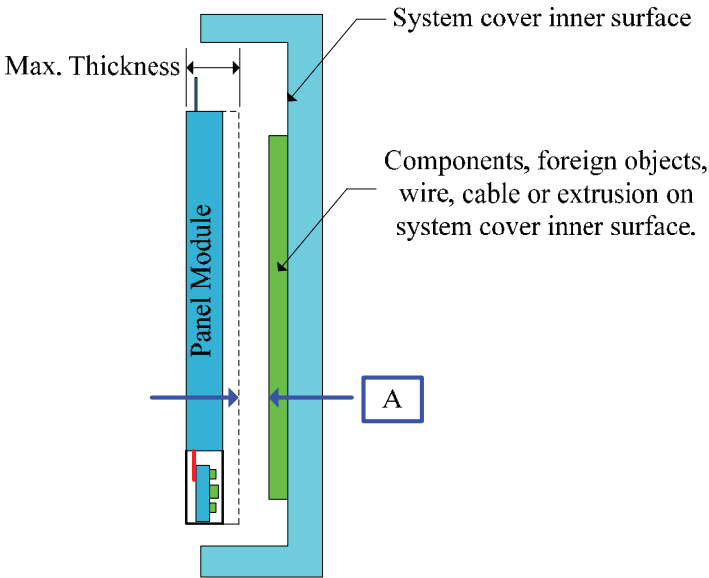
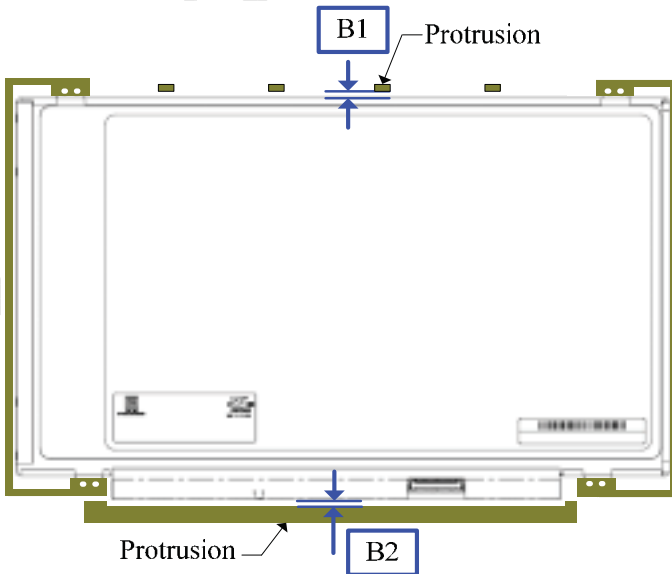
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 4	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 5	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 6	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 7	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 8	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Detailed timing description # 1 Pixel clock ("76.42MHz", According to VESA CVT Rev1.1)	DA	11011010
54	36	# 1 Pixel clock (hex LSB first)	1D	00011101
55	37	# 1 H active ("1366")	56	01010110
56	38	# 1 H blank ("226")	E2	11100010
57	39	# 1 H active : H blank ("1366 : 226")	50	01010000
58	3A	# 1 V active ("768")	00	00000000
59	3B	# 1 V blank ("32")	20	00100000
60	3C	# 1 V active : V blank ("768 :32")	30	00110000
61	3D	# 1 H sync offset ("68")	44	01000100
62	3E	# 1 H sync pulse width ("45")	2D	00101101
63	3F	# 1 V sync offset : V sync pulse width ("4 : 7")	47	01000111
64	40	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("68: 45 : 4 : 7")	00	00000000
65	41	# 1 H image size ("309 mm")	35	00110101
66	42	# 1 V image size ("174 mm")	AE	10101110
67	43	# 1 H image size : V image size ("309 : 174")	10	00010000
68	44	# 1 H boarder ("0")	00	00000000
69	45	# 1 V boarder ("0")	00	00000000
70	46	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
71	47	Detailed timing description # 2	00	00000000
72	48	# 2 Flag	00	00000000
73	49	# 2 Reserved	00	00000000
74	4A	# 2 FE (hex) defines ASCII string (Model Name "N140BGE-EA3", ASCII)	FE	11111110
75	4B	# 2 Flag	00	00000000
76	4C	# 2 1st character of name ("N")	4E	01001110
77	4D	# 2 2nd character of name ("1")	31	00110001
78	4E	# 2 3rd character of name ("4")	34	00110100
79	4F	# 2 4th character of name ("0")	30	00110000
80	50	# 2 5th character of name ("B")	42	01000010
81	51	# 2 6th character of name ("G")	47	01000111
82	52	# 2 7th character of name ("E")	45	01000101
83	53	# 2 8th character of name ("-")	2D	00101101
84	54	# 2 9th character of name ("E")	45	01000101
85	55	# 2 9th character of name ("A")	41	01000001

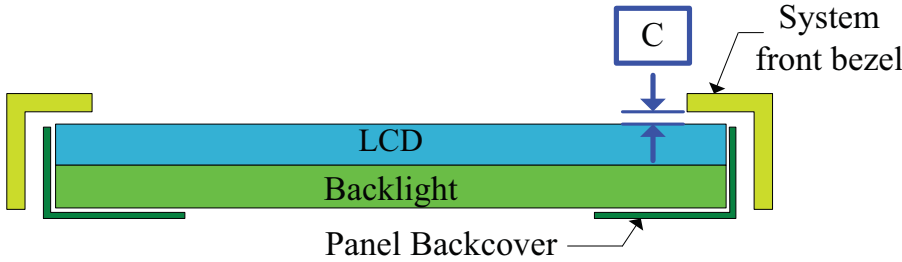
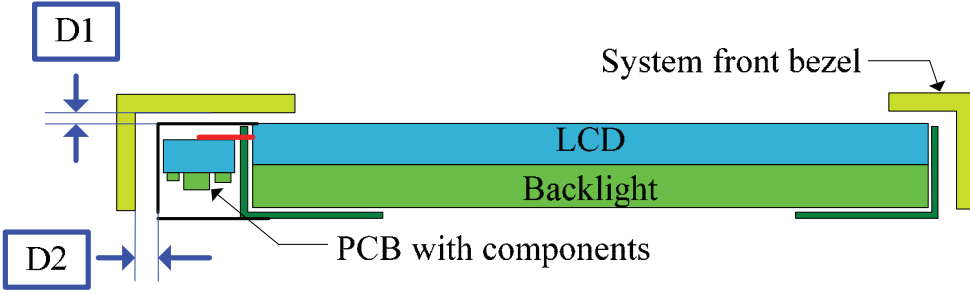
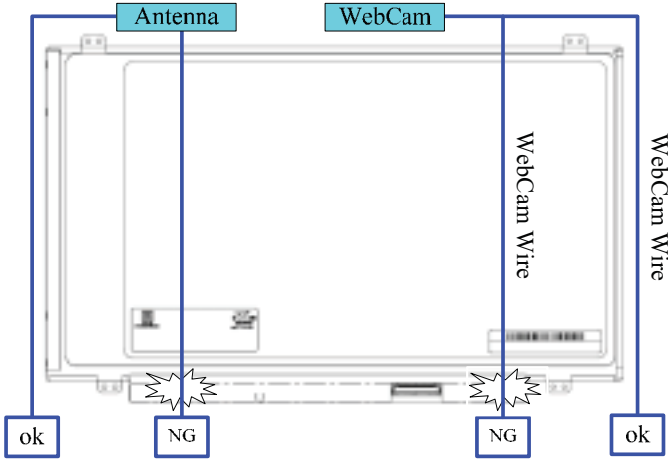
86	56	# 2 Ath character of name ("3")	33	00110011
87	57	# 2 New line character indicates end of ASCII string	0A	00001010
88	58	# 2 Padding with "Blank" character	20	00100000
89	59	Detailed timing description # 3	00	00000000
90	5A	# 3 Flag	00	00000000
91	5B	# 3 Reserved	00	00000000
92	5C	# 3 FE (hex) defines ASCII string (Vendor "CMN", ASCII)	FE	11111110
93	5D	# 3 Flag	00	00000000
94	5E	# 3 1st character of string ("C")	43	01000011
95	5F	# 3 2nd character of string ("M")	4D	01001101
96	60	# 3 3rd character of string ("N")	4E	01001110
97	61	# 3 New line character indicates end of ASCII string	0A	00001010
98	62	# 3 Padding with "Blank" character	20	00100000
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	Detailed timing description # 4	00	00000000
108	6C	# 4 Flag	00	00000000
109	6D	# 4 Reserved	00	00000000
110	6E	# 4 FE (hex) defines ASCII string (Model Name"N140BGE-EA3", ASCII)	FE	11111110
111	6F	# 4 Flag	00	00000000
112	70	# 4 1st character of name ("N")	4E	01001110
113	71	# 4 2nd character of name ("1")	31	00110001
114	72	# 4 3rd character of name ("4")	34	00110100
115	73	# 4 4th character of name ("0")	30	00110000
116	74	# 4 5th character of name ("B")	42	01000010
117	75	# 4 6th character of name ("G")	47	01000111
118	76	# 4 7th character of name ("E")	45	01000101
119	77	# 4 8th character of name ("-")	2D	00101101
120	78	# 4 9th character of name ("E")	45	01000101
121	79	# 4 9th character of name ("A")	41	01000001
122	7A	# 4 Ath character of name ("3")	33	00110011
123	7B	# 4 New line character indicates end of ASCII string	0A	00001010
124	7C	# 4 Padding with "Blank" character	20	00100000
125	7D	Extension flag	00	00000000
126	7E	Checksum	EC	11101100
127	7F	Header	00	00000000

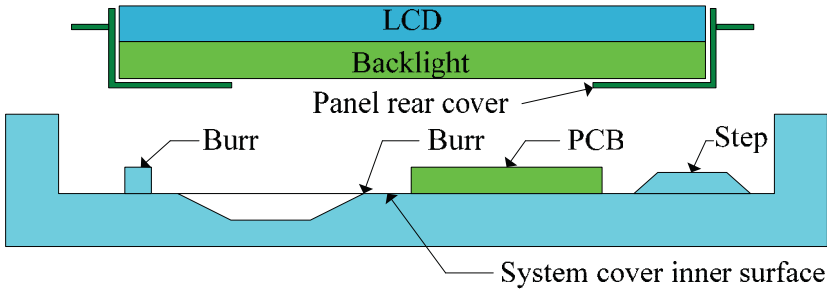
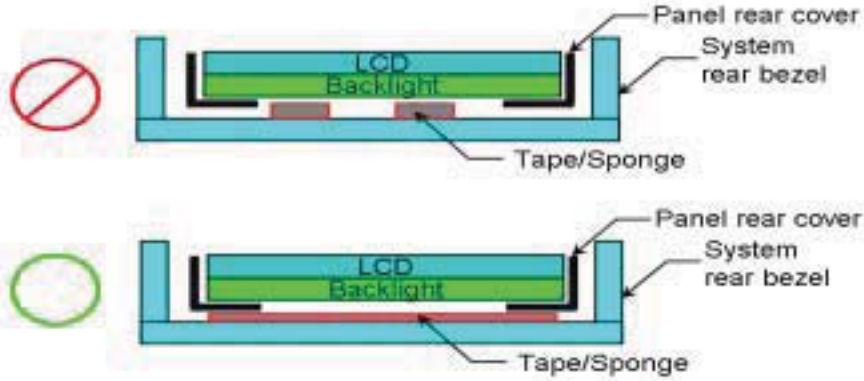
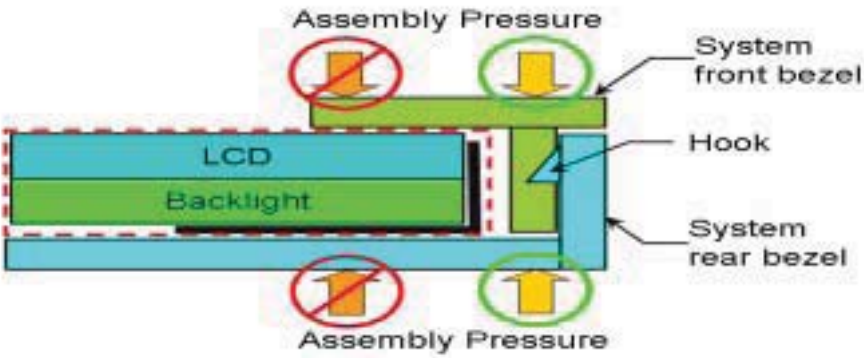
Appendix. OUTLINE DRAWING

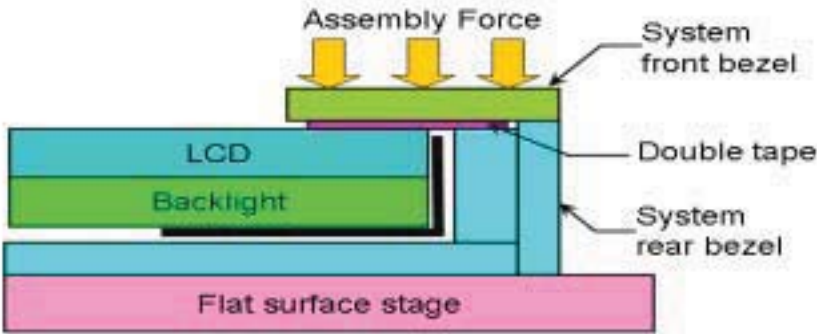
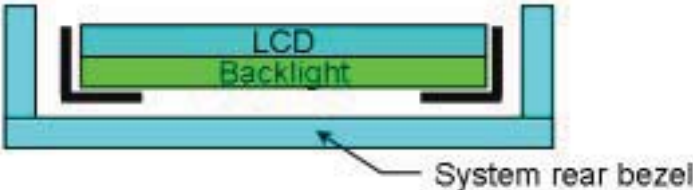
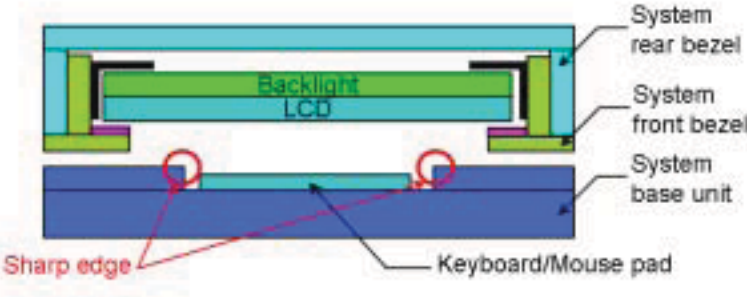


Appendix. SYSTEM COVER DESIGN NOTICE

1.	Design gap A between panel & any components on system cover
 <p>Max. Thickness</p> <p>System cover inner surface</p> <p>Components, foreign objects, wire, cable or extrusion on system cover inner surface.</p> <p>Panel Module</p> <p>A</p>	
Definition	<p>a). Sufficient gap between panel & system is a must for preventing from backpack or pogo test fail.</p> <p>b). Zero gap from panel's maximum thickness boundary to any components, foreign objects, wire, cable or extrusion on system cover inner surface is forbidden.</p>
2	Design gap B1 & B2 between panel & protrusions
 <p>B1</p> <p>Protrusion</p> <p>Protrusion</p> <p>B2</p>	
Definition	2.0mm min. gap is recommended between panel & protrusions for preventing from shock related failures.
3	Design gap C between system front bezel & panel surface.

	 <p>System front bezel</p> <p>LCD</p> <p>Backlight</p> <p>Panel Backcover</p>
Definition	<p>a). Sufficient gap between system front bezel & panel surface is a must for preventing from pooling or glass broken.</p> <p>b). Zero gap or interference is forbidden.</p>
4	Design gap D1 & D2 between system front bezel & PCB Assembly.
	 <p>System front bezel</p> <p>LCD</p> <p>Backlight</p> <p>PCB with components</p> <p>D1</p> <p>D2</p>
Definition	<p>a). Sufficient gap between system front bezel & PCB assembly is a must for preventing from abnormal display after backpack test, hinge test, twist test or pogo test.</p> <p>b). Zero gap or interference is forbidden.</p>
5	Interference examination of antenna cable and WebCam wire
	 <p>Antenna</p> <p>WebCam</p> <p>WebCam Wire</p> <p>WebCam Wire</p> <p>ok</p> <p>NG</p> <p>NG</p> <p>ok</p>
Definition	<p>a). Antenna cable or WebCam wire overlap with panel outline is forbidden for preventing from abnormal display & white spot after backpack test, hinge test, twist test or pogo test.</p> <p>b). Antenna cable or WebCam wire bypass panel outline is recommended.</p>
6	System inner surface examination

	
Definition	<p>a). Burr at logo edge, step, protrusion or PCB board will easily cause white spot or glass broken.</p> <p>b). Keeping flat surface underneath backlight is recommended.</p>
7	Tape/sponge design on system inner surface
	
Definition	<p>a) To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, it is not recommended to add tape/sponge in separate location. Since each tape/sponge may act as pressure concentration location.</p> <p>b) We suggest to design a tape/sponge that well covered under panel rear cover.</p>
8	Assembly SOP examination
	
Definition	To prevent panel crack during system front bezel assembly process with hook design, it is prohibited to press panel or any location that related directly to the panel.
9	Material used for system rear bezel

	
Definition	To prevent panel crack during system front bezel assembly process without hook design, it is only allowed to give slight pressure with large contact area. This can help to distribute the stress to prevent point concentration, also it is suggest to put the system on a flat surface stage during the assembly.
10	Material used for system rear bezel
	
Definition	a) To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, as the poor rigidity result from deformation of system rear cover during the test. b) We suggest to use aluminum-magnesium alloy as the rear frame material with thickness min 1.5mm, instead of using PC/ABS.
11	System base unit design near keyboard and mouse pad
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, no sharp edge design is allowed in any area that may damage the panel during the test. We suggest to remove all sharp edges, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.