TFT LCD Approval Specification

MODEL NO.: N141C1 - L05

Customer: Dell

Approved by:

Note:

記錄	工作	審核	角色	投票
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
3.0	Mar. 01,'07	All	All	Approval specification was first issued.

1 GENERAL DESCRIPTION

1.1 OVERVIEW

N141C1 - L05 is a 14.1" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1440 x (3 RGB) x 900 WXGA+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is built in.

1.2 FEATURES

- Thin and Light Weight
- WXGA+ (1440 x 900 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	303.48(H) X 189.675(V) (14.1 inch Diagonal)	mm	(1)
Bezel Opening Area	306.76 (H) x 193.0 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1440 x R.G.B. x 900	pixel	-
Pixel Pitch	0.21075 (H) x 0.21075 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Antiglare, Haze 44%, 3H	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	319	319.5	320	mm	(1)
	Vertical(V)	205	205.5	206	mm	
	Depth(D)	--	5.2	5.5	mm	
Weight		--	395	410	g	(2)
Weight		--	410	425	g	(3)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions

(2) Weight without inverter

(3) Weight with inverter.

2 ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

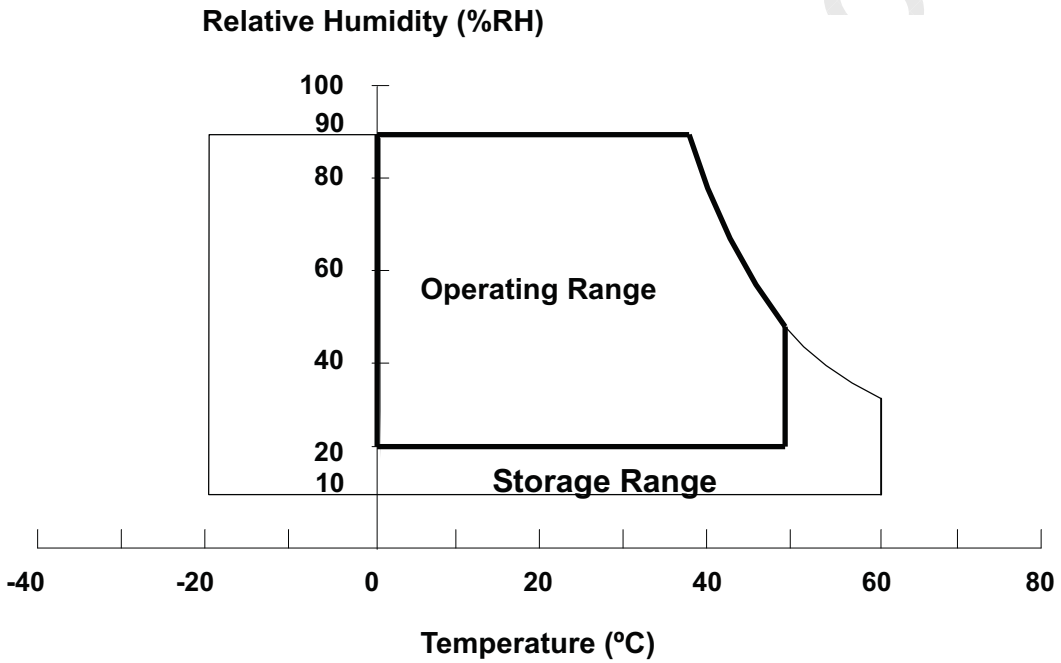
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation .

Note (2) The temperature of panel display surface area should be 0 ºC Min. and 60 ºC Max.

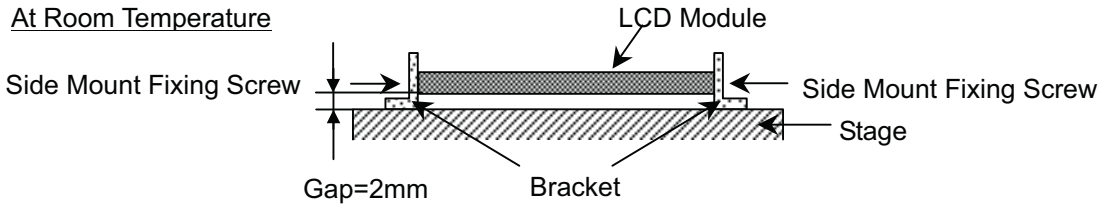


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave

Note (4) 10 ~ 300 Hz, 10 min / Cycle, 3 cycles for each X, Y, Z.:

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	V_{CC}+0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2)
Lamp Current	I_L	2.0	6.5	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	45	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3 ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

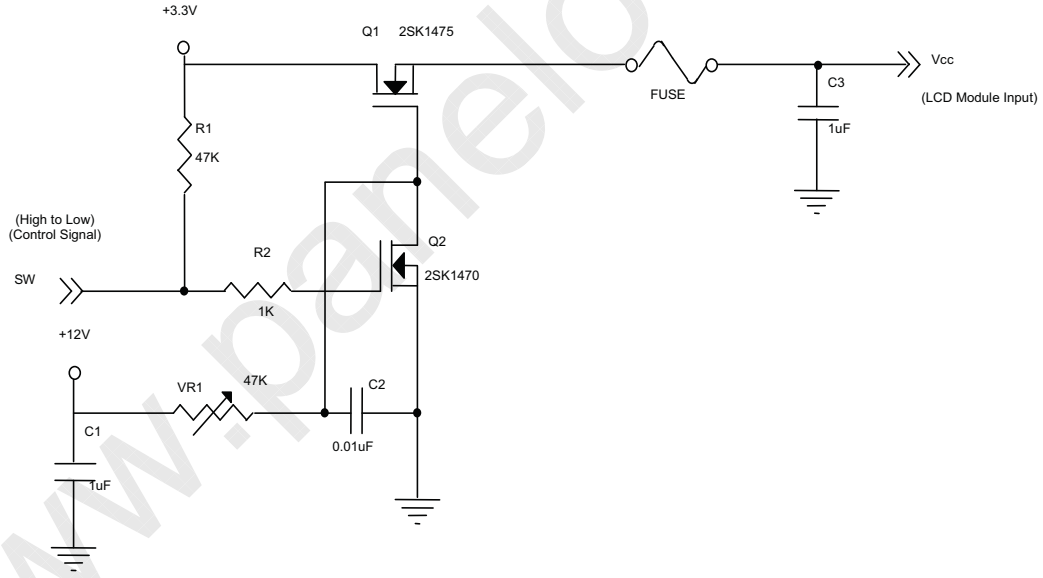
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Permissive Ripple Voltage		V_{RP}	-	50	-	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Initial Stage Current		I_{IS}	-	-	1.0	A	(2)
Power Supply Current	White	Icc	-	420	470	mA	(3)a
	Black		-	500	565	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$	-	-	+100	mV	(5), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100	-	-	mV	(5) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125	-	1.375	V	(5)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100	-	600	mV	(5)
Terminating Resistor		R_T	-	100	-	Ohm	-
Power per EBL WG		P_{EBL}	-	(3.19)	-	W	(4)

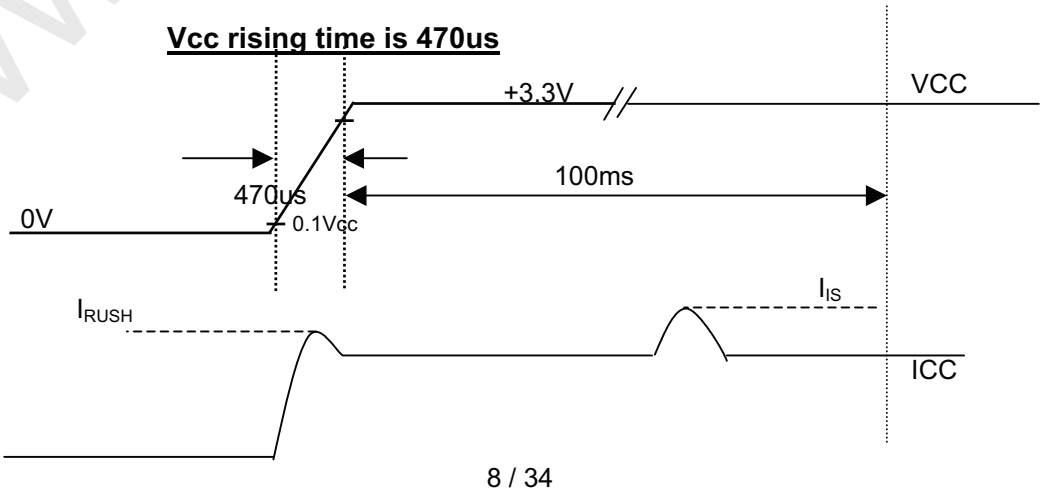
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.





Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

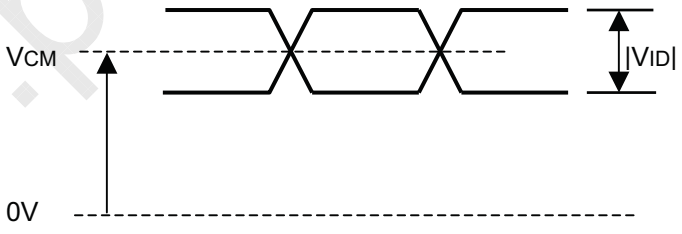
(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

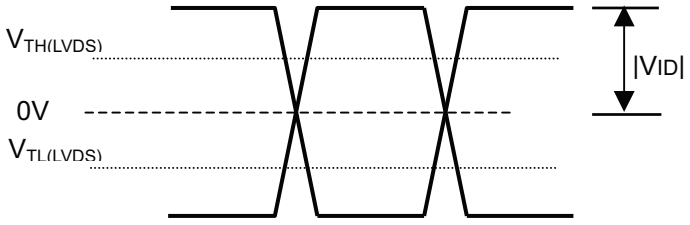
(d) The inverter used is provided from Sumida.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential

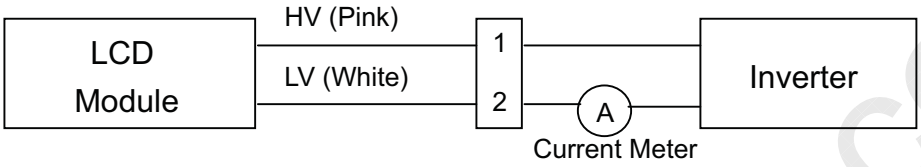


3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	612	680	748	V_{RMS}	I_L = 6.0 mA
Lamp Current	I_L	2.0	6.0	6.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	1370 (25 °C)	V_{RMS}	(2)
		-	-	1520 (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	45	-	80	KHz	(3)
Lamp Life Time	L_{BL}	15,000	-	-	Hrs	(5)
Power Consumption	P_L	-	4.08	-	W	(4), I_L = 6.0 mA

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I_L = 6 mArms until one of the following events occurs:

(a) When the brightness becomes or lowers than 50% of its original value.

(b) When the effective ignition length becomes or lowers than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter

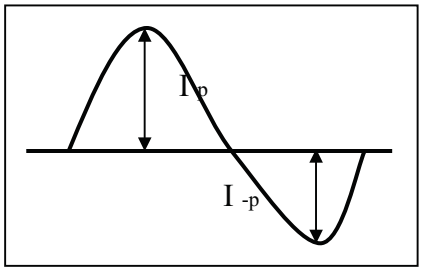
which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below.

b. The distortion rate of the waveform should be within $\sqrt{2}$ ± 10%.

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

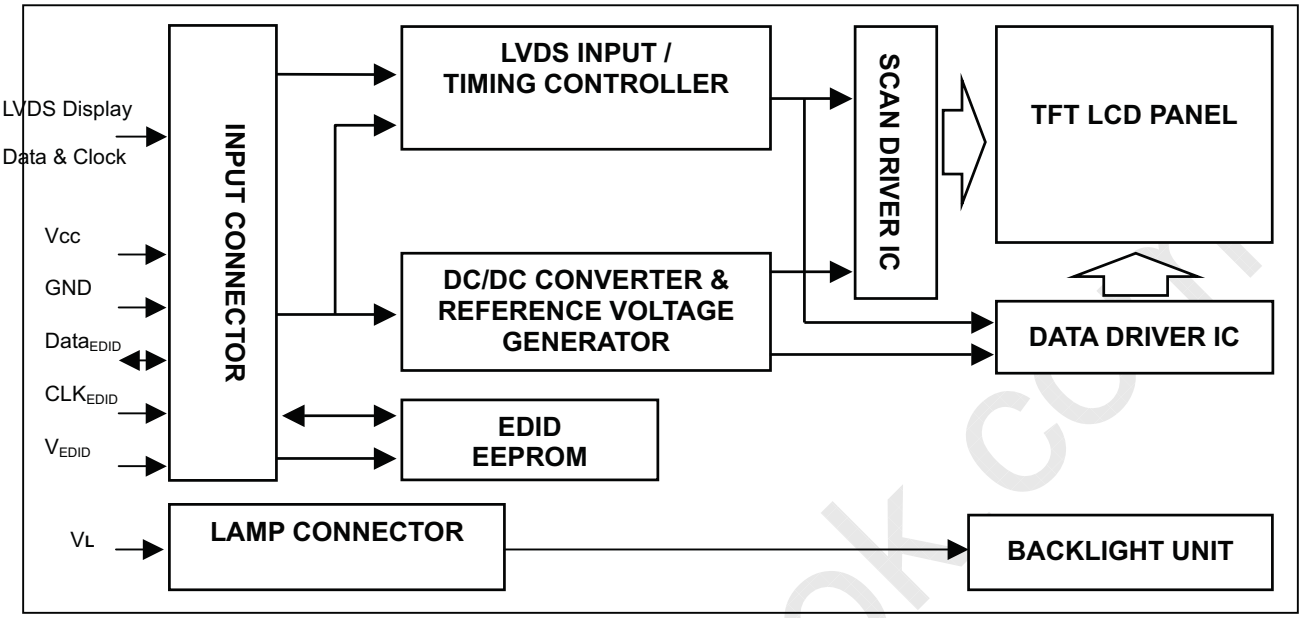
$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

4 BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT

5 INPUT TERMINAL PIN ASSIGNMENT

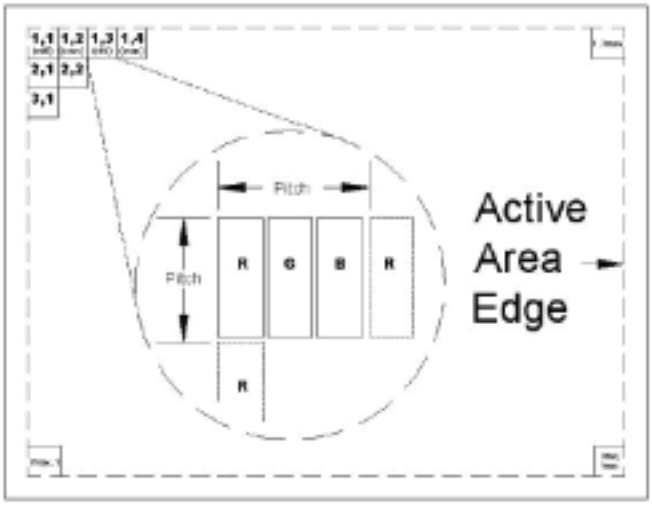
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V_{EDID}	DDC 3.3V Power		
5	BIST	Panel BIST enable		
6	CLK_{EDID}	DDC Clock		
7	$DATA_{EDID}$	DDC Data		-
8	RXO0-	LVDS Differential Data Input (Odd)	Negative	
9	RXO0+	LVDS Differential Data Input (Odd)	Positive	
10	Vss	Ground		
11	RXO1-	LVDS Differential Data Input (Odd)	Negative	
12	RXO1+	LVDS Differential Data Input (Odd)	Positive	
13	Vss	Ground		
14	RXO2-	LVDS Differential Data Input (Odd)	Negative	
15	RXO2+	LVDS Differential Data Input (Odd)	Positive	
16	Vss	Ground		
17	RXOC-	LVDS Clock Data Input (Odd)	Negative	
18	RXOC+	LVDS Clock Data Input (Odd)	Positive	
19	Vss	Ground		
20	RxE0-	LVDS Differential Data Input (Even)	Negative	
21	RxE0+	LVDS Differential Data Input (Even)	Positive	
22	Vss	Ground		
23	RxE1-	LVDS Differential Data Input (Even)	Negative	
24	RxE1+	LVDS Differential Data Input (Even)	Positive	
25	Vss	Ground		
26	RxE2-	LVDS Differential Data Input (Even)	Negative	
27	RxE2+	LVDS Differential Data Input (Even)	Positive	
28	Vss	Ground		
29	RXEC-	LVDS Clock Data Input (Even)	Negative	
30	RXEC+	LVDS Clock Data Input (Even)	Positive	

Note (1) Connector Part No.: JAE-FI-XB30SRL-HF11 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

Note (3) The first pixel is odd as shown in the following figure.



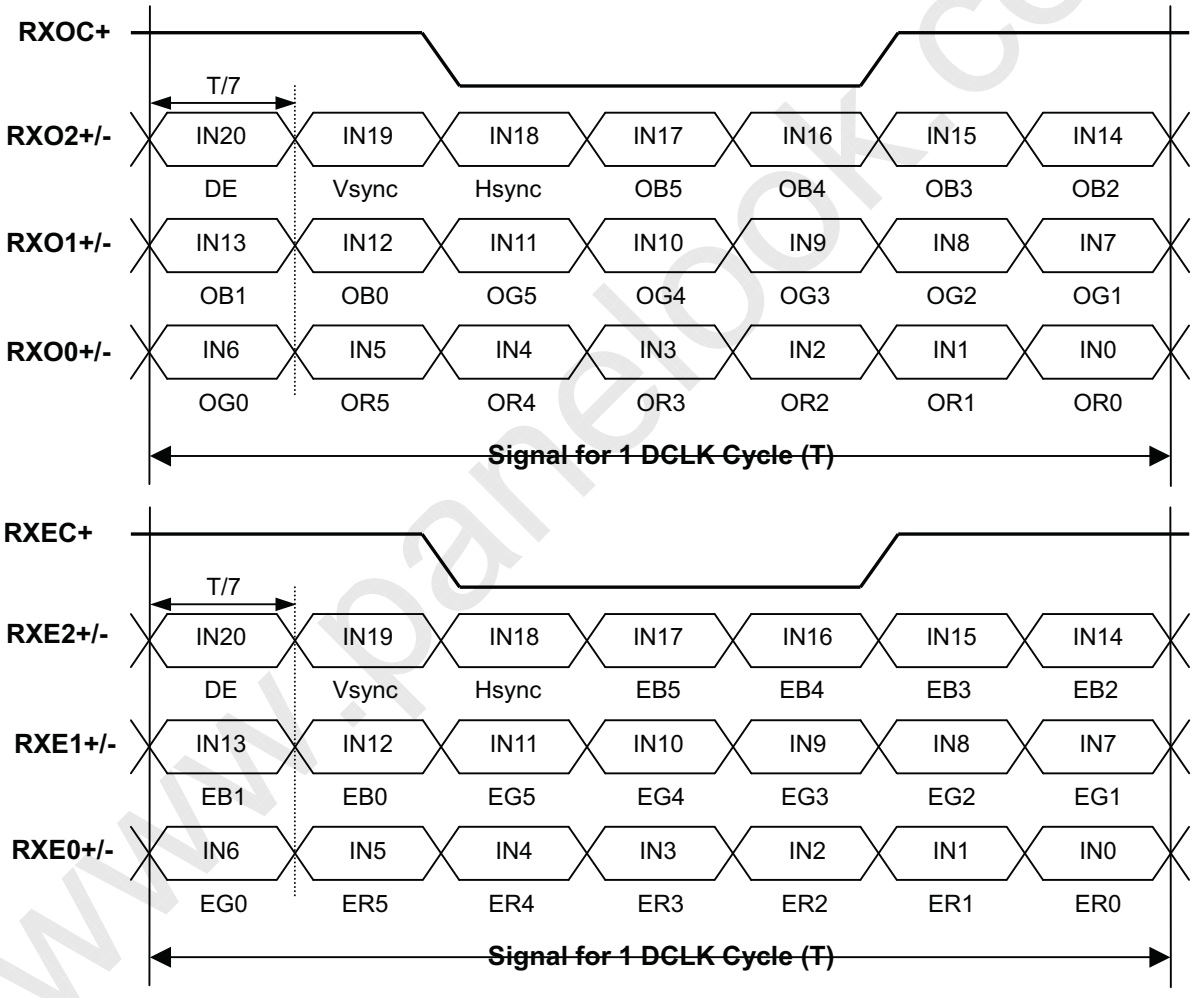
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	White

Note (1) Connector Part No.: JST- BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte #(decimal)	Byte #(hex)	Field Name and Comments	Value(hex)	Value(binary)
1	0	Header	00	00000000
2	1	Header	FF	11111111
3	2	Header	FF	11111111
4	3	Header	FF	11111111
5	4	Header	FF	11111111
6	5	Header	FF	11111111
7	6	Header	FF	11111111
8	7	Header	00	00000000
9	8	EISA ID manufacturer name (“CMO”)	0D	00001101
10	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
11	0A	ID product code (N141C1-L05)	33	00110011
12	0B	ID product code (hex LSB first; N141C1-L05)	14	00010100
13	0C	ID S/N (fixed “0”)	00	00000000
14	0D	ID S/N (fixed “0”)	00	00000000
15	0E	ID S/N (fixed “0”)	00	00000000
16	0F	ID S/N (fixed “0”)	00	00000000
17	10	Week of manufacture (fixed “00H”)	00	00000000
18	11	Year of manufacture (fixed “00H”)	00	00000000
19	12	EDID structure version # (“1”)	01	00000001
20	13	EDID revision # (“3”)	03	00000011
21	14	Video I/P definition (“digital”)	80	10000000
22	15	Active area horizontal 30.348cm	1E	00011110
23	16	Active area vertical 18.9675cm	13	00010011
24	17	Display Gamma (Gamma = ”2.2”)	78	01111000
25	18	Feature support (“Active off, RGB Color”)	0A	00001010
26	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	C0	11000000
27	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	05	00000101
28	1B	Rx=0.597	98	10011000
29	1C	Ry=0.340	57	01010111
30	1D	Gx=0.320	52	01010010
31	1E	Gy=0.535	89	10001001
32	1F	Bx=0.152	27	00100111
33	20	By=0.125	20	00100000
34	21	Wx=0.313	50	01010000
35	22	Wy=0.329	54	01010100
36	23	Established timings 1	00	00000000
37	24	Established timings 2 (1440*900@60Hz)	00	00000000
38	25	Manufacturer’s reserved timings	00	00000000
39	26	Standard timing ID # 1	01	00000001
40	27	Standard timing ID # 1	01	00000001
41	28	Standard timing ID # 2	01	00000001
42	29	Standard timing ID # 2	01	00000001

43	2A	Standard timing ID # 3	01	00000001
44	2B	Standard timing ID # 3	01	00000001
45	2C	Standard timing ID # 4	01	00000001
46	2D	Standard timing ID # 4	01	00000001
47	2E	Standard timing ID # 5	01	00000001
48	2F	Standard timing ID # 5	01	00000001
49	30	Standard timing ID # 6	01	00000001
50	31	Standard timing ID # 6	01	00000001
51	32	Standard timing ID # 7	01	00000001
52	33	Standard timing ID # 7	01	00000001
53	34	Standard timing ID # 8	01	00000001
54	35	Standard timing ID # 8	01	00000001
55	36	Detailed timing description # 1 Pixel clock (“88.75MHz”, According to VESA CVT Rev1.1)	AB	10101011
56	37	# 1 Pixel clock (hex LSB first)	22	00100010
57	38	# 1 H active (“1440”)	A0	10100000
58	39	# 1 H blank (“160”)	A0	10100000
59	3A	# 1 H active : H blank (“1440 : 160”)	50	01010000
60	3B	# 1 V active (”900”)	84	10000100
61	3C	# 1 V blank (”26”)	1A	00011010
62	3D	# 1 V active : V blank (”900 :26”)	30	00110000
63	3E	# 1 H sync offset (”48”)	30	00110000
64	3F	# 1 H sync pulse width ("32”)	20	00100000
65	40	# 1 V sync offset : V sync pulse width (”3 : 6”)	36	00110110
66	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 3 : 6”)	00	00000000
67	42	# 1 H image size (”303 mm”)	2F	00101111
68	43	# 1 V image size (”190 mm”)	BE	10111110
69	44	# 1 H image size : V image size (”303 : 190”)	10	00010000
70	45	# 1 H boarder (”0”)	00	00000000
71	46	# 1 V boarder (”0”)	00	00000000
72	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	19	00011001
73	48	Detailed timing description # 2 Pixel clock (“73.75 MHz”, According to VESA CVT Rev1.1)	CF	11001111
74	49	# 2 Pixel clock (hex LSB first)	1C	00011100
75	4A	# 2 H active (“1440”)	A0	10100000
76	4B	# 2 H blank (“160”)	A0	10100000
77	4C	# 2 H active : H blank (“1440 : 160”)	50	01010000
78	4D	# 2 V active (”900”)	84	10000100
79	4E	# 2 V blank (”22”)	16	00010110
80	4F	# 2 V active : V blank (”900 : 22”)	30	00110000
81	50	# 2 H sync offset (”48”)	30	00110000
82	51	# 2 H sync pulse width (”32”)	20	00100000
83	52	# 2 V sync offset : V sync pulse width (”3 : 6”)	36	00110110
84	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width (”48 : 32 : 3 : 6”)	00	00000000
85	54	# 2 H image size (”303 mm”)	2F	00101111
86	55	# 2 V image size (”190 mm”)	BE	10111110
87	56	# 2 H image size : V image size (”303 : 190”)	10	00010000
88	57	# 2 H boarder (”0”)	00	00000000
89	58	# 2 V boarder (”0”)	00	00000000

90	59	Module "A" Revision = Example: 00, 01, 02, 03, etc.	00	00000000
91	5A	Detailed timing description # 3	00	00000000
92	5B	# 3 Flag	00	00000000
93	5C	# 3 Reserved	00	00000000
94	5D	# 3 FE (hex) defines ASCII string (Model Name “N141C1”, ASCII)	FE	11111110
95	5E	# 3 Flag	00	00000000
96	5F	# Dell P/N "MC196" 1st character (“Y”)	59	01011001
97	60	# Dell P/N " MC196" 1st character (“Y”)	59	01011001
98	61	# Dell P/N " MC196" 1st character (“2”)	32	00110010
99	62	# Dell P/N " MC196" 1st character (“7”)	37	00110111
100	63	# Dell P/N " MC196" 1st character (“2”)	32	00110010
101	64	LCD Supplier EEDID Revision #: "1"	31	00110001
102	65	Manufacturer P/N ("N")	4E	01001110
103	66	Manufacturer P/N ("1")	31	00110001
104	67	Manufacturer P/N ("4")	34	00110100
105	68	Manufacturer P/N ("1")	31	00110001
106	69	Manufacturer P/N ("C")	43	01000011
107	6A	Manufacturer P/N ("1")	31	00110001
108	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
109	6C	Flag	00	00000000
110	6D	Flag	00	00000000
111	6E	Flag	00	00000000
112	6F	Data Type Tag:	FE	11111110
113	70	Flag	00	00000000
114	71	SMBUS value @ 10nits = 36d	24	00100100
115	72	SMBUS value @ 17nits = 51d	33	00110011
116	73	SMBUS value @ 24nits = 58d	3A	00111010
117	74	SMBUS value @ 30nits = 70d	46	01000110
118	75	SMBUS value @ 60nits = 98d	62	01100010
119	76	SMBUS value @ 110nits = 141d	8D	10001101
120	77	SMBUS value @ 150nits = 171d	AB	10101011
121	78	SMBUS value @ 220 nits = 255d	FF	11111111
122	79	Numbers of LVDS Recevier chip = 2	02	00000010
123	7A	BIST Enable: Yes = '01' No = '00' ("Yes")	01	00000001
124	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
125	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
127	7E	Extension flag	00	00000000
128	7F	Checksum	1A	00011010

6 INVERTER SPECIFICATION

6.1 Connector type

Input connector type: **LVC-D20SFYG** (HONDA)

Output connector: **JST SM02B-BHSS-1-TB** (JST)

6.2 Input connector pin assignment

6.2.1 Input Connector pin assignment:

Input connector		Comments
HONDA	**LVC-D20SFYG**	
Pin	**Function**	
1	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
2	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
5	GND	Ground
6	NC	No Connection
7	5VALW	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
8	GND	Ground
9	SMB_DAT	SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK	SMBus interface for sending brightness & contrast information to the inverter/panel
11	GND	Ground
12	INV_PWM	System side PWM input signal for brightness control
13	GND	Ground
14	NC	No Connection
15 ~ 20	NC	No Connection

6.2.2 Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.3 Output connector pin assignment

Pin	Name	Description
1	CFL-High	High-voltage output to the CCFL
2	CFL-Low	Low-voltage output to the CCFL

6.4 General electrical specification

6.4.1 Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.4.2 Electrical characteristics:

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Uint
1	Input Voltage	INV_SRC		7.5	14.4	21	V
2	Input Signal Level for 5VSUS	5VSUS		-	-	-	V
3	Input Signal Level for 5VALW	5VALW		4.75	5	5.2	V
4	Input Power	Pin(Max)	220nits@Vin=12V	-	-	5.5	W
5	Brightness Adjust (Lamp Current Control)	SMB_DAT	Control by SMBus(256 steps dimming control)	00H	-	FFH	-
6	Output Voltage	Vout	IL = 6.3mA(typ)	612	680	748	Vrms
7	Output Current	Iout (Min)	Vin=7.5V~21V SMB_DAT=00H Ta=25℃, after running 30 min.	1.5	1.8	2.1	mArms
		Iout (Max)	Vin=7.5V~21V SMB_DAT=FFH Ta=25℃, after running 30 min.	6	6.3	6.6	mArms
8	Operation Frequency	Freq	Vin=7.5V~21V	45	-	65	KHz
9	Burst mode frequency	f_B	Vin=7.5V~21V	200	-	220	Hz
10	Open Lamp Voltage	Vopen	No Load	1400	--	1800	Vrms
11	Striking Time	Ts	No Loadw	0.6	1	1.4	Sec
12	Efficiency	η	Vin=7.5V, SMB_DAT=FFH (RES LOAD=100K ohm)	80	-	-	%
13	Start and Delay Time		Vin=14.4V, SMB_DAT=00H	-	130	200	uS

14	Start –up time (Turn on delay time)		Vin=14.4V, SMB_DAT=FFH	-	-	0.1	Sec

- Input Voltage

  The operating input voltage of inverter shall be defined.

  The inverter shall ignite the CCFL lamp at minimum input voltage at any environment conditions.

- On/Off control

  Enable: At "**ON**" condition (FPBACK=Hi), enable the inverter.

  Disable: At "**OFF**" condition (FPBACK=Lo), disable the inverter.

- Quiescent current

  At the inverter "**OFF**" condition, input quiescent should be less than 0.1mA.

- Open lamp voltage

  The inverter start-up output voltage will be above "**Vopen**" for "**Ts**" minimum at any condition under specify until lamp to be ignited. The inverter should be shutdown if lamp ignition was failed in "**Ts**" maximum. The inverter shall be capable of withstanding the output connections open without component over-stress / fire / smoke /arc.

- Burst mode frequency

  The burst mode frequency should be in specification in any environment condition and electrical condition.

- Brightness control

  SM-BUS values for panel luminance are to be included in the on LCD board EEDID ROM chip table. The supplier will measure panel luminance in a system and define the SMBUS values for each of the 8 required luminance levels. The panel luminance, for which SMBUS values will be provided in the EEDID from byte # 113(hex #71), to byte # 120, (hex # 78), is show in the table below. The inverter supplier should provide these appropriate values to CMO.

Step Count	Step 1	Step 2	Step3	Step 4	Step 5	Step 6	Step 7	Step 8
Address	Byte 113	Byte 114	Byte 115	Byte 116	Byte 117	Byte 118	Byte 119	Byte 120
SM-Bus Data Value	24	33	3A	46	62	8D	AB	E8
Luminance (nits)	10	17	24	30	60	110	150	Max

- Output ripple ratio

  Ripple ratio = 2 * (Ipeak - Ivalley) / (Ipeak + Ivalley) * 100%

  The Ripple ratio should be less than 5% and ripple frequency should be less than 200 Hz.

- Power up Overshoot & Undershoot

  Overshoot & Undershoot at power up should not exceed the following limits.

Vin	Output current Io(rms)	Io (dI) Overshoot/Undershoot	Settling time (dT)
0→Vin(min.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(typ.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		

0→Vin(max.)	Io(max.) Io(min.)	150% / 50%	5 ms max.

dI=Imax.-Io or dI=(Io-Imin.)/Io

- Output connections short protection

  The inverter shall be capable of withstanding the output connections short without damage or over-stress. And the inverter maximum input power shall be limited within 1W.

6.4.3 Mechanical Drawing

6.4.4 Other Information

- Safety
  - The inverter shall meet the requirement of “Limited current circuits” in paragraphs 2.4.1 in IEC60950. There is no fire/smoke while simulating the component of the inverter open/short test.
  - The Inverter AND panel must be UL certified with CB certificate and LCC (Limited Current Circuit) test and test reports from UL. Inverter panel combo must pass Dell Safety requirements.
- EMI

  The inverter must meet the radiated limitation requirement of CISPR22 class B, FCC-B and VCCI level II with 6dB margin minimum while the inverter operating in the complete system.
- Environment Regulation
  - Follow the RoHS requirement.
  - Fill in CMO’s official document <<Environmentally Conscious Products Questionnaire for Suppliers of Materials, Parts, and Products>> and turn in to CMO before CMO’s specification approval process.
- Dell’s other requirements
  1. The inverter must not emit any audible noise.
  2. Please refer to CMO’s official document. “General Inverter Specification for LCD Module” for other general information such as reliability test, safety and etc..
  3. Please also refer to DELL’s official document about inverter:
     - LCD Backlight Design Spec X00-04
     - DELL’s LCD Inverter Qualification Plan, Rev. A00
     - Prohibited Components
     - “Holy Stone(禾申堂)”’s products are prohibited.

Confidential Notice

Remind that all the information described in this document is confidential. Please don’t reveal to other people else before getting CMO’s agreement.ibed in this document is confidential. Please don’t reveal to other people else before getting CMO’s agreement.

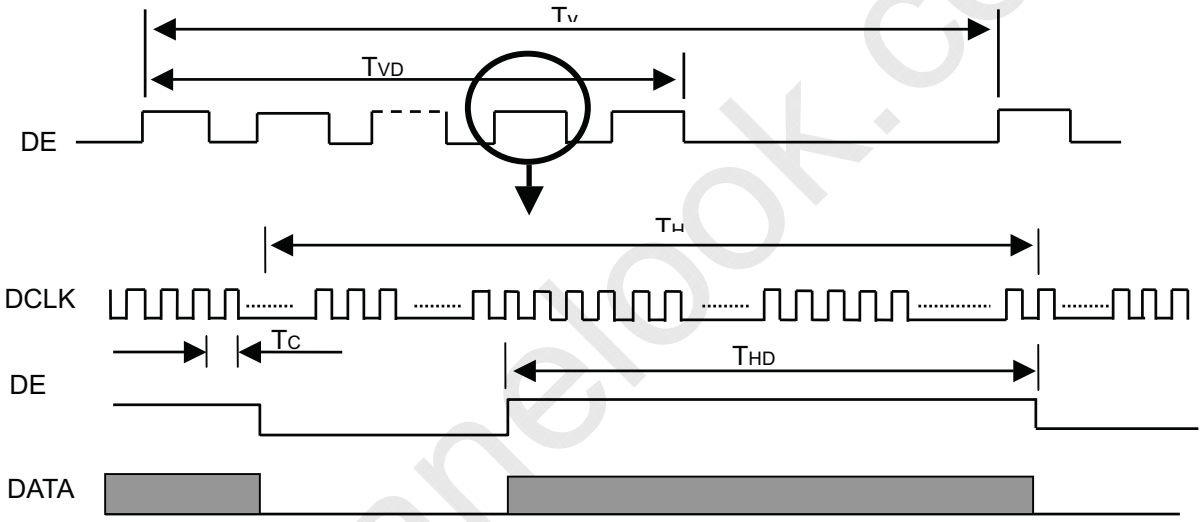
7 INTERFACE TIMING

7.1 INPUT SIGNAL TIMING SPECIFICATIONS

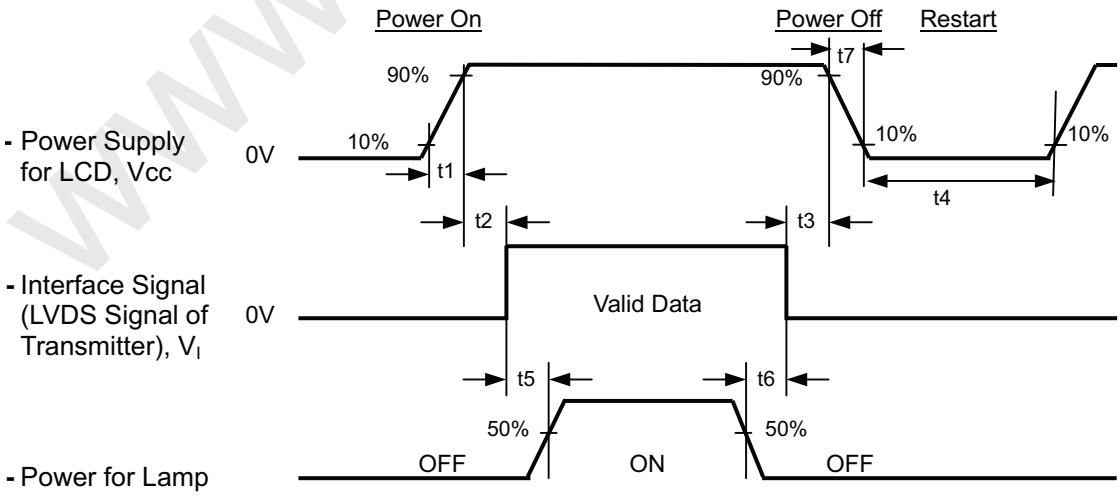
The specifications of input signal timing are as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	25	44.5	60	MHz	(2)
DE	Vertical Total Time	TV	910	926	1500	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	10	26	600	TH	
	Horizontal Total Time	TH	760	800	880	Tc	(2)
	Horizontal Active Display Period	THD	720	720	720	Tc	(2)
	Horizontal Active Blanking Period	THB	40	80	160	Tc	(2)

INPUT SIGNAL TIMING DIAGRAM



7.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5< t1 ≦ 10 msec

0 < t2 ≦ 50 msec

0 < t3 ≦ 50 msec

t4 ≧ 500 msec

t5 ≧ 200 msec

t6 ≧ 200 msec

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow

t7 ≧ 5 msec

8 OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

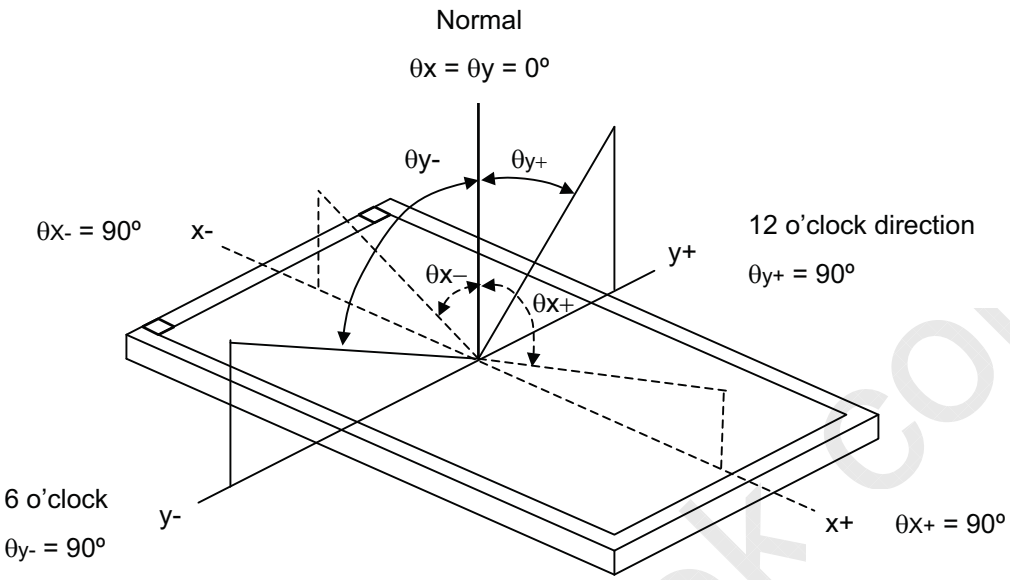
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	6	mA
Inverter Driving Frequency	F_L	61	KHz
Inverter	Sumida H05-4915		

The relative measurement methods of optical characteristics are shown in 8.2. The following items should be measured under the test conditions described in 8.1 and stable environment shown in Note (6).

8.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	**300**	**400**	-	-	(2), (5)
Response Time		T_R		-	5	10	ms	(3)
		T_F		-	11	16	ms	
Average Luminance of White		L_{5p}		**200**	**220**	-	cd/m^2	(4), (5)
Luminance Non-Uniformity		δW_{5p}		-	-	20	%	(5), (6)
		δW_{13p}		-	-	35	%	
Color Gamut		C.G		42	45	-	%	(5), (7)
Color Chromaticity	Red	Rx		TYP -0.02	0.590	TYP +0.02	-	(1), (5)
		Ry			0.340		-	
	Green	Gx			0.319		-	
		Gy			0.541		-	
	Blue	Bx			0.152		-	
		By			0.125		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45	-	Deg.	
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L_{63} / L_0

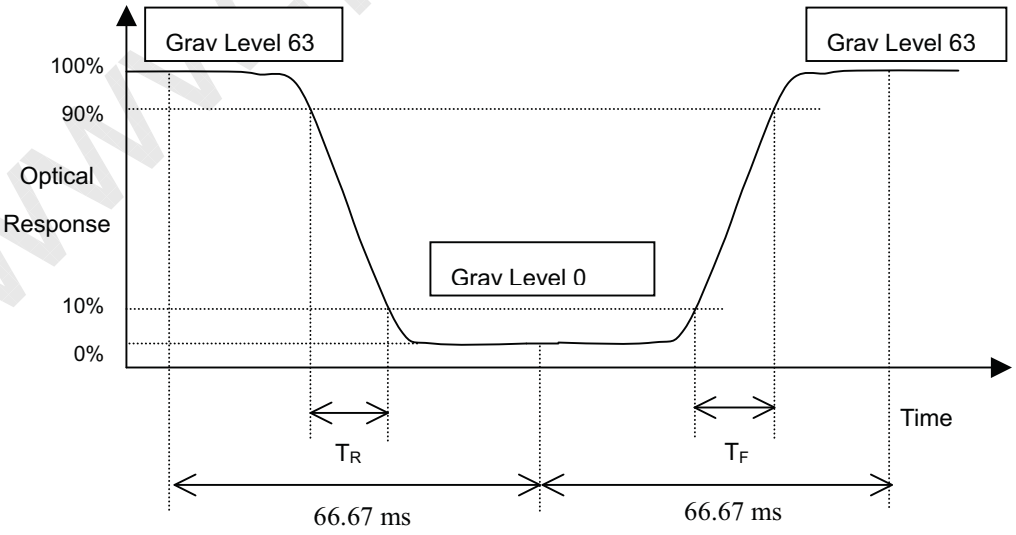
L_{63}: Luminance of gray level 63

L_0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{5p}):

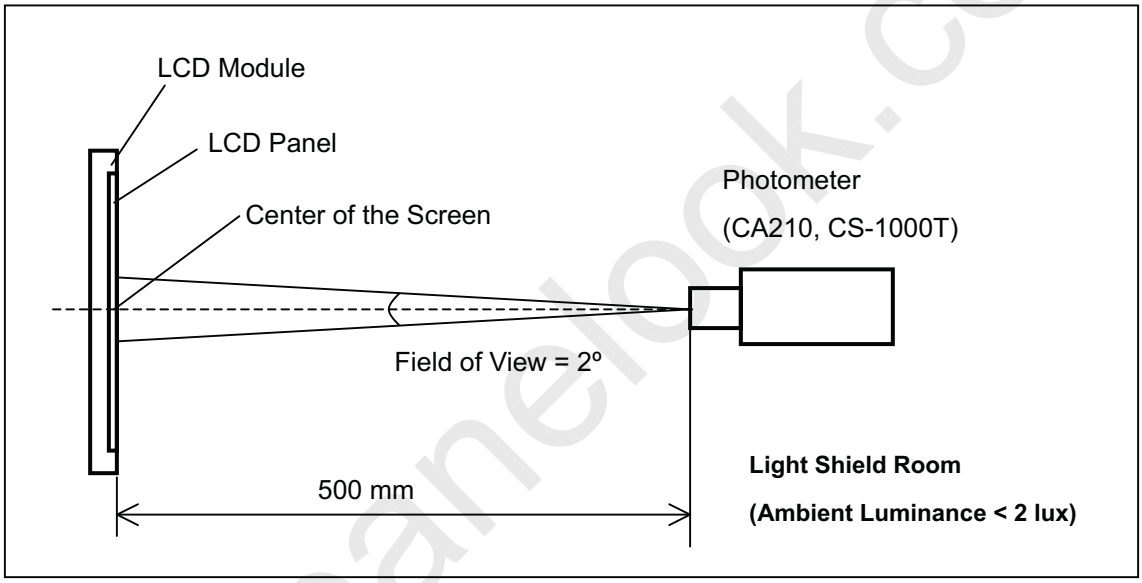
Measure the luminance of gray level 63 at 5 points

L_{5p} = [L (5)+ L (10)+ L (11)+ L (12)+ L (13)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

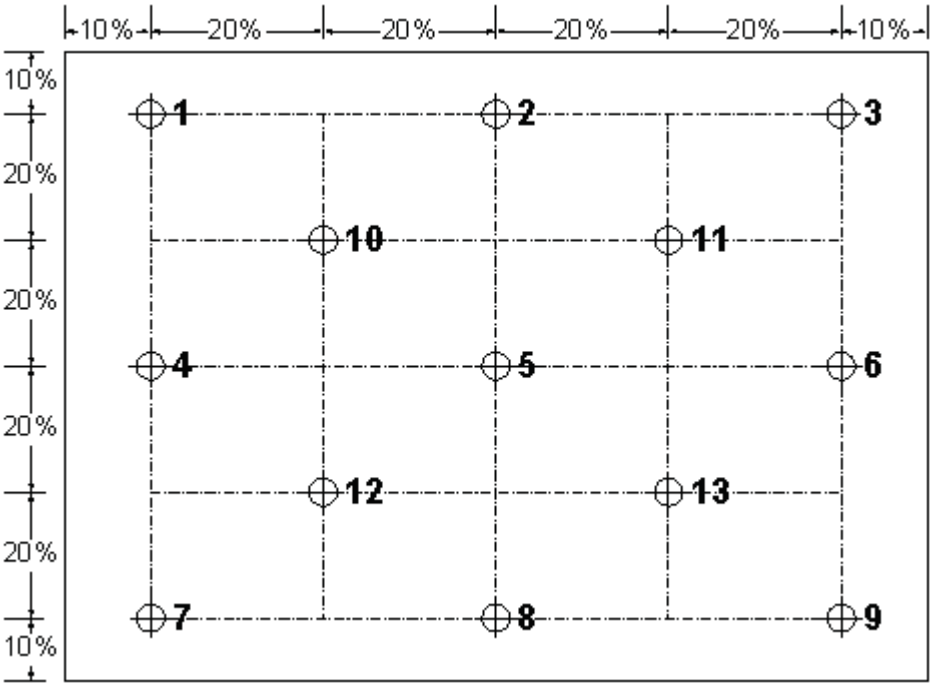


Note (6) Definition of White Variation (δW_{5p}, δW_{13p}):

Measure the luminance of gray level 63 at 5, 13 points

δW_{5p} ={1-{ Minimum [L (5)+ L (10)+ L (11)+ L (12)+ L (13)] / Maximum [L (5)+ L (10)+ L (11)+ L (12)+ L (13)]}} *100%

δW_{13p} ={1-{ Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}} *100%



Ⓧ : Test Point

X=1 to 5

Note (7) Definition of color gamut (C.G):

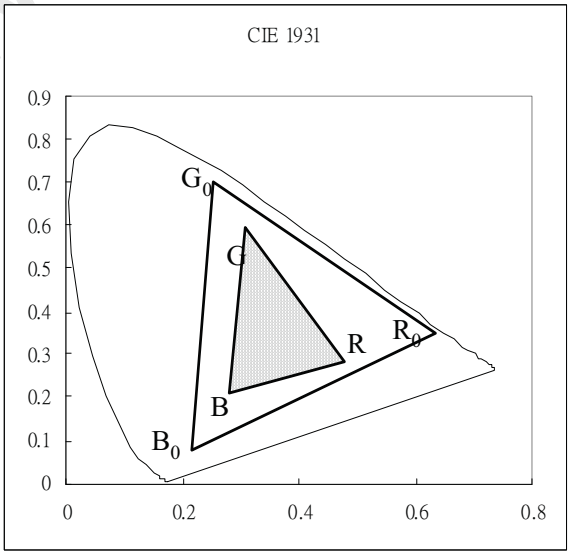
C.G= ΔR G B /ΔR_0 G_0 B_0,*100%

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

ΔR_0 G_0 B_0 : area of triangle defined by R_0, G_0, B_0

ΔR G B: area of triangle defined by R, G, B



9 PRECAUTIONS

9.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

9.2 SAFETY PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

9.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

10 PACKAGING

10.1 CARTON

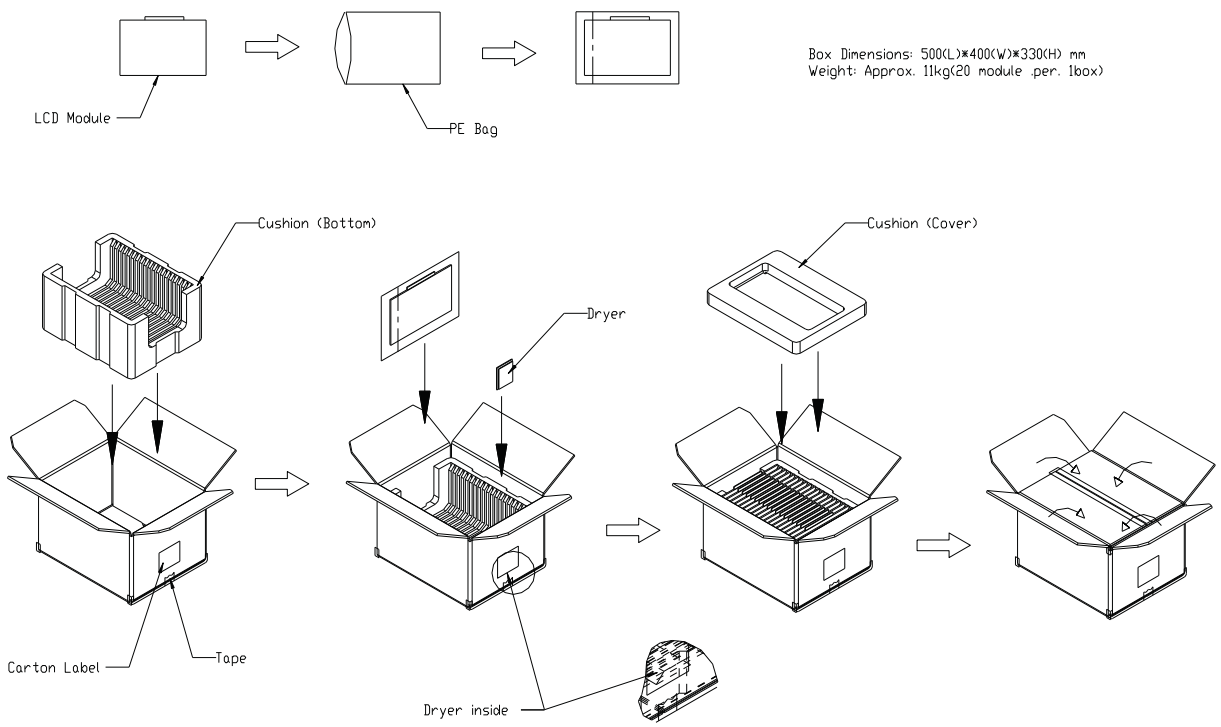


Figure. 10-1 Packing method

10.2 PALLET

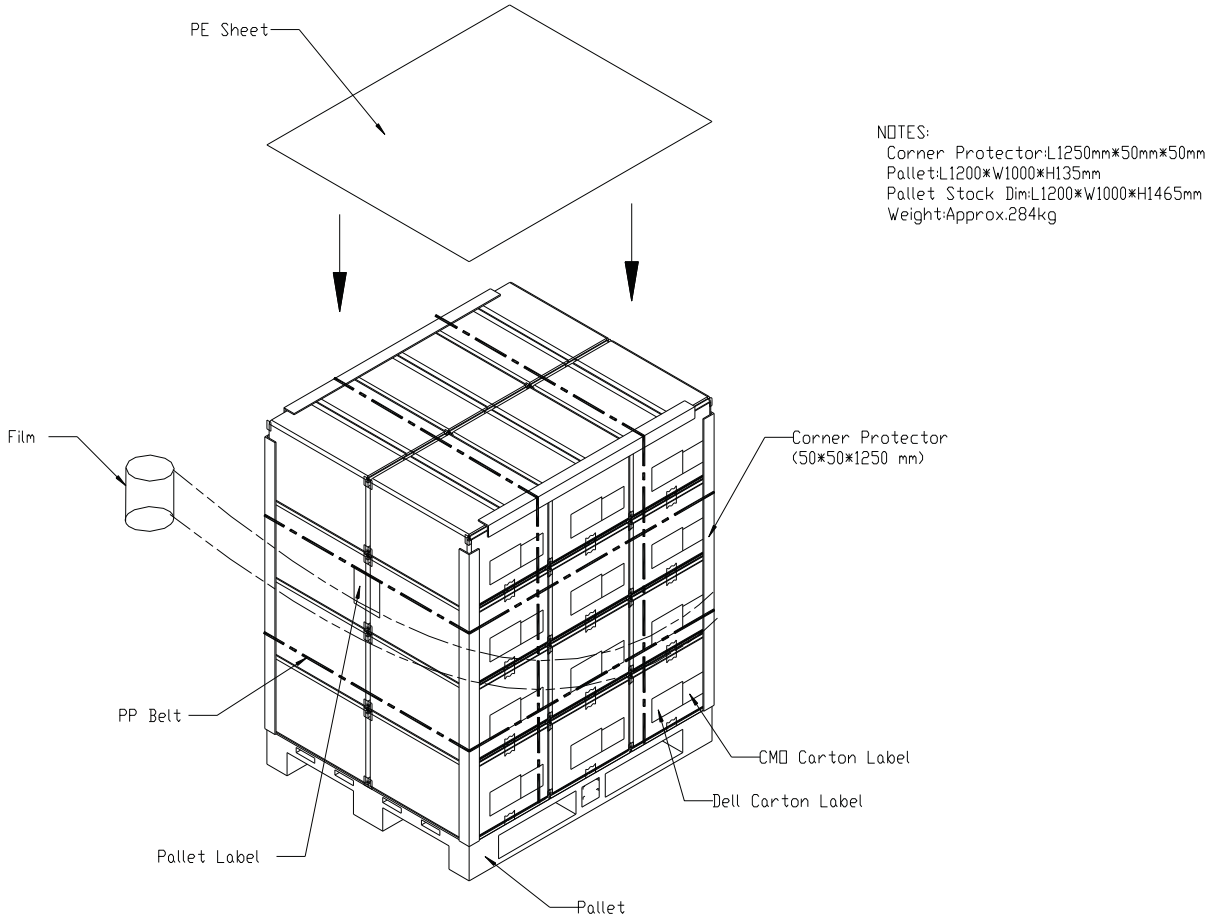
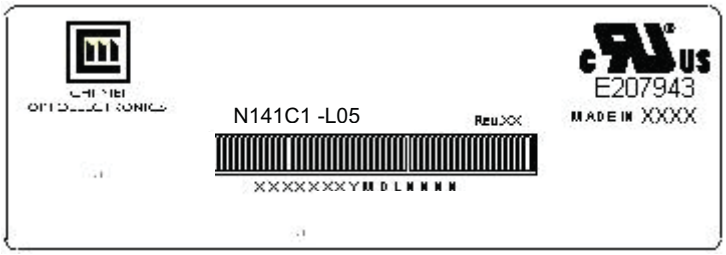


Figure. 10-2 Packing method

11 DEFINITION OF LABELS

11.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N141C1 - L05

(b) Revision: Rev. XX, for example: A1, …, C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D X N N N N

- Serial No.
- CMO Internal Use
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

(d) Production Location: MADE IN XXXX. XXXX stands for production location.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

11.2 CMO CARTON LABEL

(a) Production location: Made In XXXX. XXXX stands for production location.

11.3 PPID LABEL

pe J Label

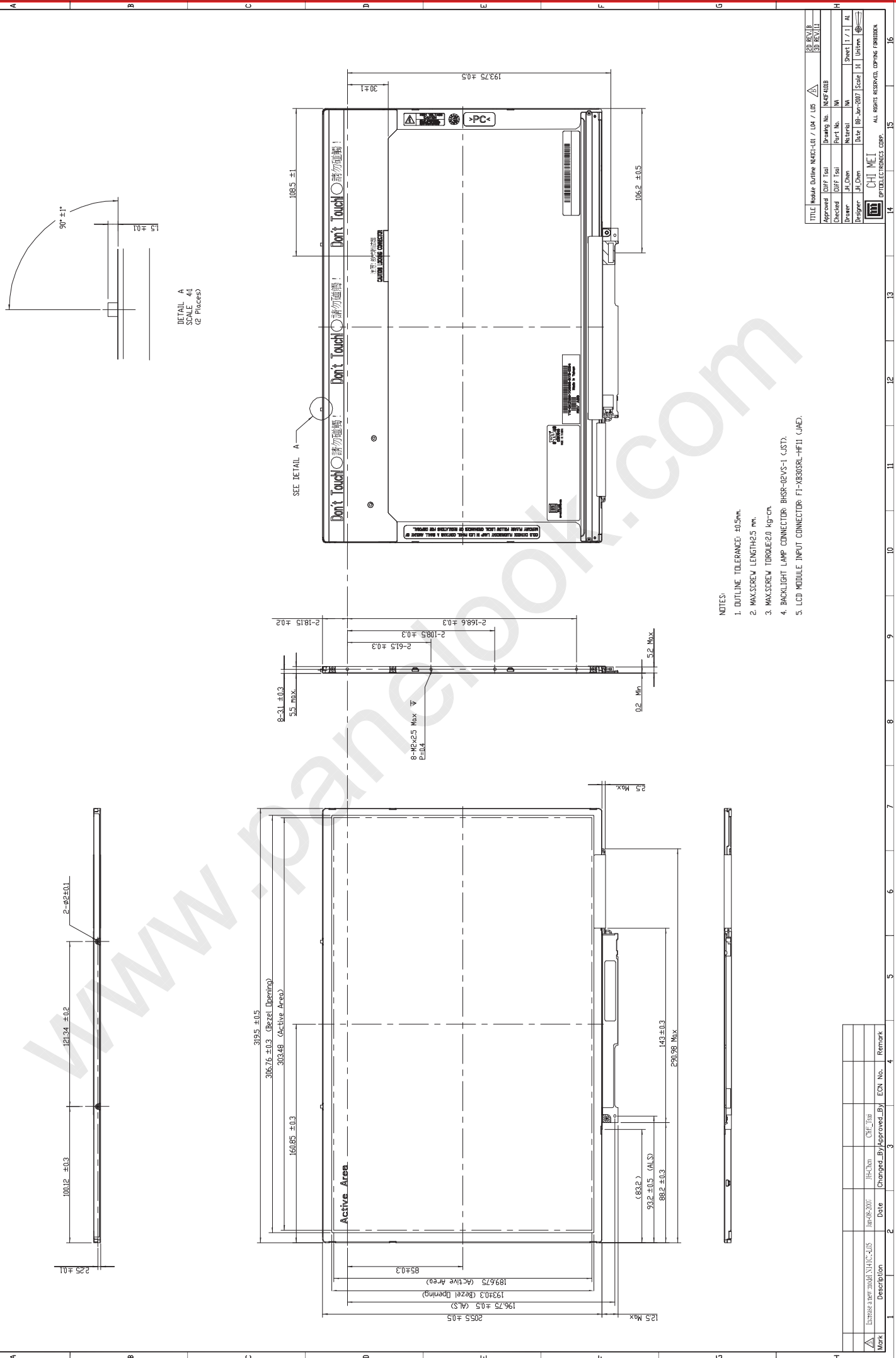
- –Verdana font or equivalent,bold
- –20pt.–all fields
- –203 DPI printer minimum
- –Code 128B
- –10–15 mil minimum narrow bar
- –.75"minimum barcode height
- –.10" or greater quiet zone
- –4.0" x 6.0" label size
- –Brady THT –25–402–1 or equivalent
- –Brady R6107 series ribbon or equivalent

11.4 PALLET LABEL

FROM :CMO Corporation Tainan, Taiwan 744 R.O.C			TO:DELL COMPUTER 2128 West Braker Austin TX
P.O.NUMBER 12345678			
			DELL P/N 12345
COUNTRY OF ORIGIN TW			
			PACKING LIST# 1234567890123
PACKING LIST QTY 654321			
			DESTINATION MAS LOC 60
DESTINATION LOCATION B4			
			AIRBILL NUMBER 12345678901234567890
PKG CNT 999 OF 999	BOX CNT 12345	REVISION A00-00	SHIP DATE Apr 29,2003
PART DESCRIPTION XXXXXXXXXXXXXXXXXXXXXXXXX 12345678901234567890123456789012345678901			

Type K Label

- –Verdana font or equivalent,bold
- –12pt.–all descript fields
- –10pt.–all data fields
- –203 DPI printer minimum
- –Code 128B
- –10 mil minimum narrow bar
- –.30–,50"minimum barcode height
- –.10" or greater quiet zone
- –4.0" x 6.5" label size
- –Brady THT –78–402–.9 or equivalent
- –Brady R6107 series ribbon or equivalent



NOTES:
1. OUTLINE TOLERANCE: ±0.5mm.
2. MAX.SCREW LENGTH:2.5 mm.
3. MAX.SCREW TORQUE:2.0 Kg-cm.
4. BACKLIGHT LAMP CONNECTOR: BHSR-02VS-1 (JST).
5. LCD MODULE INPUT CONNECTOR: FI-XB30SRL-HF11 (JAE).

TITLE	Module Outline NA4G1-L01 / L04 / L05			2D REV.B		
Approved	Cliff Tsai	Drawing No.	NA4F4018	3D REV.U4		
Checked	Cliff Tsai	Part No.	NA	Sheet	1 / 1	A4
Drawer	JH_Chen	Material	NA	Scale	1/4	Unit:mm
Designer	JH_Chen	Date	08-Jan-2007	CHI MEI OPTOELECTRONICS CORP.		

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Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
A	Release a new model N14IC-L05	Jan-08-2007	JH-Chen	Cliff_Tsai		