TFT LCD Tentative Specification

MODEL NO.: N141I4 - L01

Customer: Dell

Approved by:

Note:

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval
陳 95.6.16 永一	Wu Chao-Wen 6/15'06

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
0.1	JUN, 15,'06	All	All	Tentative specification was first issued.

1 GENERAL DESCRIPTION

1.1 OVERVIEW

N141I4 - L01 is a 14.1" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1280 x 800 WXGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is built in.

1.2 FEATURES

- Thin and Light Weight
- WXGA (1280 x 800 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock
- RoHS compliance

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	303.36(H) X 189.6(V)	mm	(1)
Bezel Opening Area	306.76 (H) x 193 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.237 (H) x 0.237 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Anti-glare , Haze 26,3H	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	319	319.5	320	mm	(1)
	Vertical(V)	205	205.5	206	mm	
	Depth(D)	--	5.2	5.5	mm	
Weight		--	390	405	g	(2)
Weight			400	415	g	(3)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions

(2) Weight without inverter

(3) Weight with inverter.

2 ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	200	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

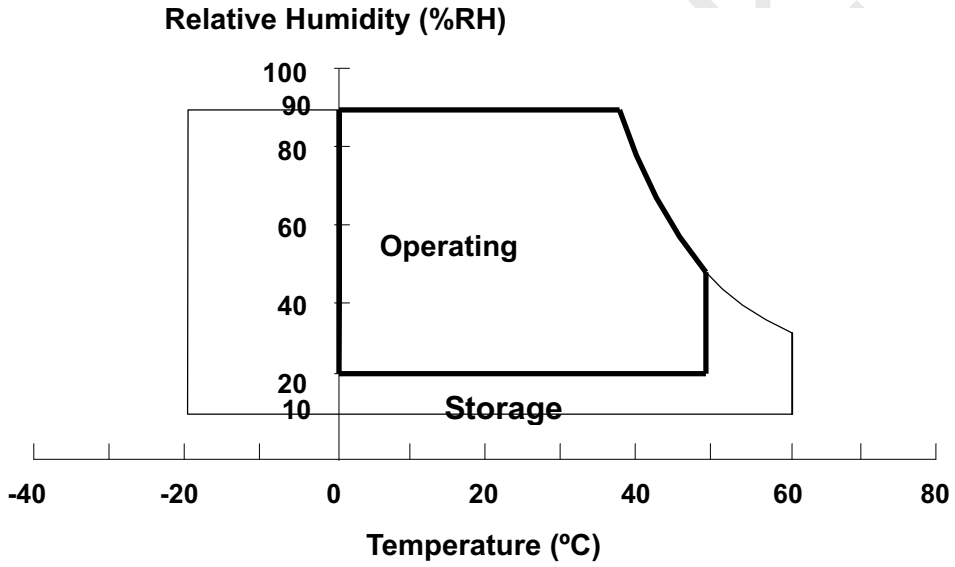
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The ambient temperature means the temperature of panel surface.

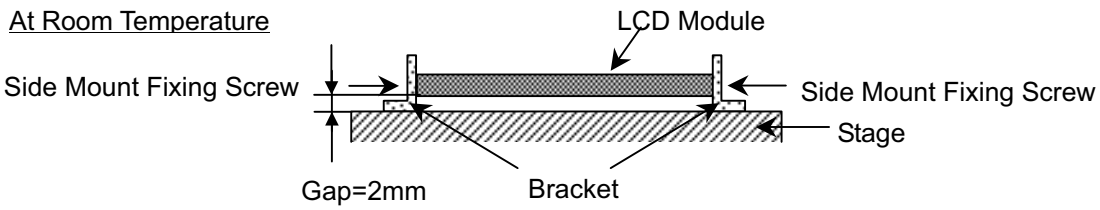


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (200G / 2ms) is half Sine Wave.

Note (4) 10 ~ 200 Hz, 30 min / Cycle, 1 cycles for each X, Y, Z axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	V_{CC}+0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2), I_L = 6.0 mA
Lamp Current	I_L	2.0	6.5	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	45	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3 ELECTRICAL CHARACTERISTICS

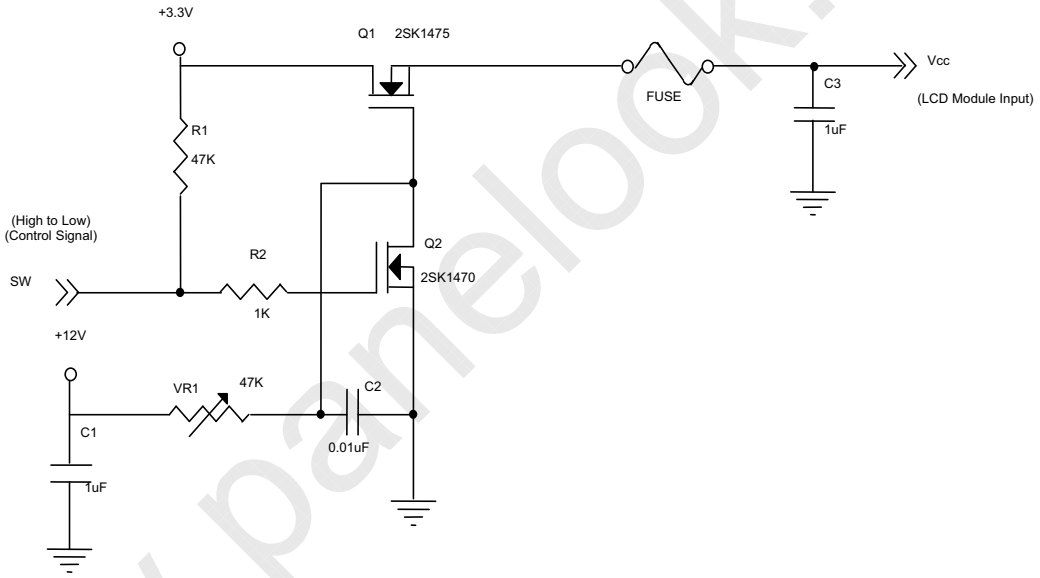
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

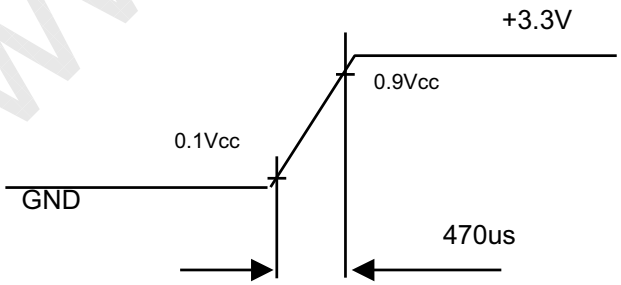
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	-	100	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Power Supply Current	White	Icc	-	335	375	mA	(3)a
	Black		-	400	450	mA	(3)b
Logical Input Voltage	"H" Level	V_{IL}	-	-	+100	mV	-
	"L" Level	V_{IH}	-100	-	-	mV	-
Terminating Resistor		R_T	-	100	-	Ohm	-
Power per EBL WG		P_{EBL}	-	TBD	-	W	(4)
LCD logic Power consumption		P_{LC}	-	-	TBD	W	(3)

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

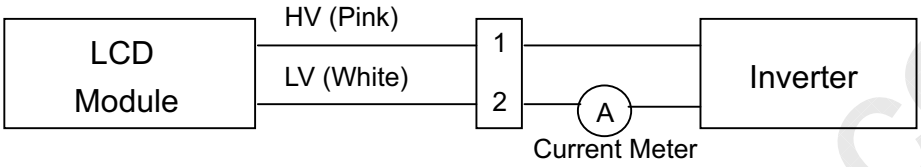
(c) Luminance: 60 nits.

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	612	680	748	V_{RMS}	I_L = 6.0 mA
Lamp Current	I_L	2.0	6.0	6.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	---	---	1370 (25 °C)	V_{RMS}	(2)
		---	---	1520 (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	45	---	80	KHz	(3)
Lamp Life Time	L_{BL}	15,000	---	---	Hrs	(5)
Power Consumption	P_{BL}	-	4.3	4.6	W	(4)

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) P_{BL} = Inverter input power

Inverter input power is measured at 8th step(the max brightness step) @Vin=12V

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I_L = 6 mArms until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and

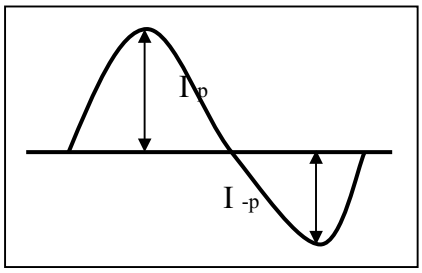
symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below.

b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

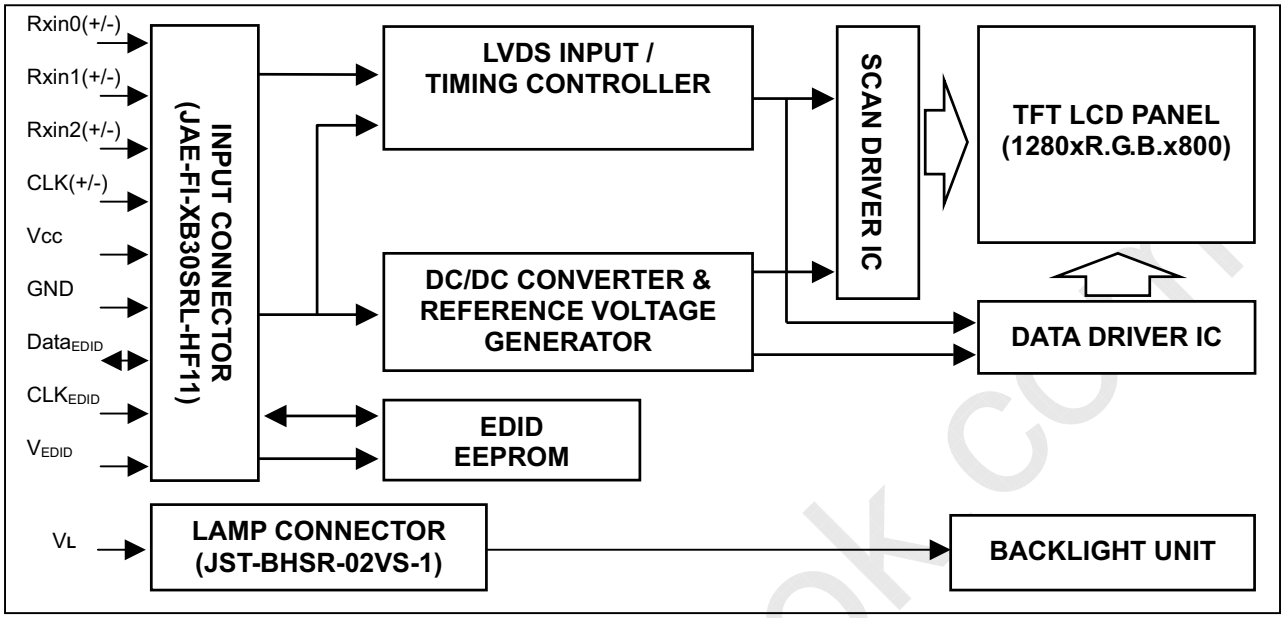
$$| I_p - I_{-p} | / I_{rms} * 100\%$$

* Distortion rate

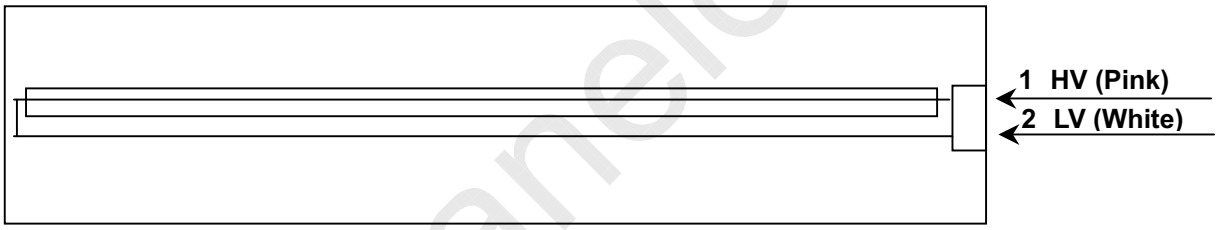
$$I_p \text{ (or } I_{-p}) / I_{rms}$$

4 BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5 INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V_{EDID}	DDC 3.3V Power		DDC 3.3V Power
5	BIST	Panel BIST enable		
6	CLK_{EDID}	DDC Clock		DDC Clock
7	$DATA_{EDID}$	DDC Data		DDC Data
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5,G0
9	Rxin0+	LVDS Differential Data Input	Positive	-
10	Vss	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	G1~G5, B0, B1
12	Rxin1+	LVDS Differential Data Input	Positive	-
13	Vss	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2~B5, DE, Hsync, Vsync
15	Rxin2+	LVDS Differential Data Input	Positive	
16	Vss	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	Vss	Ground		
20	NC	Non-Connection		
21	NC	Non-Connection		
22	NC	Non-Connection		
23	NC	Non-Connection		
24	NC	Non-Connection		
25	NC	Non-Connection		
26	NC	Non-Connection		
27	NC	Non-Connection		
28	NC	Non-Connection		
29	NC	Non-Connection		
30	NC	Non-Connection		

Note (1) Connector Part No.: JAE-FI-XB30SRL-HF11 or equivalent

Note (2) User's connector Part No: FI-X30C2L or equivalent

Note (3) The first pixel is even.

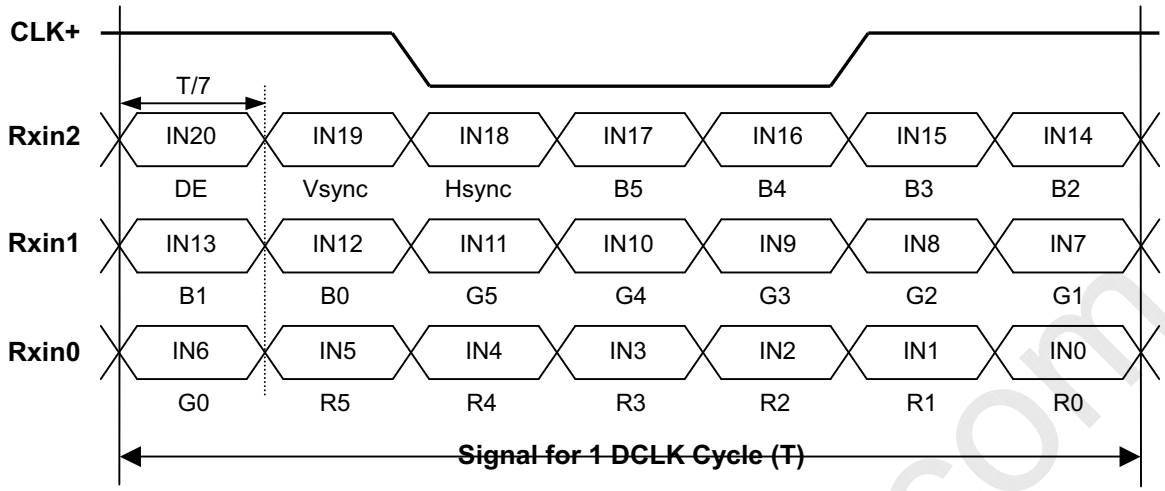
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	White

Note (1) Connector Part No.: JST- BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

TBD

6 INVERTER SPECIFICATION

6.1 Connector type

Input connector type: **LVC-D20SFYG** (HONDA)

Output connector: **JST SM02B-BHSS-1-TB** (JST)

6.2 Input connector pin assignment

Input Connector pin assignment:

Input connector		Comments
HONDA	**LVC-D20SFYG**	
Pin	**Function**	
1	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
2	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
5	GND	Ground
6	NC	No Connection
7	5VALW	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
8	GND	Ground
9	SMB_DAT	SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK	SMBus interface for sending brightness & contrast information to the inverter/panel
11	GND	Ground
12	INV_PWM	System side PWM input signal for brightness control
13	GND	Ground
14	NC	No Connection
15 ~ 20	NC	No Connection

Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.3 Output connector pin assignment

Pin	Name	Description
1	CFL-High	High-voltage output to the CCFL
2	CFL-Low	Low-voltage output to the CCFL

6.4 General electrical specification:

6.4.1 Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.4.2 Electrical characteristics:

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Uint
1	Input Voltage	INV_SRC		7.5	14.4	21	V
2	Input Signal Level for 5VSUS	5VSUS		4.85	5	5.2	V
3	Input Signal Level for 5VALW	5VALW		4.85	5	5.2	V
4	Input Power	Pin(Max)	Vin=7.5V~21V SMB_DAT=FFH	TBD	TBD	TBD	W
5	Lamp Power	Po	Vin=7.5V~21V SMB_DAT=FFH	TBD	4.02	4.6	W
6	Backlight ON/OFF Control	FPBACK=ON	Enable the inverter	2.0	-	5.25	V
		FPBACK=OFF	Disable the inverter	-0.3	-	0.8	V
7	Brightness Adjust (Lamp Current Control)	SMB_DAT	Control by SMBus(256 steps dimming control)	00H	-	FFH	-
8	Output Voltage	Vout	IL = 6.0mA(typ)	(603)	(670)	(737)	Vrms
9	Output Current	Iout (Min)	Vin=7.5V~21V SMB_DAT=00H Ta=25℃, after running 30 min.	2.0	2.3	2.6	mArms
		Iout (Max)	Vin=7.5V~21V SMB_DAT=FFH Ta=25℃, after running 30 min.	5.7	6.0	6.3	mArms
10	Operation Frequency	Freq	Vin=7.5V~21V	(45)	-	(65)	KHz

11	Burst mode frequency	f_B	Vin=7.5V~21V	200	-	220	Hz
12	Open Lamp Voltage	Vopen	No Load	(1500)	TBD	(1800)	Vrms
13	Striking Time	Ts	No Loadw	0.6	1	1.4	Sec
14	Efficiency	η	Vin=7.5V, SMB_DAT=FFH (RES LOAD=100K ohm)	(80)	-	-	%
15	Start and Delay Time		Vin=14.4V, SMB_DAT=00H	-	130	200	uS
16	Start –up time (Turn on delay time)		Vin=14.4V, SMB_DAT=FFH	-	-	0.1	Sec

- Input Voltage

  The operating input voltage of inverter shall be defined.

  The inverter shall ignite the CCFL lamp at minimum input voltage at any environment conditions.

- On/Off control

  Enable: At "**ON**" condition (FPBACK=Hi), enable the inverter.

  Disable: At "**OFF**" condition (FPBACK=Lo), disable the inverter.

- Quiescent current

  At the inverter "**OFF**" condition, input quiescent should be less than 0.1mA.

- Open lamp voltage

  The inverter start-up output voltage will be above "**Vopen**" for "**Ts**" minimum at any condition under specify until lamp to be ignited. The inverter should be shutdown if lamp ignition was failed in "**Ts**" maximum. The inverter shall be capable of withstanding the output connections open without component over-stress / fire / smoke /arc.

- Burst mode frequency

  The burst mode frequency should be in specification in any environment condition and electrical condition.

- Brightness control

  SM-BUS values for panel luminance are to be included in the on LCD board EEDID ROM chip table. The supplier will measure panel luminance in a system and define the SMBUS values for each of the 8 required luminance levels. The panel luminance, for which SMBUS values will be provided in the EEDID from byte # 113(hex #71), to byte # 120, (hex # 78), is show in the table below. The inverter supplier should provide these appropriate values to CMO.

Step Count	Step 1	Step 2	Step3	Step 4	Step 5	Step 6	Step 7	Step 8
Address	Byte 113	Byte 114	Byte 115	Byte 116	Byte 117	Byte 118	Byte 119	Byte 120
SM-Bus Data Value	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Luminance (nits)	10	17	24	30	60	110	150	Max

- Output ripple ratio

  Ripple ratio = 2 * (Ipeak - Ivalley) / (Ipeak + Ivalley) * 100%

  The Ripple ratio should be less than 5% and ripple frequency should be less than 200 Hz.

- Power up Overshoot & Undershoot

  Overshoot & Undershoot at power up should not exceed the following limits.

Vin	Output current Io(rms)	Io (dI) Overshoot/Undershoot	Settling time (dT)
0→Vin(min.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(typ.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(max.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		

dI=Imax.-Io or dI=(Io-Imin.)/Io

- Output connections short protection

  The inverter shall be capable of withstanding the output connections short without damage or over-stress. And the inverter maximum input power shall be limited within 1W.

6.4.3 Mechanical Drawing

Please refer to CMO's previous mechanical drawing of appendix (07N2737_mech.pdf)

6.4.4 Other Information

- Safety
  - The inverter shall meet the requirement of "Limited current circuits" in paragraphs 2.4.1 in IEC60950. There is no fire/smoke while simulating the component of the inverter open/short test.
  - The Inverter AND panel must be UL certified with CB certificate and LCC (Limited Current Circuit) test and test reports from UL. Inverter panel combo must pass Dell Safety requirements.
- EMI

  The inverter must meet the radiated limitation requirement of CISPR22 class B, FCC-B and VCCI level II with 6dB margin minimum while the inverter operating in the complete system.
- Environment Regulation
  - Follow the RoHS requirement.
  - Fill in CMO's official document <<Environmentally Conscious Products Questionnaire for Suppliers of Materials, Parts, and Products>> and turn in to CMO before CMO's specification approval process.
- Dell's other requirements
  1. The inverter must not emit any audible noise.
  2. Please refer to CMO's official document. "General Inverter Specification for LCD Module" for other general information such as reliability test, safety and etc..

3. Please also refer to DELL's official document about inverter:
   - DELL's Generic Inverter Specification, Rev. X00-00 –4.
   - DELL's LCD Inverter Qualification Plan, Rev. X04.

Confidential Notice

Remind that all the information described in this document is confidential. Please don't reveal to other people else before getting CMO's agreement.

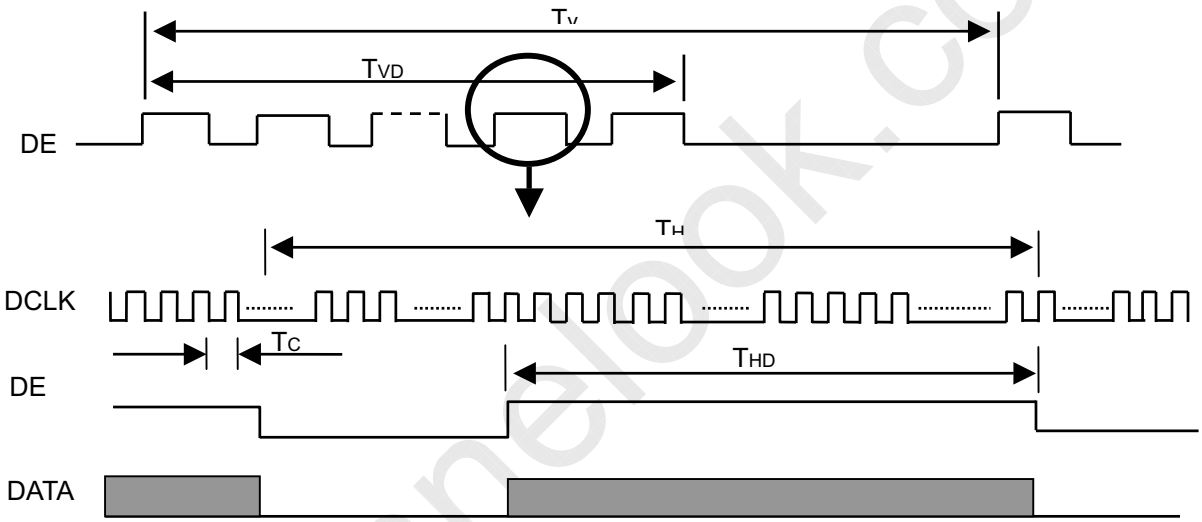
7 INTERFACE TIMING

7.1 INPUT SIGNAL TIMING SPECIFICATIONS

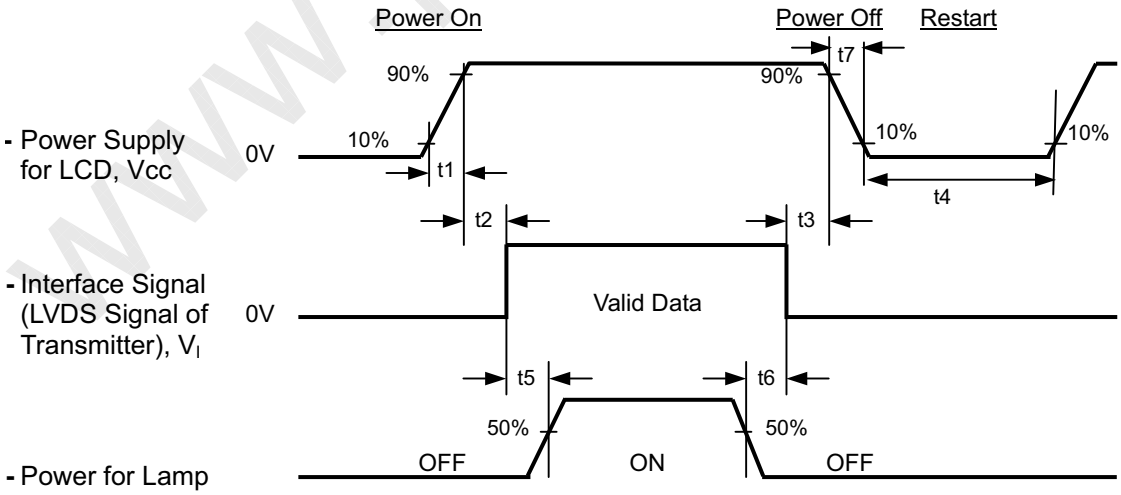
The specifications of input signal timing are as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	50	71.1	80	MHz	-
DE	Vertical Total Time	TV	810	823	2000	TH	-
	Vertical Addressing Time	TVD	800	800	800	TH	-
	Horizontal Total Time	TH	1360	1440	1900	Tc	-
	Horizontal Addressing Time	THD	1280	1280	1280	Tc	-

INPUT SIGNAL TIMING DIAGRAM



7.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5< t1 ≦ 10 msec

0 < t2 ≦ 50 msec

0 < t3 ≦ 50 msec

t4 ≧ 500 msec

t5 ≧ 200 msec

t6 ≧ 200 msec

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow

t7 ≧ 5 msec

8 OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

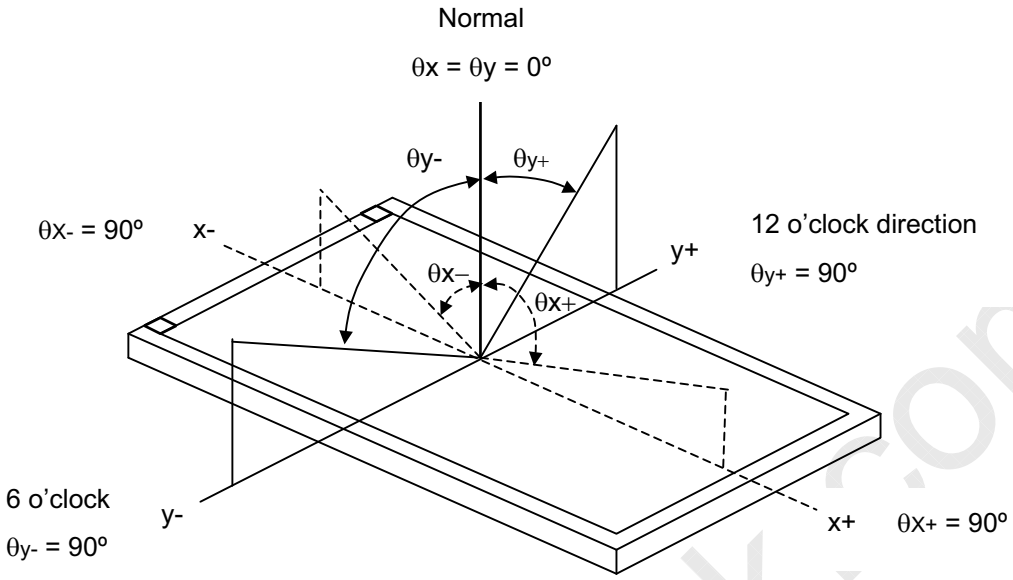
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	6	mA
Inverter Driving Frequency	F_L	61	KHz
Inverter	H05-4915		

The relative measurement methods of optical characteristics are shown in 8.2. The following items should be measured under the test conditions described in 8.1 and stable environment shown in Note (6).

8.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	400	600	-	-	(2), (5)
Response Time		T_R		-	3	8	ms	(3)
		T_F		-	7	12	ms	
Average Luminance of White		L_{5p}		180	220		cd/m^2	(4), (5)
Luminance Non-Uniformity		δW_{5p}		-	-	20	%	(5), (6)
		δW_{13p}		-	-	35	%	
Color Gamut		C.G		42	45	-	%	(5), (7)
Color Chromaticity	Red	Rx		TYP -0.02	(0.595)	TYP +0.02	-	(1), (5)
		Ry			(0.340)		-	
	Green	Gx			(0.302)		-	
		Gy			(0.521)		-	
	Blue	Bx			(0.150)		-	
		By			(0.112)		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45	-	Deg.	
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L_{63} / L_0

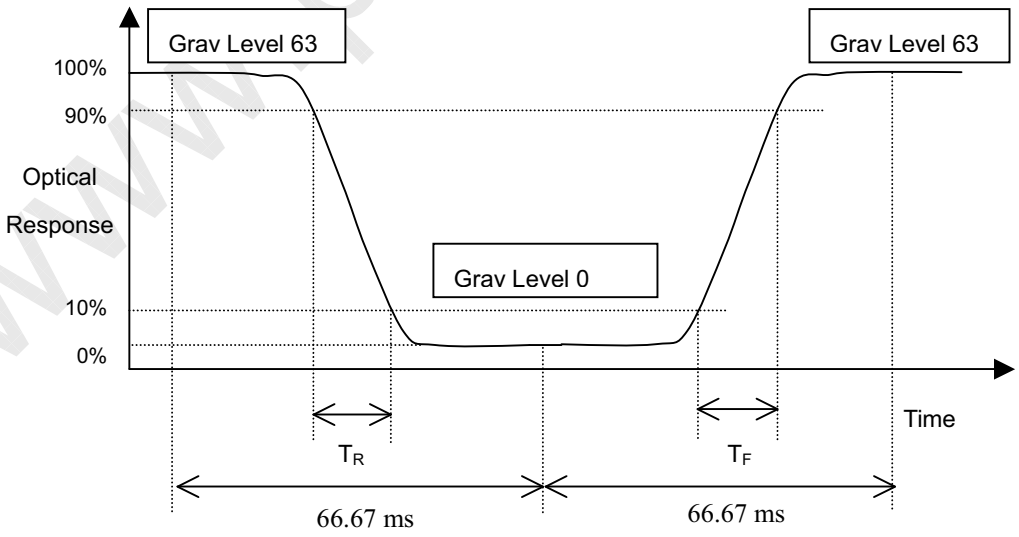
L_{63}: Luminance of gray level 63

L_0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{5p}):

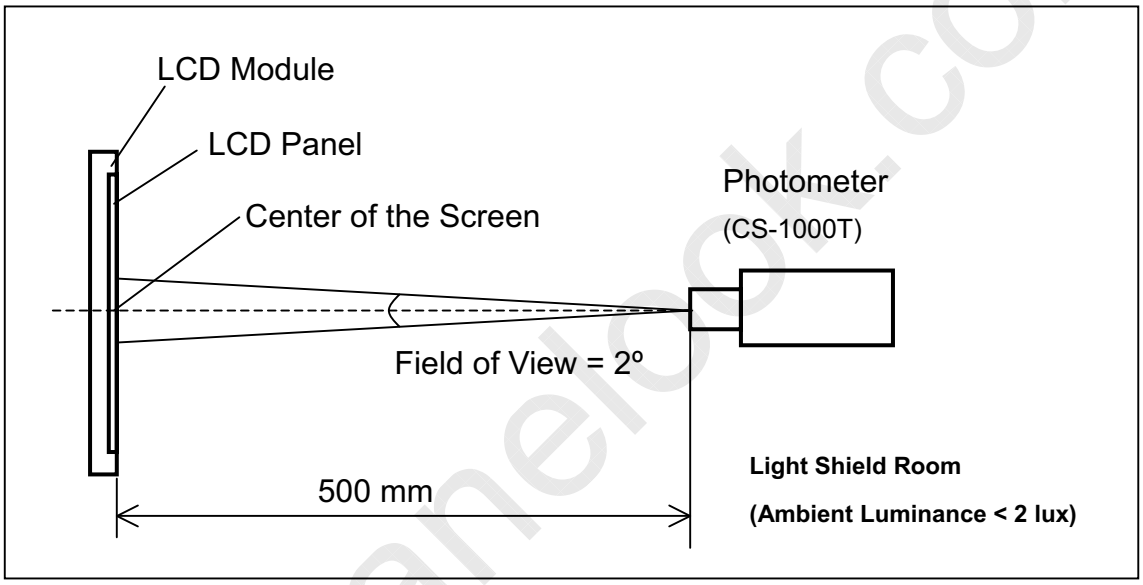
Measure the luminance of gray level 63 at 5 points

L_{5p} = [L (5)+ L (10)+ L (11)+ L (12)+ L (13)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

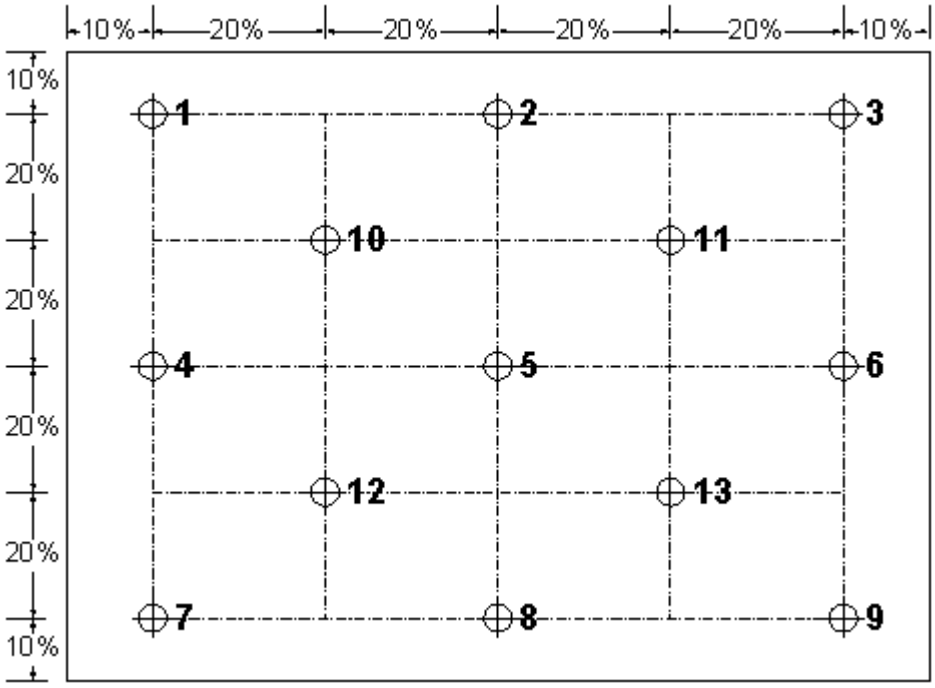


Note (6) Definition of White Variation (δW_{5p}, δW_{13p}):

Measure the luminance of gray level 63 at 5, 13 points

δW_{5p} ={1-{ Minimum [L (5)+ L (10)+ L (11)+ L (12)+ L (13)] / Maximum [L (5)+ L (10)+ L (11)+ L (12)+ L (13)]}} *100%

δW_{13p} ={1-{ Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}} *100%



Note (7) Definition of color gamut (C.G):

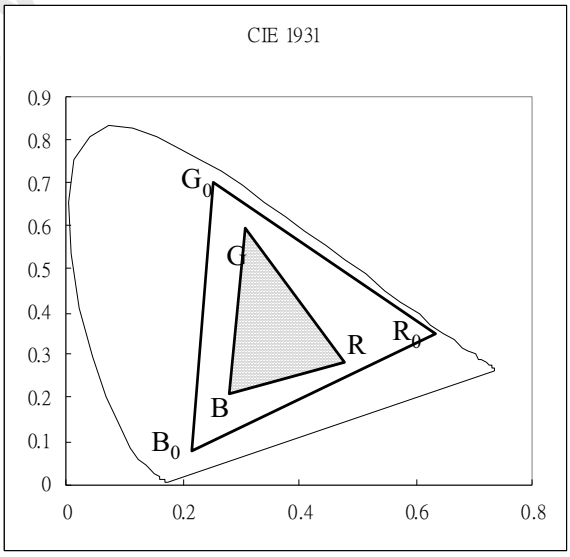
C.G= ΔR G B /ΔR_0 G_0 B_0,*100%

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

ΔR_0 G_0 B_0 : area of triangle defined by R_0, G_0, B_0

ΔR G B: area of triangle defined by R, G, B



9 PRECAUTIONS

9.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

9.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

10 PACKAGING

10.1 CARTON

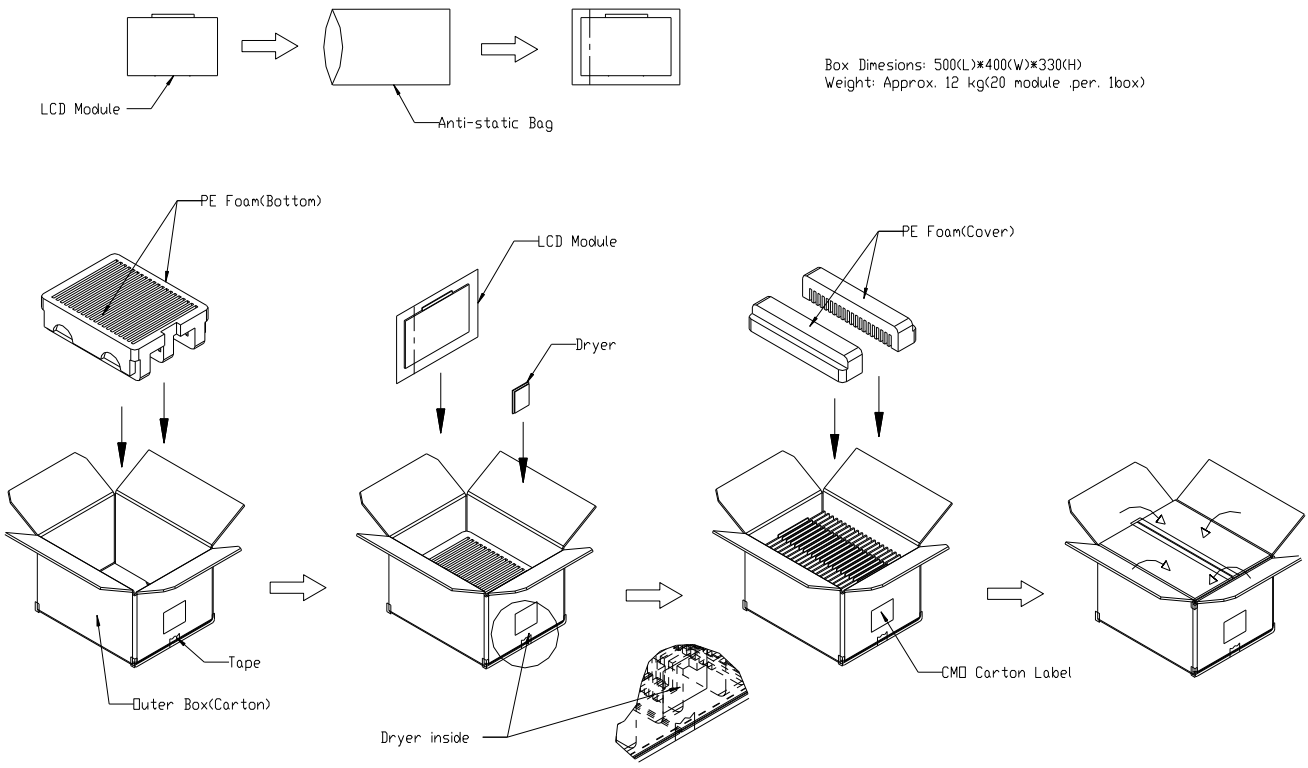


Figure. 9-1 Packing method

10.2 PALLET

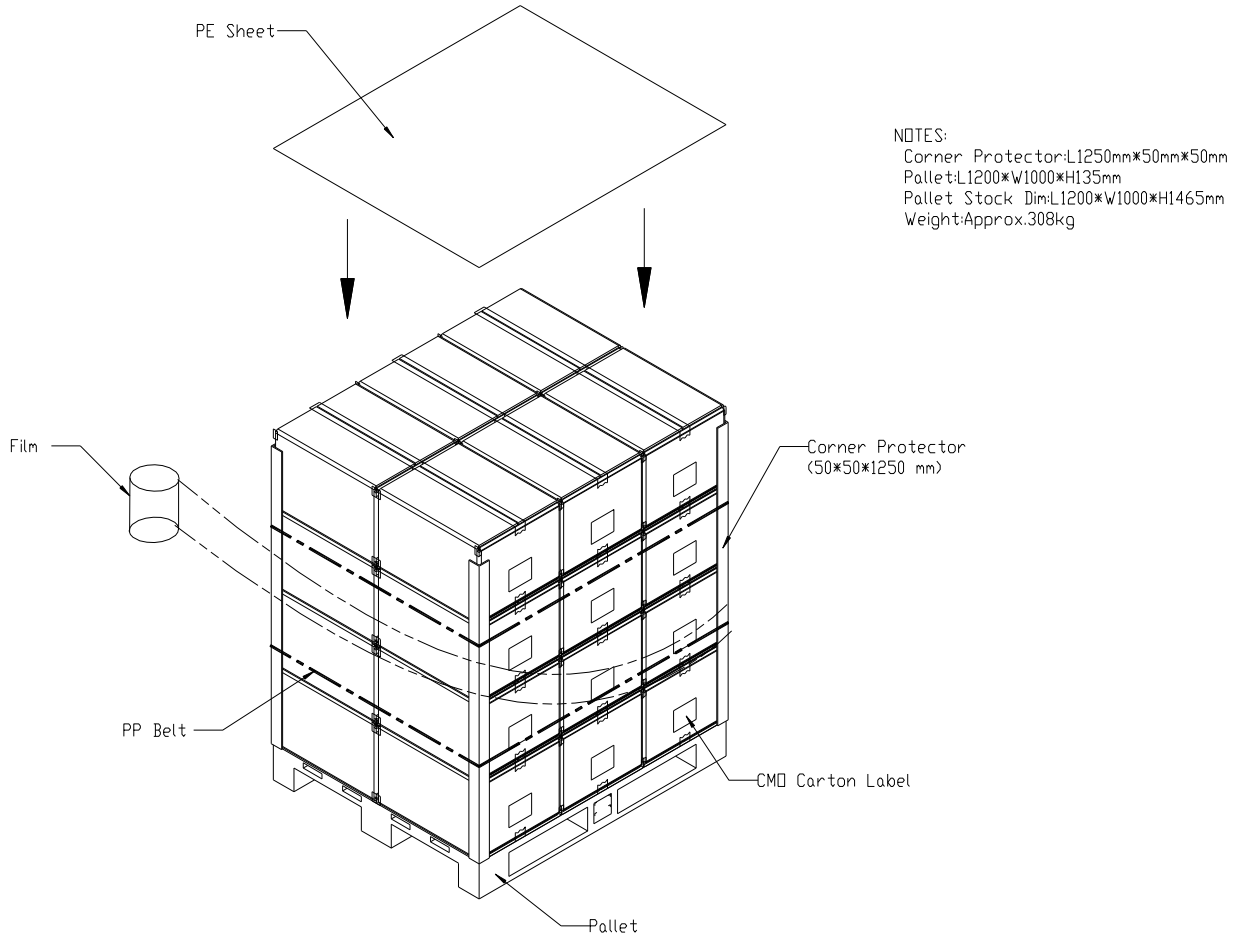
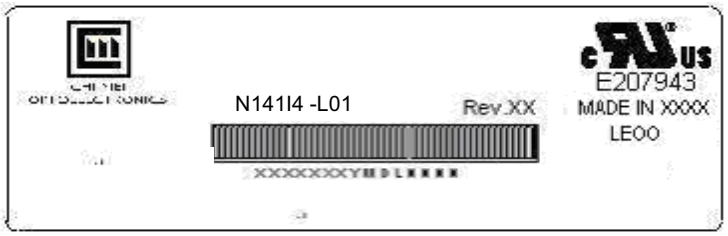


Figure. 9-2 Packing method

11 DEFINITION OF LABELS

11.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N141I4 - L01

(b) Revision: Rev. XX, for example: A1, …, C1, C2 …etc.

(c) Serial ID: X X X X X X X Y M D X N N N N

- Serial No.
- CMO Internal Use
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL/CB logo: "LEOO" especially stands for panel manufactured by CMO Ningbo satisfying UL/CB requirement. "LEOO" is the CMO's UL factory code for Ningbo factory.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

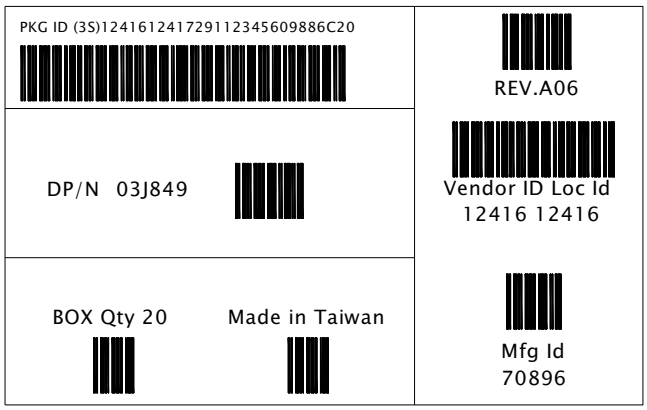
(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

11.2 CMO CARTON LABEL

(a) Production location: Made In XXXX. XXXX stands for production location.

11.3 CARTON LABEL



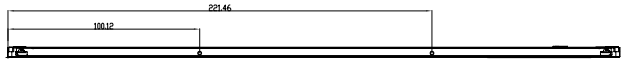
Type J Label

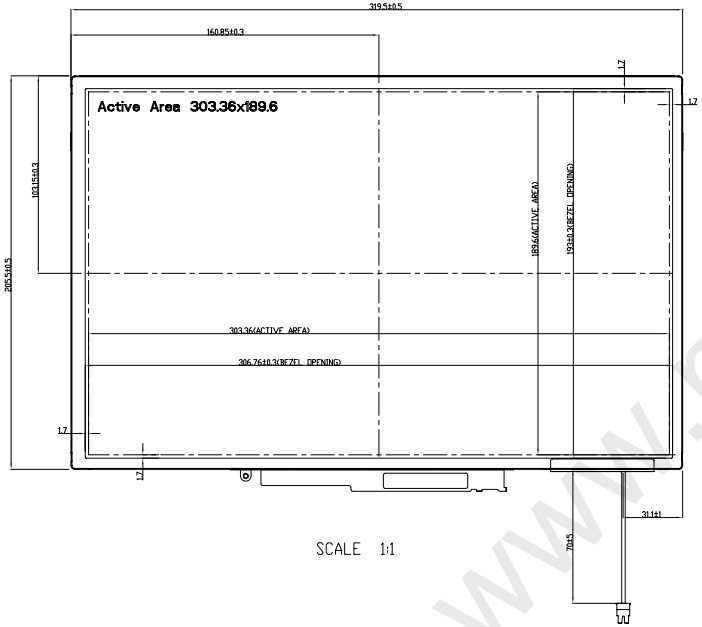
- Verdana font or equivalent,bold
- 20pt.–all fields
- 203 DPI printer minimum
- Code 128B
- 10–15 mil minimum narrow bar
- .75"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.0" label size
- Brady THT –25–402–1 or equivalent
- Brady R6107 series ribbon or equivalent

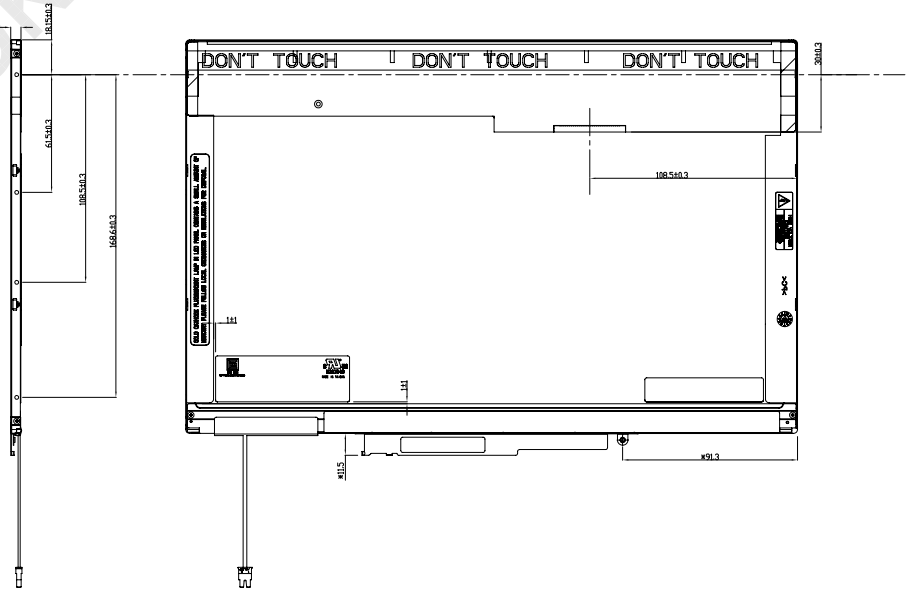
11.4 PALLET LABEL

Type K Label

- Verdana font or equivalent,bold
- 12pt.–all descript fields
- 10pt.–all data fields
- 203 DPI printer minimum
- Code 128B
- 10 mil minimum narrow bar
- .30–,50"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.5" label size
- Brady THT –78–402–.9 or equivalent
- Brady R6107 series ribbon or equivalent







Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	ASSY_MODULE_N141I4 (REF)				2D REV.	
					3D REV.	1.0+
Approved	Bill Sheu	Drawing No.	N141K41011			
Checked	Shunnan	Part No.	TBD			
Drawer	Gary Lu	Material	TBD	Sheet	1 / 1	A2
Designer	Gary Lu	Date	06-Jul-2006	Scale	1:1	Unit:mm

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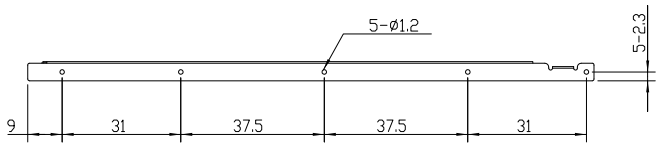
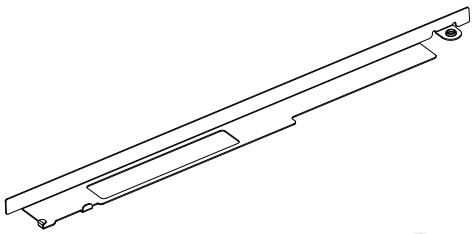
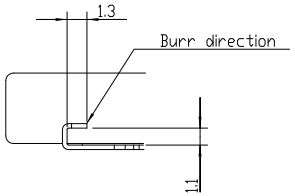
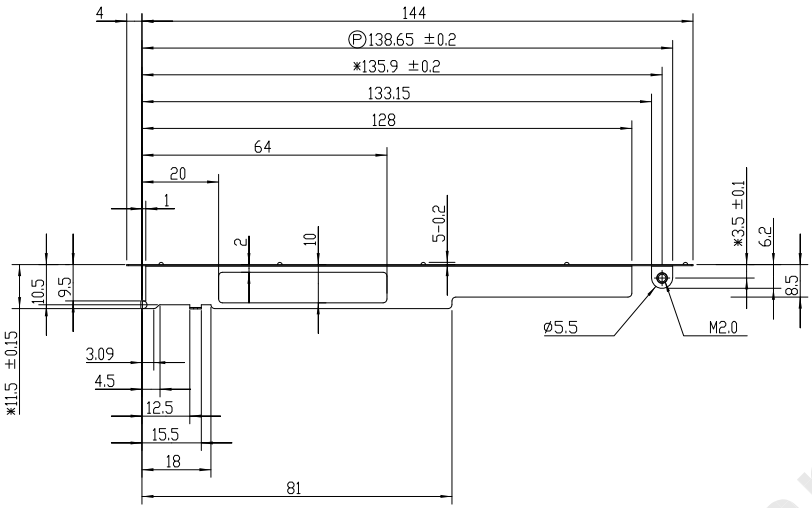
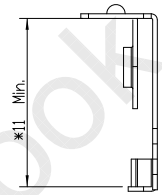




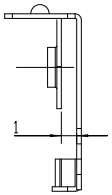


DETAIL A
SCALE 4:1





SECTION CC-CC
SCALE 4:1



SECTION BB-BB
SCALE 4:1

Notes:

1. Material: SUS304 2B, Thickness 0.3±0.05mm.
2. Part shall be clean and free from foreign material.
   Dirt, oil, grease, or other contaminants are not allowed.
3. All edges shall be conditioned for handling with industry standard burr no greater than 5% of material thickness.
4. Rotational torque: min. 2.5kgf-cm, rescrew 15 times use 2.0kgf-cm.
5. Burr direction is shown in Detail A.
6. Tolerance refer to the tolerance table unless otherwise stated.
7. All radius to be 1mm unless otherwise indicated.
* 8. Flatness: 0.3mm max.
9. "*" marks the critical dimensions.
10. " Ⓟ" marks the CPK dimensions.
11. Spot welding points: 5 places.

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

General Tolerance Unless Specified			
0–6	±0.1	300–600	±0.3
6–30	±0.15	600–	±0.6
30–300	±0.2	ANGLE	±1.0°

TITLE	M07 Inverter Bracket N141I1-L04, N141C1-L01/L04					2D REV.	A
						3D REV.	1.0
Approved	Yule Lin	Drawing No.	N141E2505A				
Checked	Yule Lin	Part No.	41-D005013				
Drawer	Shunnan	Material	SUS304 2B	Sheet	2 / 3	A2	
Designer	Shunnan	Date	11-Jan-2006	Scale	1:1	Unit:mm	

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