TO:

Accepted By: Date:

Customer's Acceptance Specification

Type 15.0 SXGA+ Color TFT/LCD Module
Model Name: N150P2-L06

Document Control Number: CAS I-N150P2-L06-FU01

Issued By: M. Suzuki M. Suzuki **Date: February 4, 2004**

Sales Support
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
February 4, 2004	CAS I-N150P2-L06-FU01	All	First Edition for FUJITSU LIMITED.

1.0 Handling Precautions

- If any signals or power lines deviate from the power on/off sequence, it may cause shorten the life of the LCD module.
- The LCD panel and the CFL are made of glass and may break or crack if dropped on a hard surface, so please handle them with care.
- CMOS ICs are included in the LCD panel. They should be handled with care, to prevent electrostatic discharge.
- Do not press the reflector sheet at the back of the LCD module to any directions.
- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- Please handle with care when mount in the system cover. Mechanical damage for lamp reflector ,for lamp cable and for lamp connector may cause safety problems.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.5, IEC60950 or UL60950), or be applied exemption conditions of flammability requirements (4.7.3.4, IEC60950 or UL60950) in an end product.
- The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL60950).
- The fluorescent lamp in the liquid crystal display(LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Never apply detergent or other liquid directly to the screen.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use solvents or abrasives.
- Do not touch the front screen surface in your system, even bezel.
- Gently wipe the covers and the screen with a soft cloth.

2.0 General Description

This specification applies to the Type 15.0 Color TFT/LCD Module 'N150P2-L06.

This module is designed for a display unit of a notebook style personal computer.

The screen format and electrical interface are intended to support the SXGA+ (1400(H) x 1050(V)) screen.

Support color is native 262k colors (RGB 6-bit data driver).

All input signals are LVDS (Low Voltage Differential Signaling) interface compatible.

This module does not contain an inverter card for backlight.

2.1 Characteristics

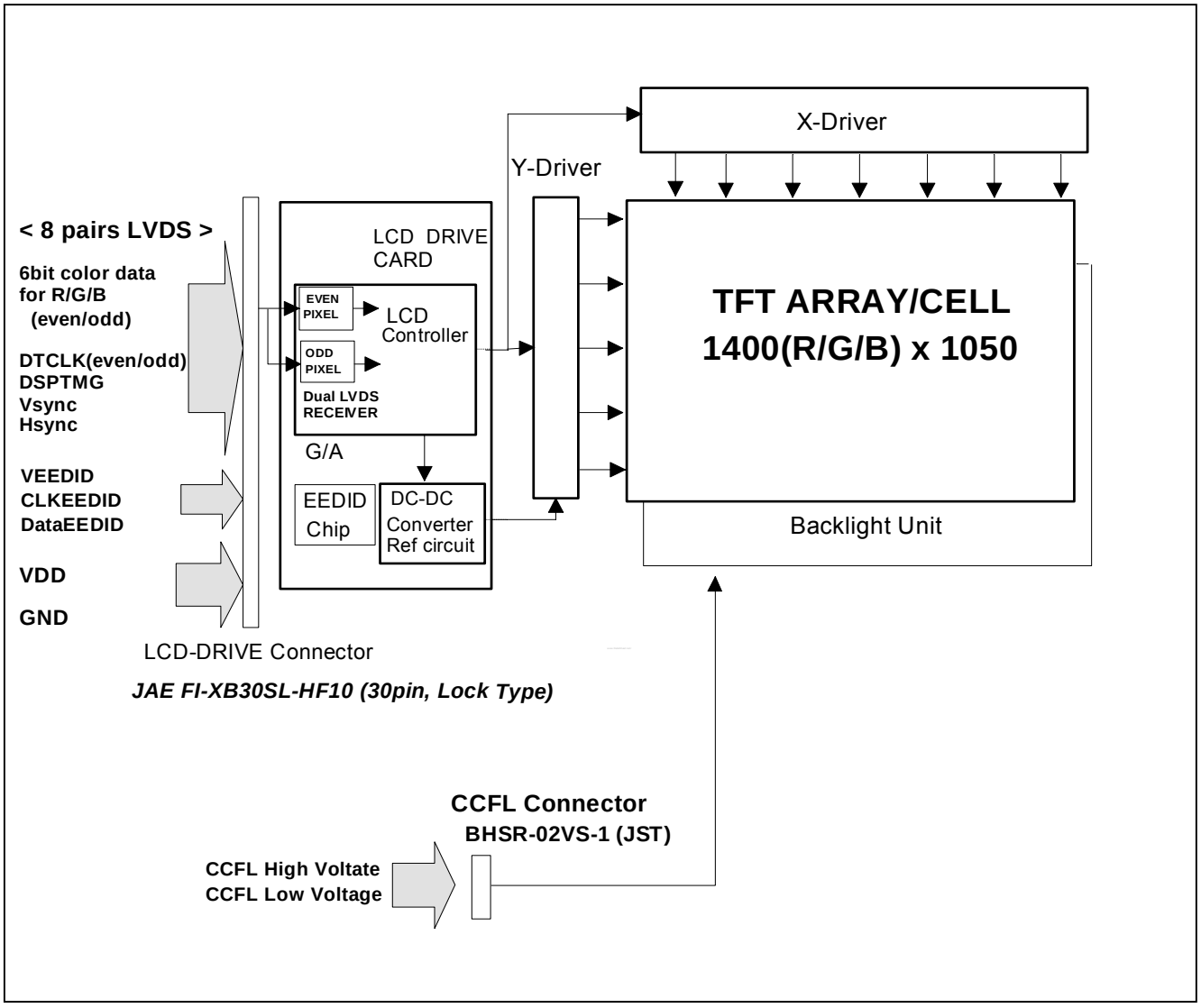
The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	381
Pixels H x V	1400(x3) x 1050
Active Area [mm]	304.5(H) x 228.375(V)
Pixel Pitch [mm]	0.2175(per one triad) x 0.2175
Pixel Arrangement	R,G,B Vertical Stripe
Weight [grams]	590 Max.
Physical Size [mm]	317.3(W) x 242.0(H) x 6.2(D) typ./6.5(D) MAX.
Display Mode	Normally White
Support Color	Native 262K colors (RGB 6-bit data driver)
White Luminance [cd/m^2] Design Point 2:(ICFL=6.5mA)	200 Typ.(center), 185 Typ.(5 points average)
Contrast Ratio	250 : 1 Typ.
Surface Treatment	Anti-Glare Treatment
Optical Rise Time/Fall Time [msec]	45 Typ.,50 Max.
Nominal Input Voltage VDD [Volt]	+3.3 Typ.
Power Consumption [Watt] Design Point 2:(ICFL=6.5mA)	Backlight : 4.1 Typ., 4.7 Max. Logic : 1.4 Typ., 2.6 Max.
Electrical Interface	8 pairs LVDS (Even/Odd R/G/B EEDID (Clock, data) Data (6bit), 3sync signals, Clock)
CFL Cable Length [mm]	105 Typ.
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 15.0 Color TFT/LCD Module.

The first LVDS port transmits even pixels while the second LVDS port transmits odd pixels.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows:

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	+4.0	V	
Input Voltage of Signal	Other Inputs	-0.3	VDD+0.3	V	
Lamp Ignition Voltage	VCFL	-	+1,650	Vrms	Ta = 0 [deg.C]
CFL Current	ICFL	-	7	mArms	
CFL Peak Inrush Current	ICFLP	-	20	mArms	Ta = 25 [deg.C] **(Note 1)**
Operating Temperature	TOP	0	+50	deg.C	**(Note 2)**
Operating Relative Humidity	HOP	8	95	%RH	**(Note 2)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 2)**
Storage Relative Humidity	HST	5	95	%RH	**(Note 2)**
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note:

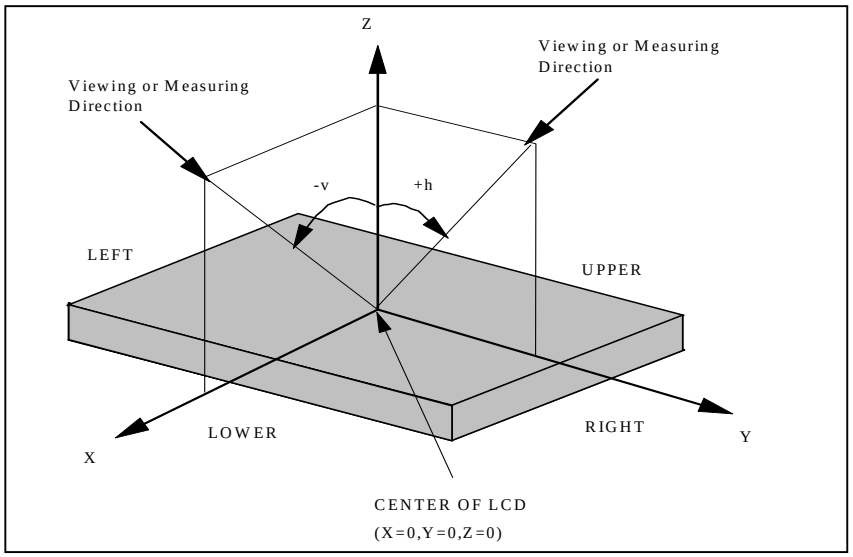
1. Duration: 50 [msec] Max.
2. Maximum Wet-Bulb should be 39 degree C and No condensation.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees)	Horizontal (Right)	40 Min.	-
	K≧10 (Left)	40 Min.	-
	Vertical (Upper)	15 Min.	-
K: Contrast Ratio	K≧10 (Lower)	30 Min.	-
Contrast ratio		250	200 Min.
Response Time (ms)	Rising	45	50 Max.
	Falling	45	50 Max.
Color Chromaticity (CIE)	Red x	0.577	±0.030
	Red y	0.338	±0.030
	Green x	0.310	±0.030
	Green y	0.554	±0.030
	Blue x	0.158	±0.030
	Blue y	0.124	±0.030
	White x	0.313	±0.030
	White y	0.329	±0.030
White Luminance (cd/m^2) ICFL 6.5 mA		200 Typ. Center 185 Typ. 5.points Average	

The following is the note for the Optical Characteristics:



- Chromaticity and White Balance are defined as the C.I.E. 1931 x,y coordinates at the center of LCD. The Measurement Equipment are as shown below table.

Item	Measuring Equipment
Viewing Angle	MCPD-7000 by Ohtsuka Elec
Contrast	MCPD-7000 by Ohtsuka Elec
Response Time	BM5A by TOPCON OPTICAL Co.,Ltd.
White Luminance	MCPD-7000 by Ohtsuka Elec
Luminance Uniformity	MCPD-7000 by Ohtsuka Elec
Chromaticity	MCPD-7000 by Ohtsuka Elec
White Balance	MCPD-7000 by Ohtsuka Elec

The measurement is to be done after 30 minutes of Power-on of BackLight.

Unless otherwise specified, the ambient conditions are as following.

Ambient Temperature	:	25 $\pm$ 2	(degreeC)
Ambient Humidity	:	25 - 85	(%)
Atmospheric Pressure	:	86.0 - 104.0	(kPa)

4.1 Luminance Uniformity

When the backlight is on with all pels in the unselected state (white), the luminance uniformity is defined as follows;

Average luminance is defined as follows.

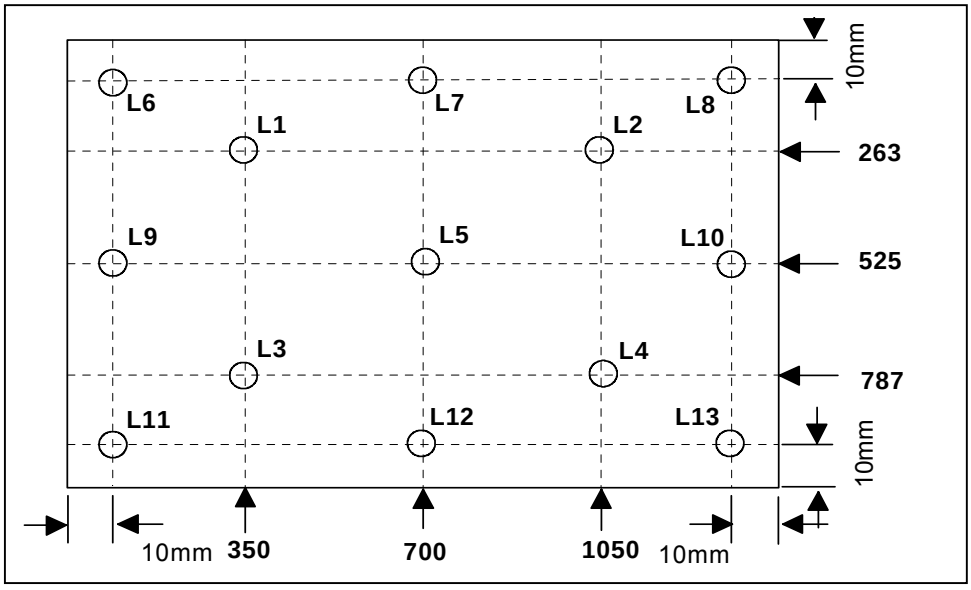
$$\text{Average Luminance} = \frac{L1 + L2 + L3 + L4 + L5}{5}$$

Luminance variation is measured by dividing the maximum luminance values of the 13 or 5 test points by the minimum luminance of the 13 or 5 test points.

$$\text{Luminance Uniformity} \quad \frac{\text{Minimum Luminance 13 Points (L1-L13)}}{\text{Maximum Luminance 13 Points (L1-L13)}} \geq 1.65$$

$$\text{Luminance Uniformity} \quad \frac{\text{Minimum Luminance 5 Points (L1-L5)}}{\text{Maximum Luminance 5 Points (L1-L5)}} \geq 1.25$$

Average luminance and Luminance uniformity test points



5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30SL-HF10
Mating Receptacle Manufacture	JAE
Mating Receptacle/Part Number	FI-X30M, FI-X30C2L

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Interface Signal Connector

Pin #	Signal Name
1	GND
2	VDD
3	VDD
4	V_{EEDID} **(Note 2,3)**
5	Reserved **(Note 1)**
6	CLK_{EEDID} **(Note 2,4)**
7	$Data_{EEDID}$ **(Note 2,4)**
8	ReIN0-
9	ReIN0+
10	GND
11	ReIN1-
12	ReIN1+
13	GND
14	ReIN2-
15	ReIN2+

Pin #	Signal Name
16	GND
17	ReCLKIN-
18	ReCLKIN+
19	GND
20	RoIN0-
21	RoIN0+
22	GND
23	RoIN1-
24	RoIN1+
25	GND
26	RoIN2-
27	RoIN2+
28	GND
29	RoCLKIN-
30	RoCLKIN+

Note:

1. 'Reserved' pins are not allowed to connect any other line.

2. This LCD Module complies with "VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3".

3. V_{EEDID} power source shall be the limited current circuit which has not exceeding 1A. (Reference Document : "Enhanced Display Data Channel (E-DDC^{TM}) Proposed Standard", VESA)

4. Both CLK_{EEDID} line and $DATA_{EEDID}$ line are pulled up with 10k ohm resistor to V_{EEDID} power source line at LCD panel, respectively.

5.3 Interface Signal Description

LCD Drive Connector Signal Description

Signal Name	Description Dual LVDS mode
ReIN0+, ReIN0-	Even LVDS differential data input (Red0-Red5, Green0)
ReIN1+, ReIN1-	Even LVDS differential data input (Green1-Green5,Blue0-Blue1)
ReIN2+, ReIN2-	Even LVDS differential data input (Blue2-Blue5, HSync, VSync, DSPTMG)
ReCLKIN+, ReCLKIN-	Even LVDS differential clock input
RoIN0+, RoIN0-	Odd LVDS differential data input (Red0-Red5, Green0)
RoIN1+, RoIN1-	Odd LVDS differential data input (Green1-Green5, Blue0-Blue1)
RoIN2+, RoIN2-	Odd LVDS differential data input (Blue2-Blue5, HSync, VSync, DSPTMG)
RoCLKIN+, RoCLKIN-	Odd LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Input signals shall be low or Hi-Z state when VDD is off

SIGNAL NAME	Description
+RED 5 (ER5/OR5) +RED 4 (ER4/OR4) +RED 3 (ER3/OR3) +RED 2 (ER2/OR2) +RED 1 (ER1/OR1) +RED 0 (ER0/OR0) (EVEN/ODD)	RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 (EG5/OG5) +GREEN 4 (EG4/OG4) +GREEN 3 (EG3/OG3) +GREEN 2 (EG2/OG2) +GREEN 1 (EG1/OG1) +GREEN 0 (EG0/OG0) (EVEN/ODD)	GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 (EB5/OB5) +BLUE 4 (EB4/OB4) +BLUE 3 (EB3/OB3) +BLUE 2 (EB2/OB2) +BLUE 1 (EB1/OB1) +BLUE 0 (EB0/OB0) (EVEN/ODD)	BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK (EVEN/ODD)	Data Clock: The typical frequency is 81MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG (DSP)	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC (V-S)	Vertical Sync: This signal is synchronized with DTCLK. Only active high signal is acceptable.
HSYNC (H-S)	Horizontal Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
VDD	Power Supply
GND	Ground
V_{EEDID}	EEDID 3.3V Power Supply
CLK_{EDID}	EEDID Clock
$Data_{EEDID}$	EEDID Data

Note: Output signals except V_{EEDID} ,CLK_{EEDID} and $Data_{EEDID}$ from any system shall be Hi-Z state when VDD is off.
VSYNC should start with active high (positive pulse) signal from when VDD is supplied and its polarity should not be changed.

5.3.1 E-EDID

E-EDID detail in this LCD module is in the following table

Address (hex)	Description	Data (hex)	Remark
00 - 07	Header	00 FF FF FF FF FF FF 00	Header, Fixed
08 - 09	ID Manufacturer Name	24 94	"IDT"
0A - 0B	ID Product Code	02 00	Product Code
0C - 0F	ID Serial Number	00 00 00 00	Unused
10	Week of Manufacture	00	Unused
11	Year of Manufacture	00	Unused
12 - 13	EDID Structure Version / Revision	01 03	Ver1.3
14 - 18	Basic Display Parameter / Features	80 1E 17 78 0A	Active Area : 30.45cm x 22.84cm,Gamma : 2.2
19 - 22	Color Characteristics	**(Note 1)**	
23 - 25	Established Timing	00 00 00	Unused
26 - 35	Standard Timing Identification	01 01 01 01 01 01 01 01 01 01 01 01 01 01 01 01	Unused
36 - 47	Detailed Timing / Monitor Description #1	30 2A 78 F0 50 1A 0F 40 30 70 13 00 31 E4 10 00 00 1E	Typical Timing
48 - 59	Detailed Timing / Monitor Description #2	**(Note 1)**	
5A - 6B	Detailed Timing / Monitor Description #3	00 00 00 FE 00 49 44 54 0A 20 20 20 20 20 20 20 20 20	Manufactuerer name "IDT"
6C - 7D	Detailed Timing / Monitor Description #4	00 00 00 FE 00 4E 31 35 30 50 32 0A 20 20 20 20 20 20	Manufacturer P/N "N150P2"
7E	Extension Flag	00	No extension
7F	Checksum	**(Note 1)**	

Note1: Detail data contents shall be determined with concurrence between user and International Display Technology (IDTech).

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

Table. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	mV	
Differential Input Low Threshold	Vtl	-100			mV	
Magnitude Differential Input Voltage	|Vid|	100		600	mV	
Common Mode Voltage	Vcm	1.125		1.5	V	
Common Mode Voltage Offset	ΔVcm	-50		+50	mV	

Note:

- Input signals shall be low or Hi-Z state when VDD is off.

Figure. Voltage Definitions

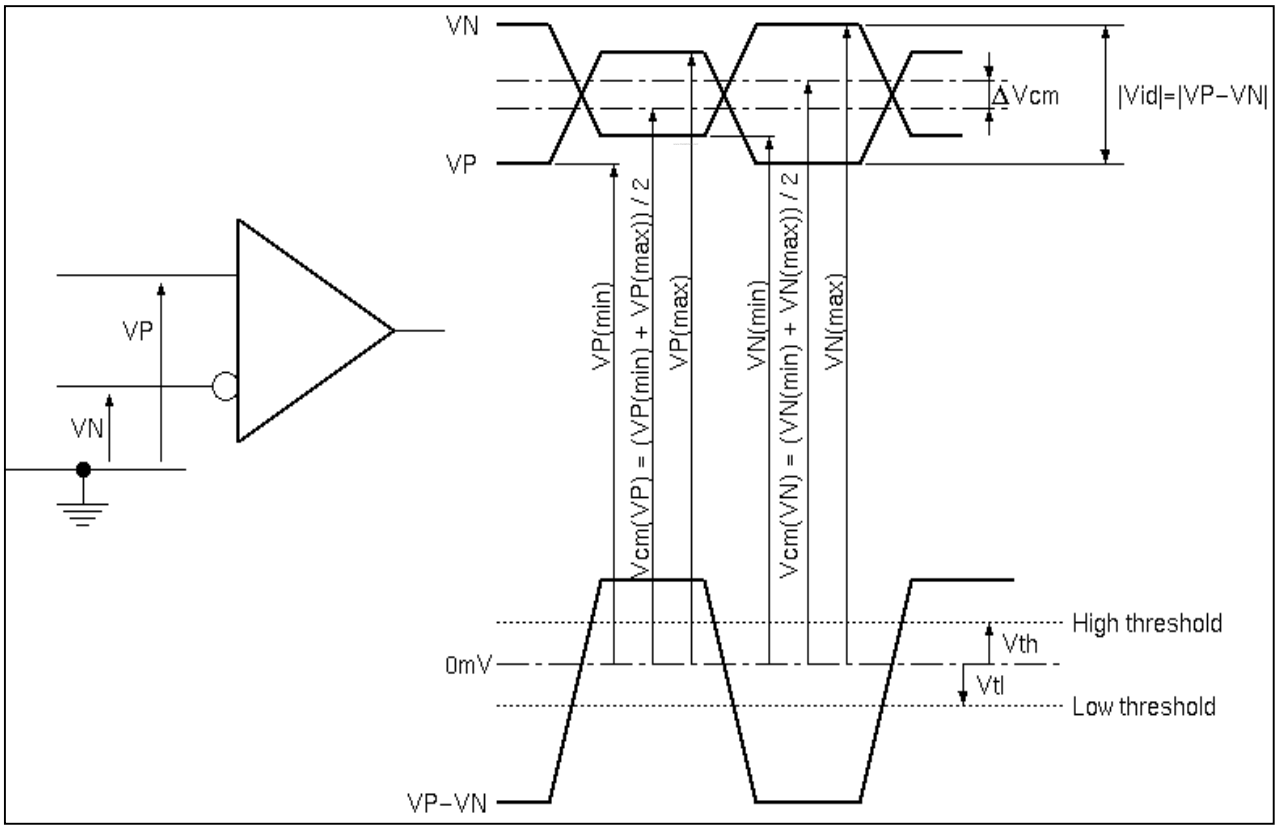


Table. Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	51	54	57	MHz	
Cycle Time	tc	17.5	18.5	19.6	ns	
Data Setup Time	Tsu	700			ps	fc = 54MHz, jitter < 50ps
Data Hold Time	Thd	700			ps	
Cycle modulation rate **(Note)**	tCJavg			20	ps/clk	

Note: This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

Figure. Timing Definition (Even)

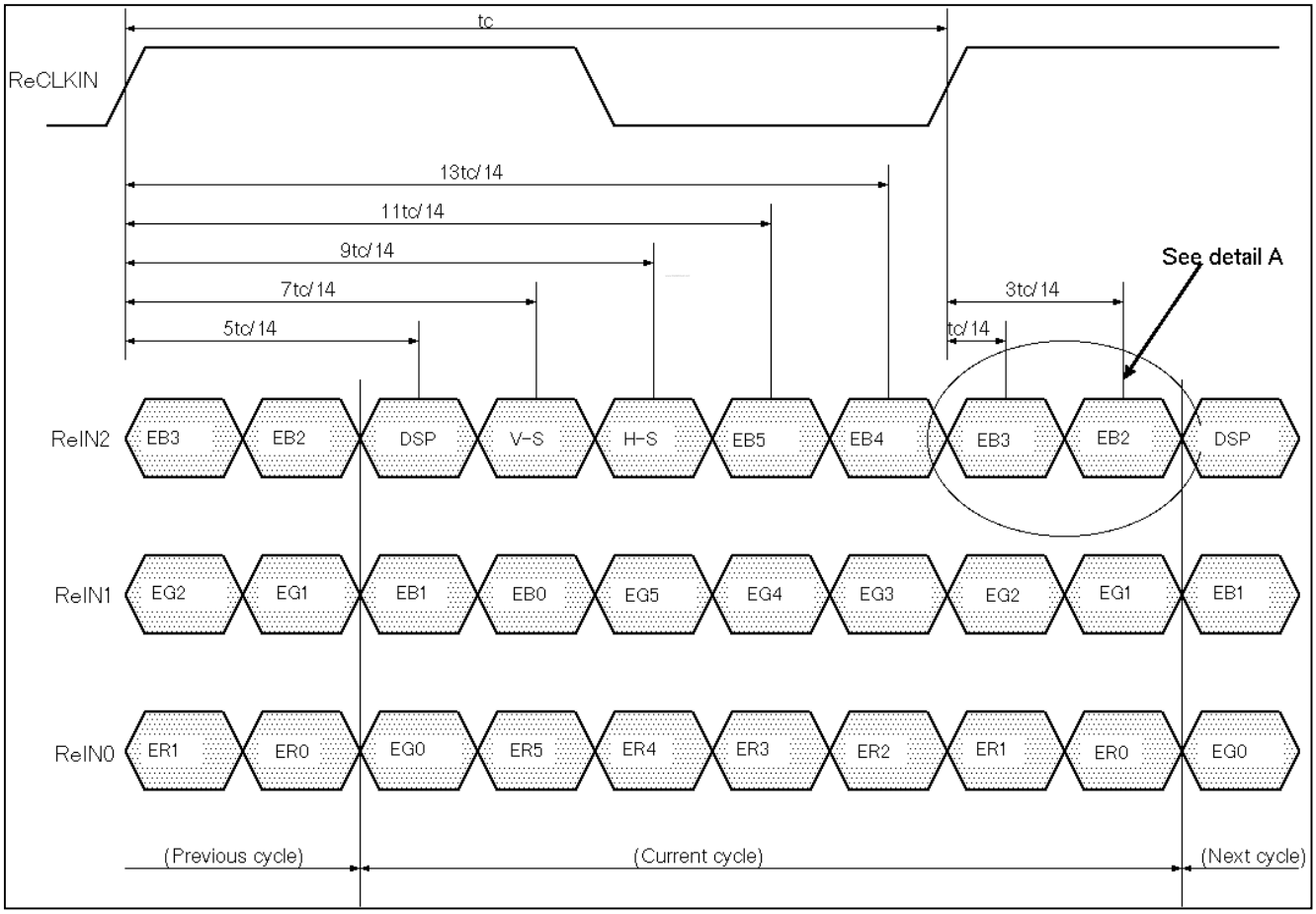


Figure. Timing Definition (Odd)

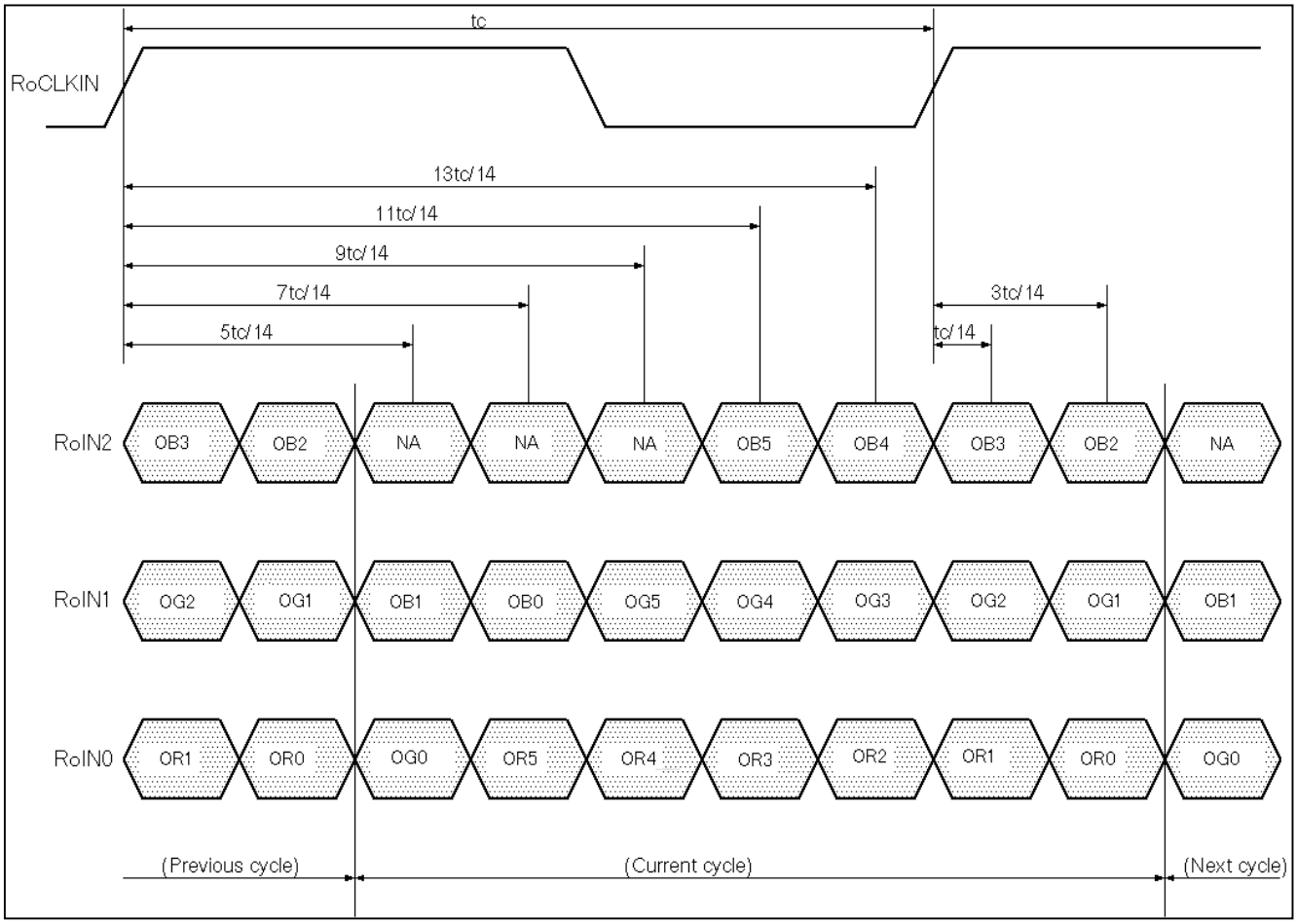
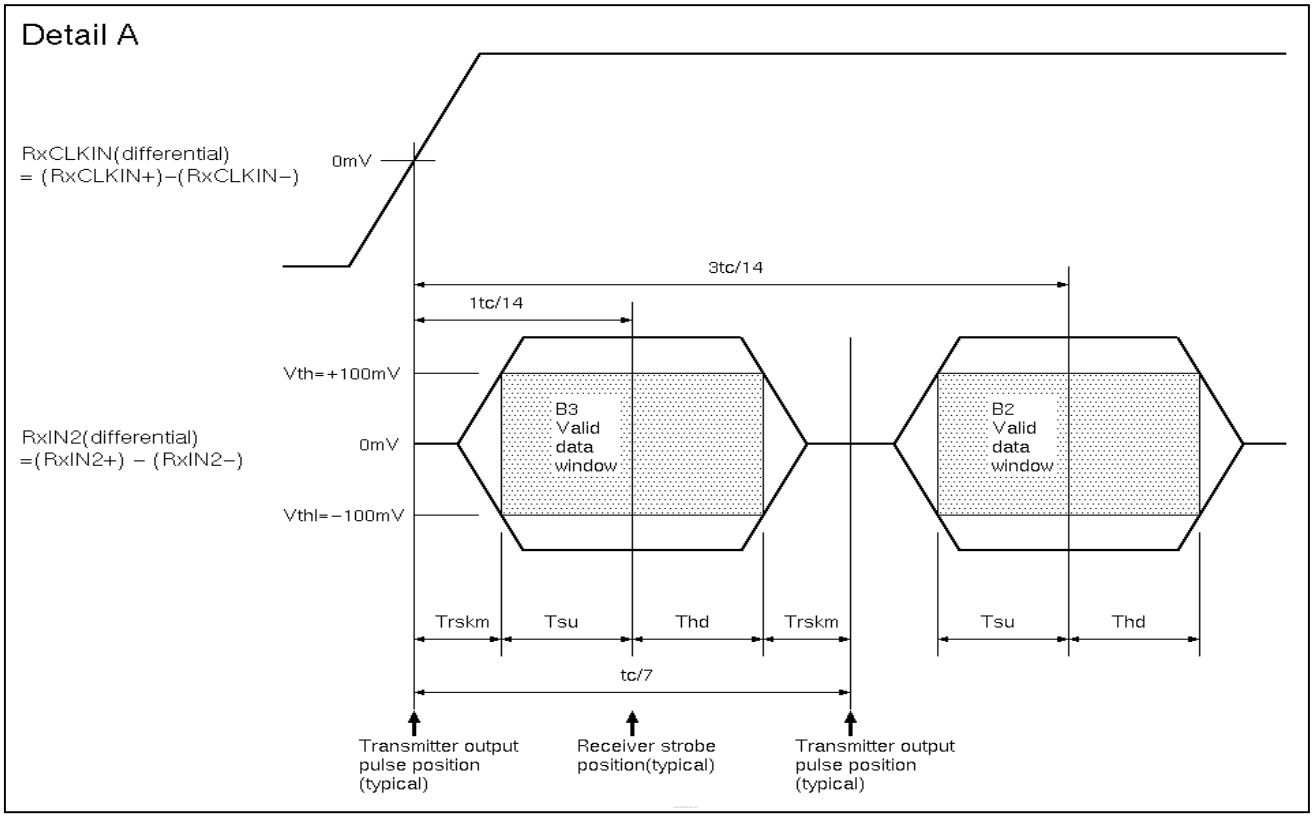
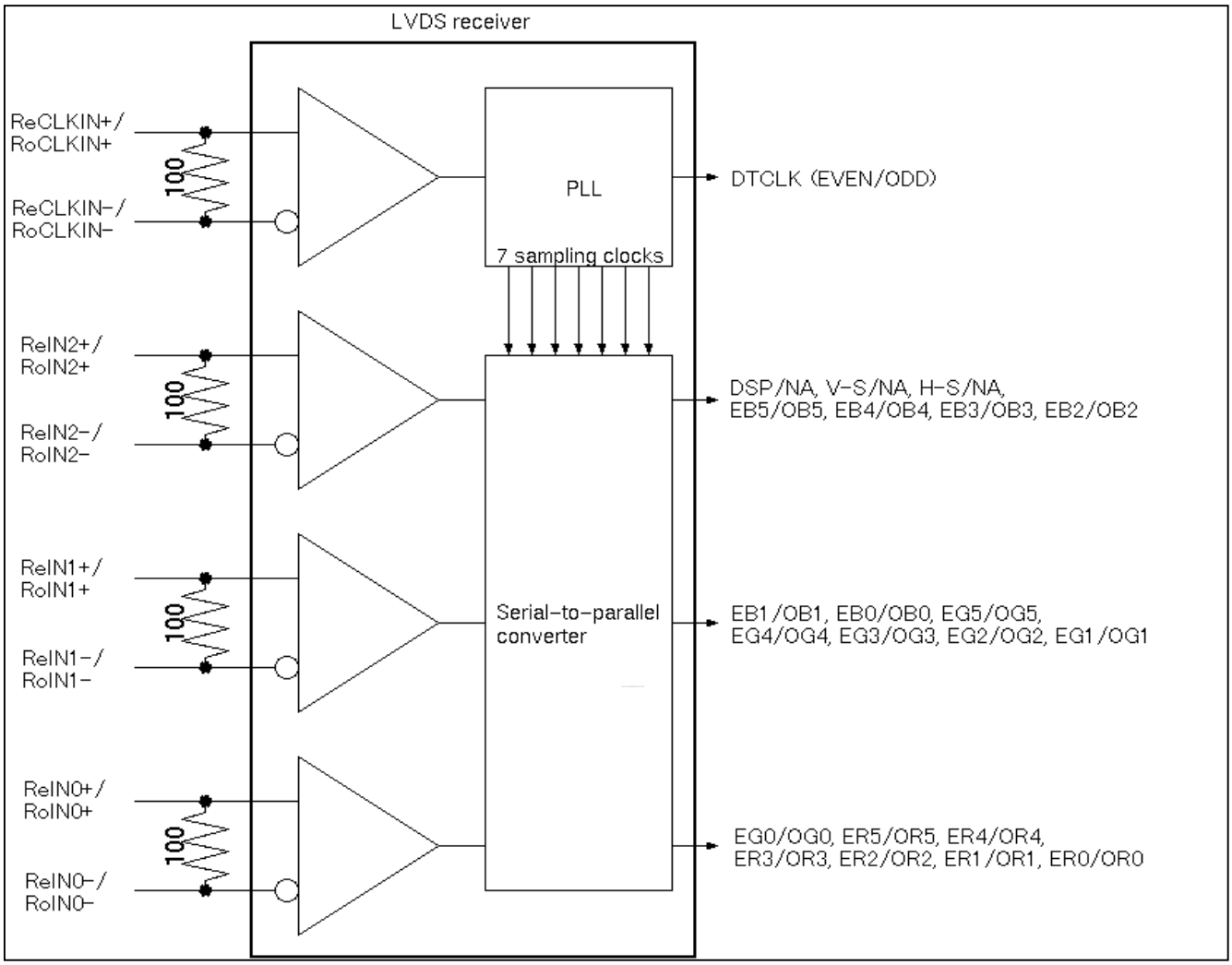


Figure. Timing Definition (detail A)



5.4.2 LVDS Receiver Internal Circuit

Below figure shows the internal block diagram of the LVDS receiver.



5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close-coupled differential traces is recommended.

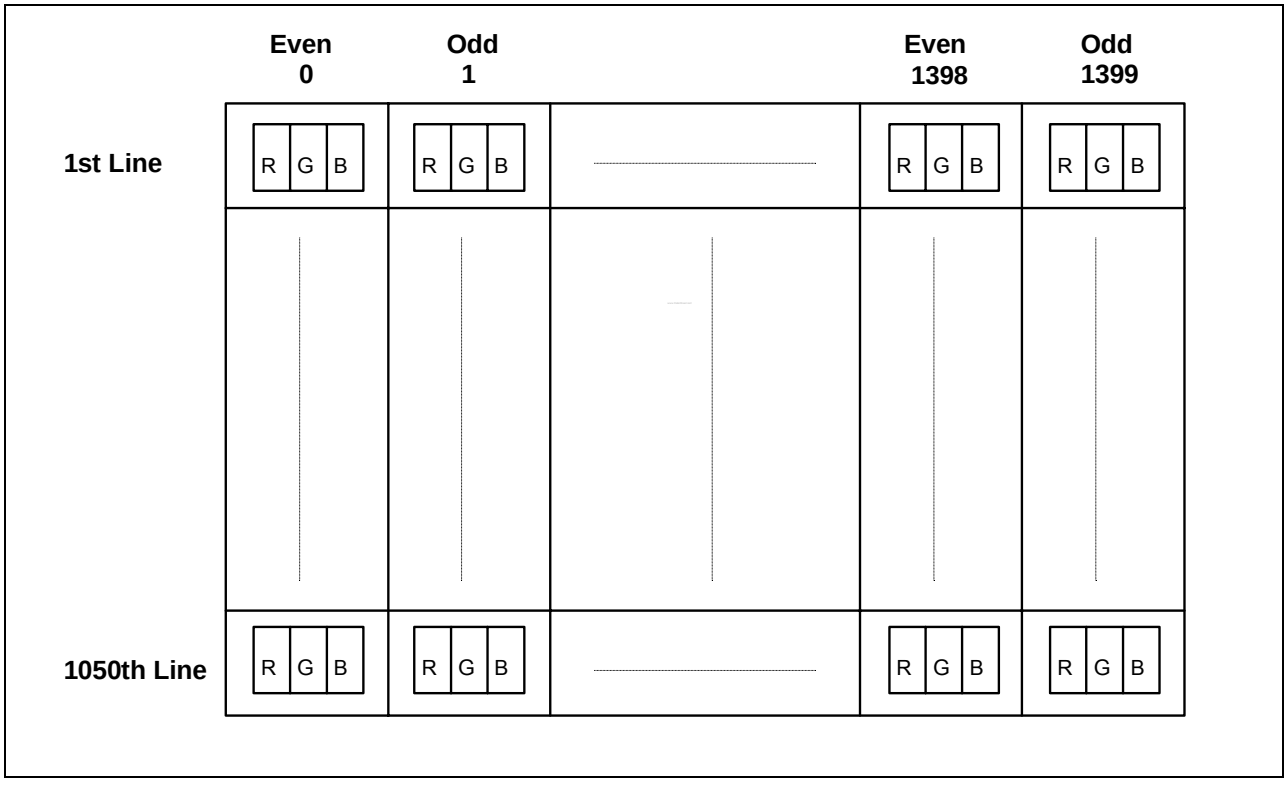
5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image.

Even and odd pair of RGB data are sampled at a time.



7.0 Parameter guide line for CFL Inverter

PARAMETER	MIN	DP	MAX	UNITS	CONDITION
White Luminance (Center) (5 Points average)	 180 165	 200 185	 - -	cd/m^2	(Ta=25 deg.C) (ICFL=6.5mArms)
CFL current (ICFL)	3.0	6.5	7.0	mArms	(Ta=25 deg.C)
CFL Frequency (FCFL)	40		60	KHz	(Ta=25 deg.C) **Note 1**
CFL Ignition Voltage (Vs)	1,500	-	-	Vrms	(Ta= 0 deg.C) **Note 3**
CFL Voltage (Reference)(VCFL)	-	630	-	Vrms	(Ta=25 deg.C) **Note 2**
CFL Power consumption (PCFL)	-	4.1	-	W	(Ta=25 deg.C) **Note 2**

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,500 voltage.Lamp units need 1,500 voltage minimum for ignition.

Note 4: DP is recommended Design Points.

*1 All of characteristics listed are measured under the condition using the Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

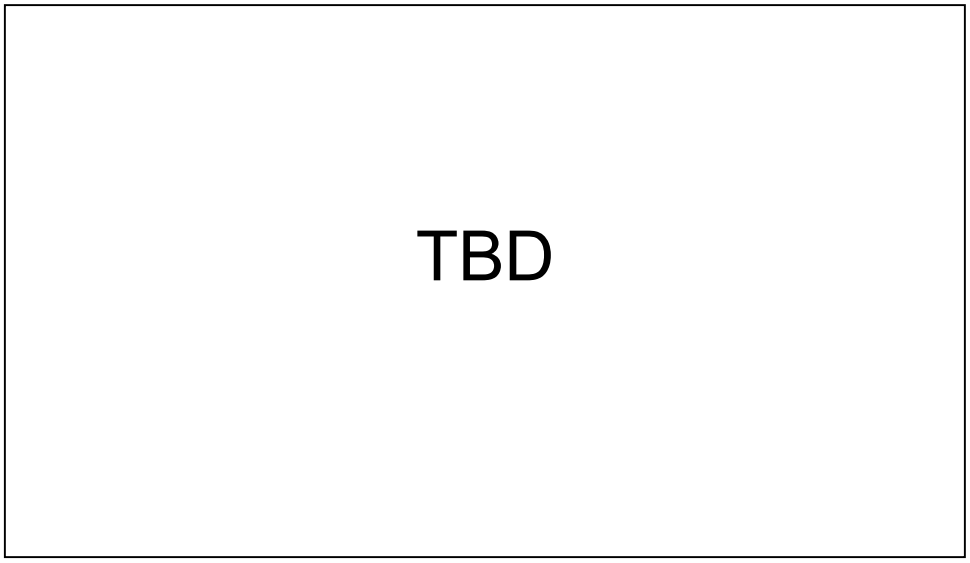
*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

*7 It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4[mA].

The following chart is Luminance versus Lamp Current for your reference.



8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86 (Texas Instruments) or equivalent.

8.1 Timing Characteristics

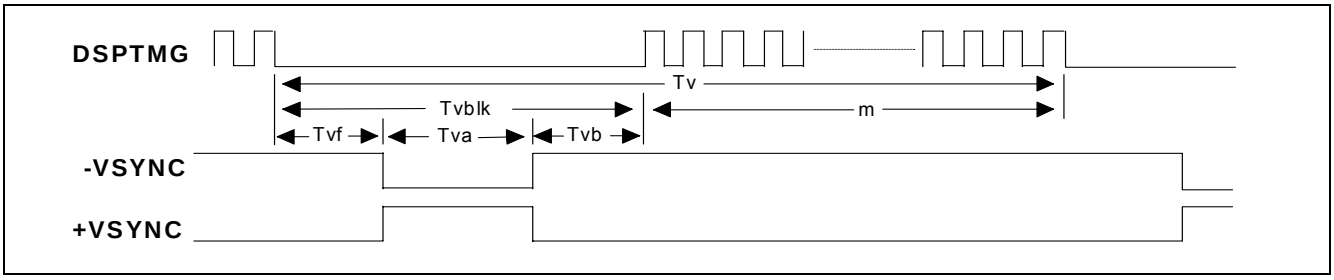
Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck	51	54	57	[MHz]
		Tck		18.5		[ns]
+V-Sync	Frame Rate	Fv		60		[Hz]
		Tv		16.67		[ms]
		Nv	1058	1066	2046	[lines]
	V-Active Level	Tva	15.78	46.7		[us]
		Nva	1	3	62	[lines]
	V-Back Porch	Nvb	6	12	125	[lines]
	V-Front Porch	Nvf	1	1		[lines]
+DSPTMG	V-Line	m		1050		[lines]
+H-Sync	Scan Rate	Fh		63.98		[KHz]
		Th		15.63		[usec]
		Nh	762	844	1023	[Tck]
	H-Active Level	Tha		1.037		[usec]
		Tha	8	56	250	[Tck]
	H-Back Porch	Thb	26	64	300	[Tck]
	H-Front Porch	Thf	8	24		[Tck]
+DSPTMG	Display	Thd		12.96		[usec]
+DATA	Data Even/Odd	n		1400		[dots]

Note: Both positive Hsync and positive Vsync polarity is recommended

8.2 Timing Definition

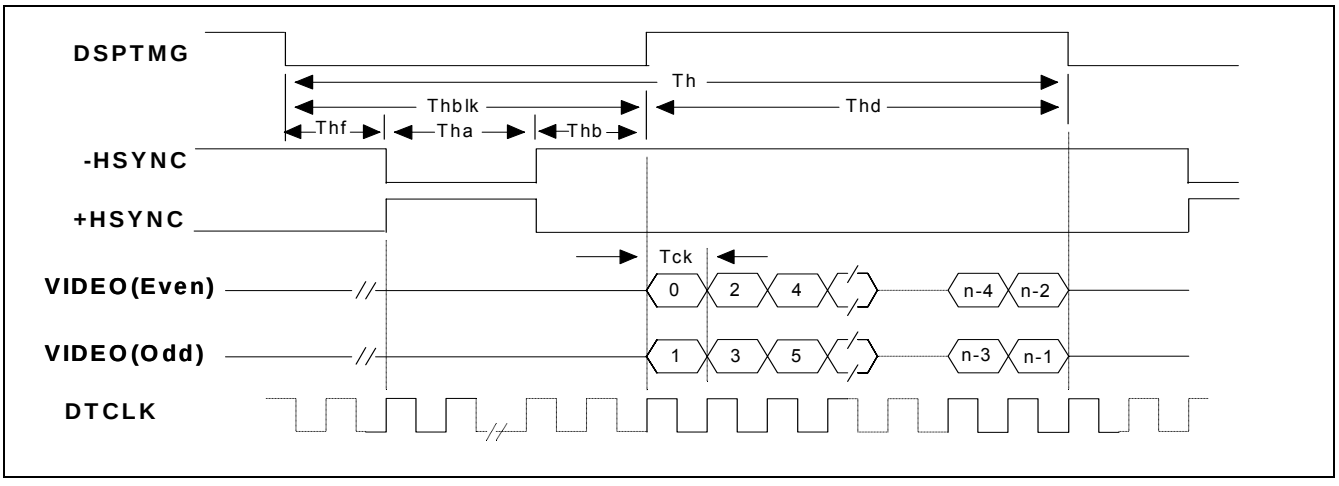
Vertical Timing

Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1400 x 1050 at 60Hz (H line rate : 15.63 us)	0.250 ms (16 lines)	16.411 ms (1050 lines)	0.016 ms (1 line)	16.661 ms (1066 lines)	0.047 ms (3 lines)	0.188 ms (12 lines)



Horizontal Timing

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1400 x 1050 Dotclock : 108.000 MHz (54.000MHz x2)	2.667 us (288 dots)	12.963 us (1400 dots)	0.444 us (48 dots)	15.630 us (1688 dots)	1.037 us (112 dots)	1.185 us (128 dots)



9.0 Power Consumption

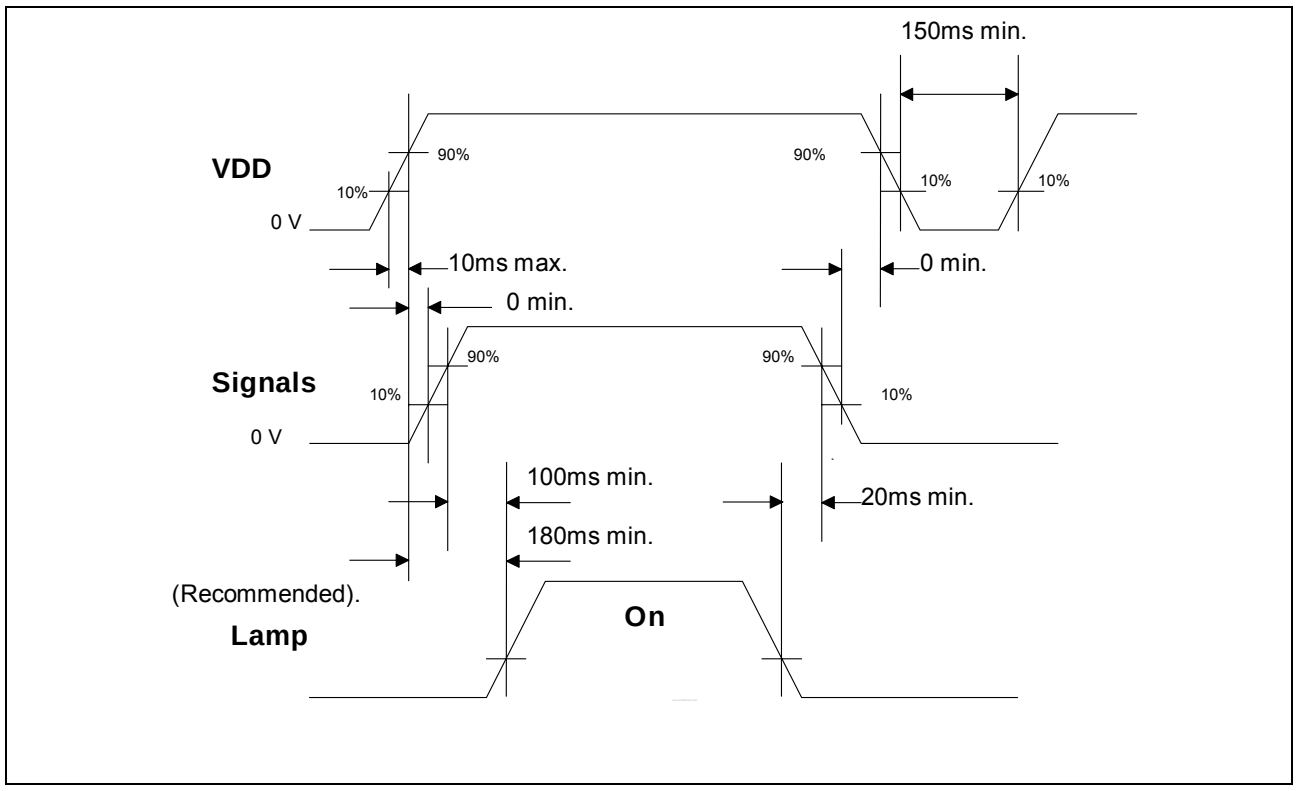
Input power specifications are as follows;

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3	3.3	3.6	V	Load Capacitance 40uF
PDD	VDD Power Max			2.6	W	MAX Pattern **VDD=3.6V**
PDD	VDD Power		1.4		W	All Black Pattern **VDD=3.3V**
IDD Max	IDD Current Max			720	mA	MAX Pattern **VDD=3.6V**
IDD	IDD Current		420		mA	All Black Pattern **VDD=3.3V**
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

Note: Max Pattern:2 dot Vertical sub-pixel stripe.

10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics

Refer to the attached drawing.

12.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

Conditions of Acceptability - When installed in the end-product, consideration shall be given to the following;

1. This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, CSA/ UL60950, Third Edition, dated December 1, 2000, Sub-clause 2.10, which would cover the component itself if submitted for Listing.
2. The unit is intended to be supplied by SELV and Limited Power Source. Also separated from electrical parts, which may produce high temperature that could cause ignition by as least 13 mm of air or by a solid barrier of material of V-1 minimum.
3. The terminals and connectors are suitable for factory wiring only.
4. A suitable electrical enclosure shall be provided.

13.0 Qualifications and CFL Life

This Quality Specification is for the SXGA+ TFT-LCD module N150P2-L06supplied from International Display Technology to the customer.

Please pay attention the following items, when this LCD Module is checked in your inspection.

1. You should consider the LCD Module to mount that uneven force is not applied to this LCD Module.

2. Do not push and put a label on the rear side that is located backlight.

3. Do not joggle the LCD Module, there will be some ripple on the screen.

4. Display qualifications depend on the power on time.
   The visual screen quality is applied the state since 30 seconds after power on

13.1 Visual Screen Quality

The following Table describes the visual screen quality of the general TFT-LCD module.

Polarizer Scratch/Bubble	Size (mm)			Allowable maximum counts
Elliptical defects	d < 0.15			Disregarded
	0.15 ≦ d < 0.3			4
	0.3 ≦ d			0
Linear defects	w < 0.05			Disregarded
	0.05 ≦ w ≦ 0.07	and	l ≦ 2.0	4
	0.07 < w	or	2.0 < l	0

d : diameter

$$d = \frac{\text{longaxis} + \text{shortaxis}}{2}$$

w : line width

l : line length

13.2 Line Defect

No visible line defect is allowed in entire screen.
A Line Defect is defined as a horizontal and vertical apparent line, visible through 5% ND-filter, that differs from adjacent lines at any gray raster pattern.

13.3 Bright and Black Dots

The following Table describes the specification of bright and black dots in the visual screen quality of the TFT-LCD module at power-ON.

Items	Specification
Any Bright Dots	6 Max
Bright and Black Dots (total)	15 Max
Definitions: 1. A Bright Dot is any one of stuck Red, Green or Blue pixel visible through 5% ND-filter under all black background. 2. A Black Dot is an unlit sub pixel under any of White, Red, Green or Blue bright raster.	
Basic Conditions: Viewing Distance 350 to 500 mm Ambient Illumination 300 to 700 lux Ambient Temperature 20 to 25 degreeC	

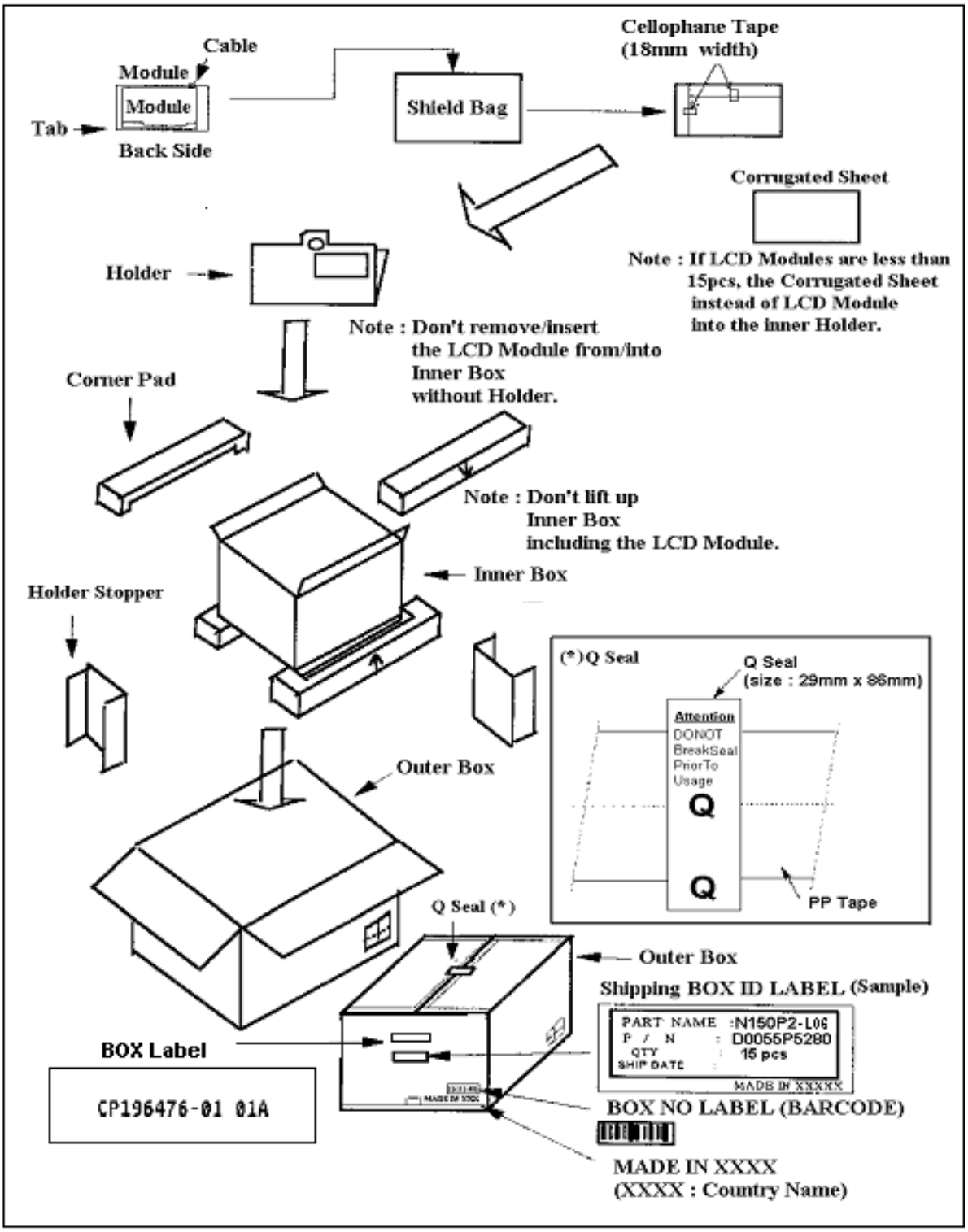
13.4 CFL Life

CFL Life Time	10,000 Hours	condition 25 degree C and 6.5 mArms

The assumed CFL Life will be until the luminance becomes 50% of it's initial value of the panel.

14.0 Packaging Specification

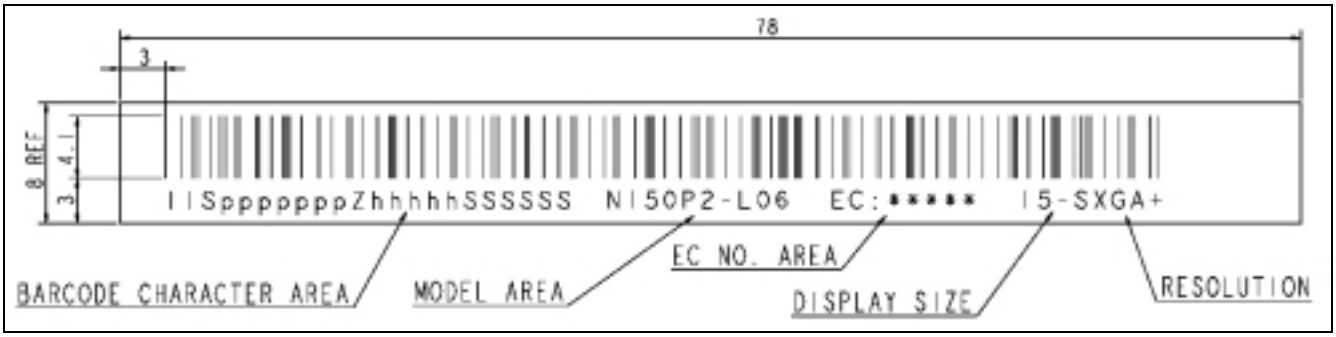
The packaging of the LCD meets 75 cm drop test. The following is the drawing of the package.



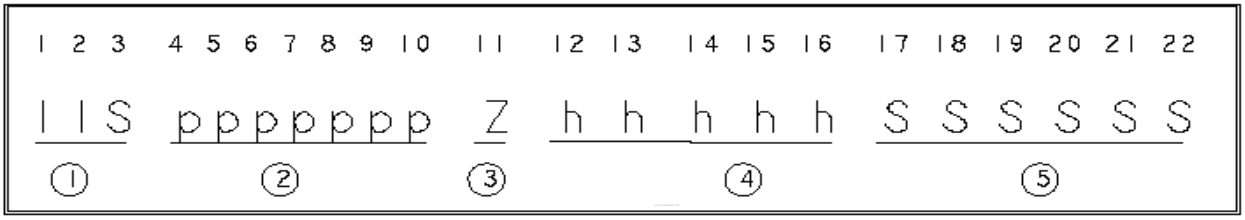
15.0 Label

There are labels on the rear side of the Module.

Serial Number Label



BARCODE CHARACTER AREA



① IIS = FIXED
STARTING IDENTIFIER WHICH IS COMMON TO COMPONENT LEVEL SERIAL NUMBERS

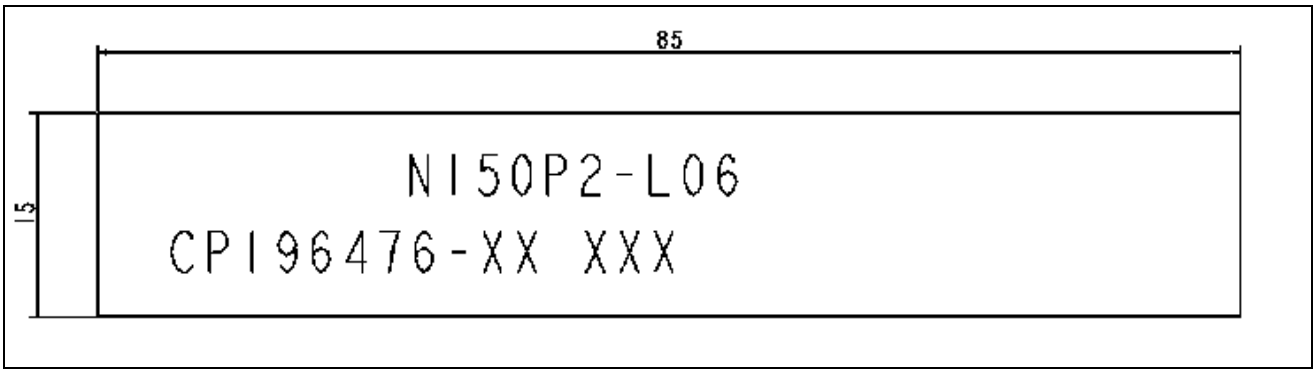
② SEVEN DIGIT IDT PART NUMBER ASSIGNED BY THE IDT DEVELOPMENT RELEASING THE PART

③ Z = FIXED
AUTOMATICALLY GIVEN WHEN USING THE IIS-Z FORMAT

④ hhhhh=HEADER CODE(EC LEVEL)

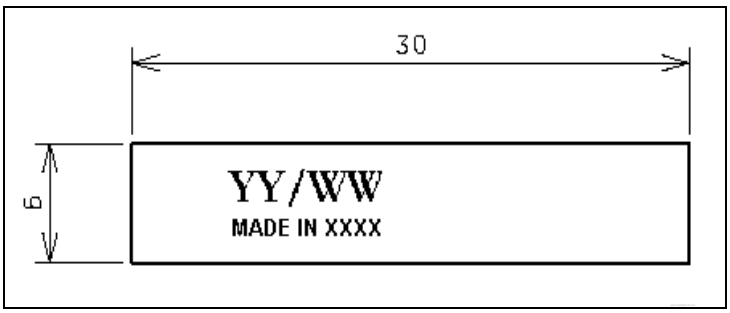
⑤ SSSSS=SEQUENCE

ID Label

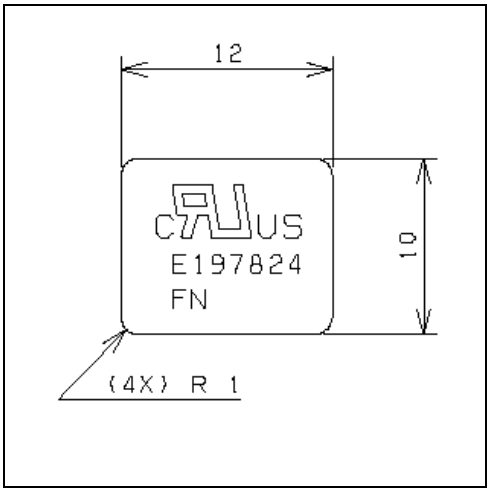


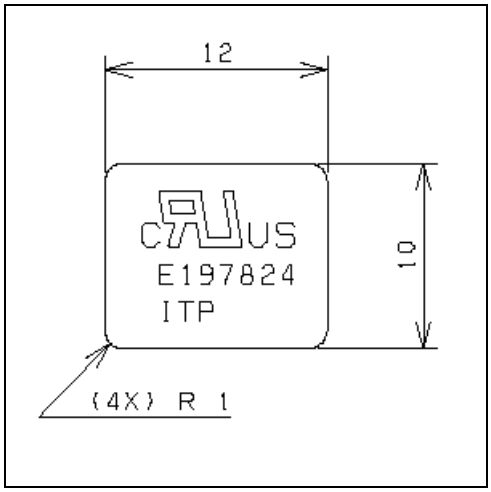
Date Label

YY and WW of the Week Code stand for the Year and the Week of the Year of manufacturing of the Module respectively.



UL Label





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