Engineering Specification

Type 15.0 UXGA Color TFT/LCD Module
Model Name: N150U3-L06

Document Control Number: OEM I-N150U3-L06

Note: Specification is subject to change without notice. Consequently it is better to contact International Display Technology before proceeding with the design of your product incorporating this module.

Sales Support
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
February 18, 2004	OEM I-N150U3-L06	All	First Edition for customer.

1.0 Handling Precautions

- Since front polarizer is easily damaged, pay attention not to scratch it.
- Be sure to turn off power supply when inserting or disconnecting from input connector.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- Do not open nor modify the Module Assembly.
- Do not press the reflector sheet at the back of the module to any directions.
- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 3rd.Ed. or UL60950 3rd. Ed.), or be applied exemption conditions of flammability requirements (4.7.3.4, IEC60950 3rd.Ed. or UL60950 3rd.Ed.) in an end product.
- The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 3rd.Ed. or UL60950 3rd.Ed.). Do not connect the CFL in Hazardous Voltage Circuit.

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▪ The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the Type 15.0 Color TFT/LCD Module 'N150U3-L06'.
This module is designed for a display unit of notebook style personal computer.
The screen format and electrical interface are intended to support the UXGA (1600(H) x 1200(V)) screen.
Support color is native 262K colors (RGB 6-bit data driver).
All input signals are LVDS (Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

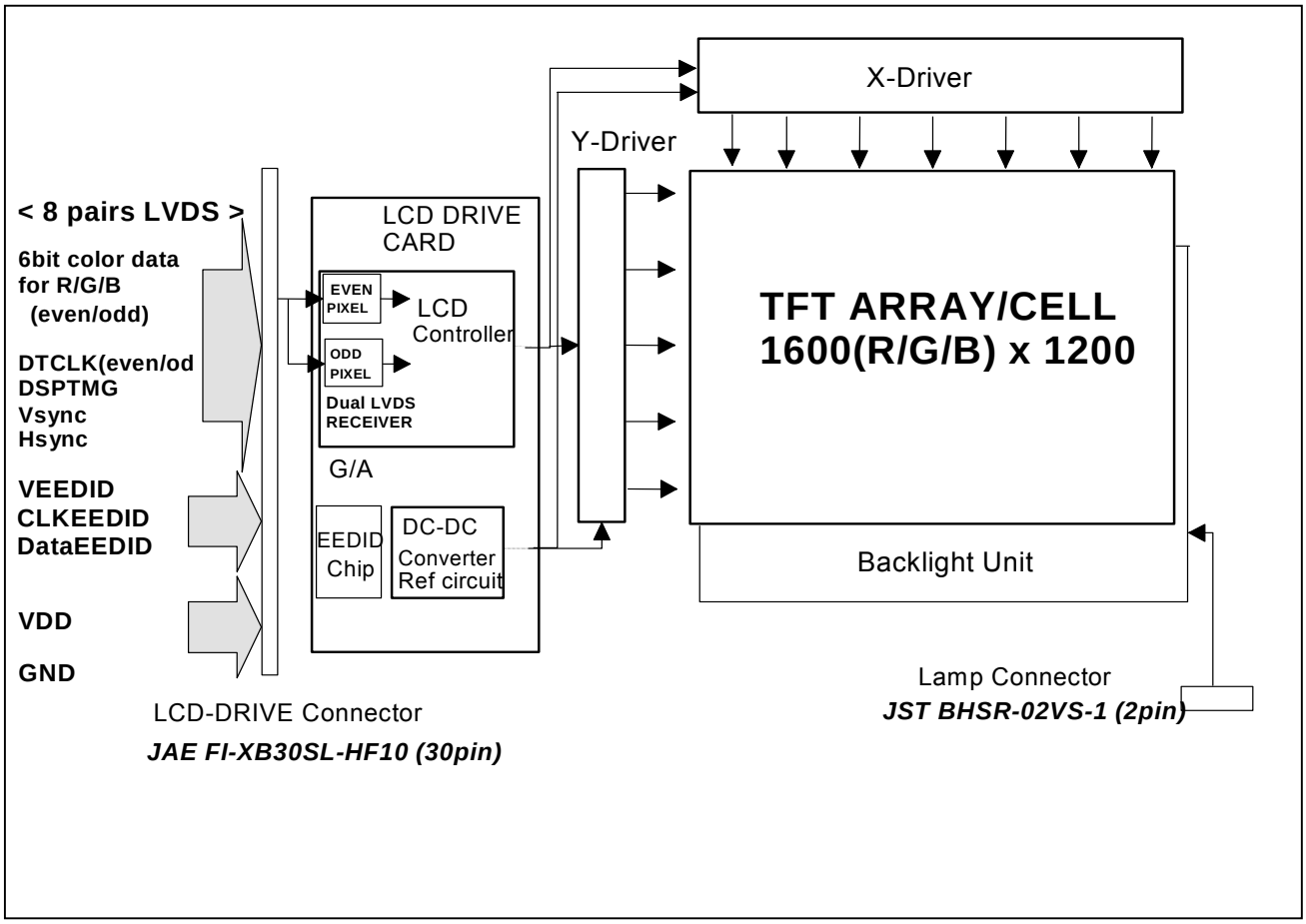
2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	381
Pixels H x V	1600(x3) x 1200
Active Area [mm]	304.8(H) x 228.6(V)
Pixel Pitch [mm]	0.1905(per one triad) x 0.1905
Pixel Arrangement	R,G,B Vertical Stripe
Weight [grams]	575 Typ 600 Max.
Physical Size [mm]	317.3(W) x 242.0(H) x 6.2(D) Typ./6.5(D) Max.
Display Mode	Normally Black
Display Surface Treatment	Anti-Glare Treatment
Support Color	Native 262K colors (RGB 6-bit data driver)
White Luminance [cd/m^2] (center)	200 Typ.
Contrast Ratio	400 : 1 Typ.
Optical Rise Time + Fall Time [msec]	60 Typ., 120 Max
Nominal Input Voltage VDD [Volt]	+3.3 Typ.
Power Consumption [Watt](VDD)	3.1 Typ., 4.4 Max.
Lamp Power Consumption [Watt]	4.1 Typ., (W/o inverter loss) 4.5 Max., (W/o inverter loss)
Typical Power Consumption [Watt]	7.2 Typ., 8.9 Max.(W/o inverter loss)
Electrical Interface	8 pairs LVDS (Even/Odd R/G/B Data(6bit), 3sync signals, Clock)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 -20 to +60
CFL Cable Length [mm]	85 Typ
Module Life	10,000 hours (same as lamp life)

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 15.0 Color TFT/LCD Module.
The first LVDS port transmits even pixels while the second LVDS port transmits odd pixels.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	V	
Input Signal Voltage	VIN	-0.3	VDD+0.3	V	
CFL Ignition Voltage	Vs	-	+2,000	Vrms	**Note 2**
CFL Current	ICFL	-	7	mAms	
CFL Peak Inrush Current	ICFLP	-	20	mA	
Operating Temperature	TOP	0	+50	deg.C	**Note 1**
Operating Relative Humidity	HOP	8	95	%RH	**Note 1**
Storage Temperature	TST	-20	+60	deg.C	**Note 1**
Storage Relative Humidity	HST	5	95	%RH	**Note 1**
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note 1: Maximum Wet-Bulb should be 39 degree C and No condensation.

Note 2: Duration: 50msec Max. Ta=0 degree C

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K: Contrast Ratio	Horizontal (Right) K≧10 (Left) Vertical (Upper) K≧10 (Lower)	85 85 85 85	- - - -
Contrast ratio		400	-
Response Time (ms)	Rising + Falling	60	-
Color Chromaticity (CIE)	Red x	0.569	-
	Red y	0.332	-
	Green x	0.312	-
	Green y	0.544	-
	Blue x	0.149	-
	Blue y	0.132	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m^2)	Icfl=6.5mA	200 Typ. (Center) 185 Typ. (5point average)	-

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30SL-HF10
Mating Receptacle Manufacture	JAE
Mating Receptacle/Part Number	FI-X30M

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Interface Signal Connector

Pin #	Signal Name
1	GND
2	VDD
3	VDD
4	V_{EEDID} **(Note 2,3)**
5	Reserved **(Note 1)**
6	CLK_{EEDID} **(Note 2,4)**
7	$Data_{EEDID}$ **(Note 2,4)**
8	ReIN0-
9	ReIN0+
10	GND
11	ReIN1-
12	ReIN1+
13	GND
14	ReIN2-
15	ReIN2+

Pin #	Signal Name
16	GND
17	ReCLKIN-
18	ReCLKIN+
19	GND
20	RoIN0-
21	RoIN0+
22	GND
23	RoIN1-
24	RoIN1+
25	GND
26	RoIN2-
27	RoIN2+
28	GND
29	RoCLKIN-
30	RoCLKIN+

Note:

1. 'Reserved' pins are not allowed to connect any other line.
2. This LCD Module complies with "VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3". This module uses Serial EEPROM AT24C02-10TI-2.7 (ATMEL) or compatible as a EEDID function.
3. V_{EEDID} power source shall be the current limited circuit which has not exceeding 1A. (Reference Document: "Enhanced Display Data Channel (E-DDC^{TM}) Proposed Standard", VESA)
4. Both CLK_{EEDID} line and $Data_{EEDID}$ line are pulled-up with 10K ohm resistor to V_{EEDID} power source line at LCD panel, respectively.

Voltage levels of all input signals are LVDS compatible (except VDD,EEDID). Refer to "Signal Electrical Characteristics for LVDS(*)", for voltage levels of all input signals.

5.3 Interface Signal Description

The LVDS receiver equipped in this LCD module is compatible with ANSI/TIA/TIA-644 standard.

PIN #	SIGNAL NAME	Description
2	GND	Ground
3	VDD	+3.3V Power Supply
4	VDD	+3.3V Power Supply
5	V_{EEDID}	EEDID 3.3V Power Supply
6	Reserved	Reserved
7	CLK_{EEDID}	EEDID Clock
8	$Data_{EEDID}$	EEDID Data
9	ReIN0-	Negative LVDS differential data input (ER0-ER5, EG0)
10	ReIN0+	Positive LVDS differential data input (ER0-ER5, EG0)
11	GND	Ground
12	ReIN1-	Negative LVDS differential data input (EG1-EG5, EB0-EB1)
13	ReIN1+	Positive LVDS differential data input (EG1-EG5, EB0-EB1)
14	GND	Ground
15	ReIN2-	Negative LVDS differential data input (EB2-EB5, HSYNC, VSYNC, DSPTMG)
16	ReIN2+	Positive LVDS differential data input (EB2-EB5, HSYNC, VSYNC, DSPTMG)
17	GND	Ground
18	ReCLKIN-	Negative LVDS differential clock input (ECLK)
19	ReCLKIN+	Positive LVDS differential clock input (ECLK)
20	GND	Ground
21	RoIN0-	Negative LVDS differential data input (OR0-OR5, OG0)
22	RoIN0+	Positive LVDS differential data input (OR0-OR5, OG0)
23	GND	Ground
24	RoIN1-	Negative LVDS differential data input (OG1-OG5, OB0-OB1)
25	RoIN1+	Positive LVDS differential data input (OG1-OG5, OB0-OB1)
26	GND	Ground
27	RoIN2-	Negative LVDS differential data input (OB2-OB5)
28	RoIN2+	Positive LVDS differential data input (OB2-OB5)
29	GND	Ground
30	RoCLKIN-	Negative LVDS differential clock input (OCLK)
31	RoCLKIN+	Positive LVDS differential clock input (OCLK)

Note:

Input signals of odd and even clock shall be the same timing.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input.

Even : First Pixel data

Odd : Second Pixel Data

SIGNAL NAME	Description
ER5/OR5	(Even / Odd) RED Data 5
ER4/OR4	(Even / Odd) RED Data 4
ER3/OR3	(Even / Odd) RED Data 3
ER2/OR2	(Even / Odd) RED Data 2
ER1/OR1	(Even / Odd) RED Data 1
ER0/OR0	(Even / Odd) RED Data 0
	Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data.
EG5/OG5	(Even / Odd) GREEN Data 5
EG4/OG4	(Even / Odd) GREEN Data 4
EG3/OG3	(Even / Odd) GREEN Data 3
EG2/OG2	(Even / Odd) GREEN Data 2
EG1/OG1	(Even / Odd) GREEN Data 1
EG0/OG0	(Even / Odd) GREEN Data 0
	Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data.
EB5/OB5	(Even / Odd) BLUE Data 5
EB4/OB4	(Even / Odd) BLUE Data 4
EB3/OB3	(Even / Odd) BLUE Data 3
EB2/OB2	(Even / Odd) BLUE Data 2
EB1/OB1	(Even / Odd) BLUE Data 1
EB0/OB0	(Even / Odd) BLUE Data 0
	Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data.
ECLK / OCLK	Data Clock (DTCLK): The typical frequency is 81MHz. The signal is used to strobe the pixel +data and the +DSPTMG
DSPTMG	Display Timing: When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync: Both active high/low signals are acceptable.
HSYNC	Horizontal Sync: Both active high/low signals are acceptable.
VDD	Power Supply
GND	Ground
V_{EEDID}	EEDID Power Supply
CLK_{EEDID}	EEDID Clock
$Data_{EEDID}$	EEDID Data

Note: Output signals except V_{EEDID}, CLK_{EEDID} and $Data_{EEDID}$ from any system shall be Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

Table. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100			mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100		600	mV	
Common Mode Voltage	Vcm	1.0	1.2	1.4	V	Vth - Vtl = 200mV
Common Mode Voltage Offset	ΔVcm	-50		+50	mV	Vth - Vtl = 200mV

Note:

- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD (see Figure **Measurement system**).

Figure . Voltage Definitions

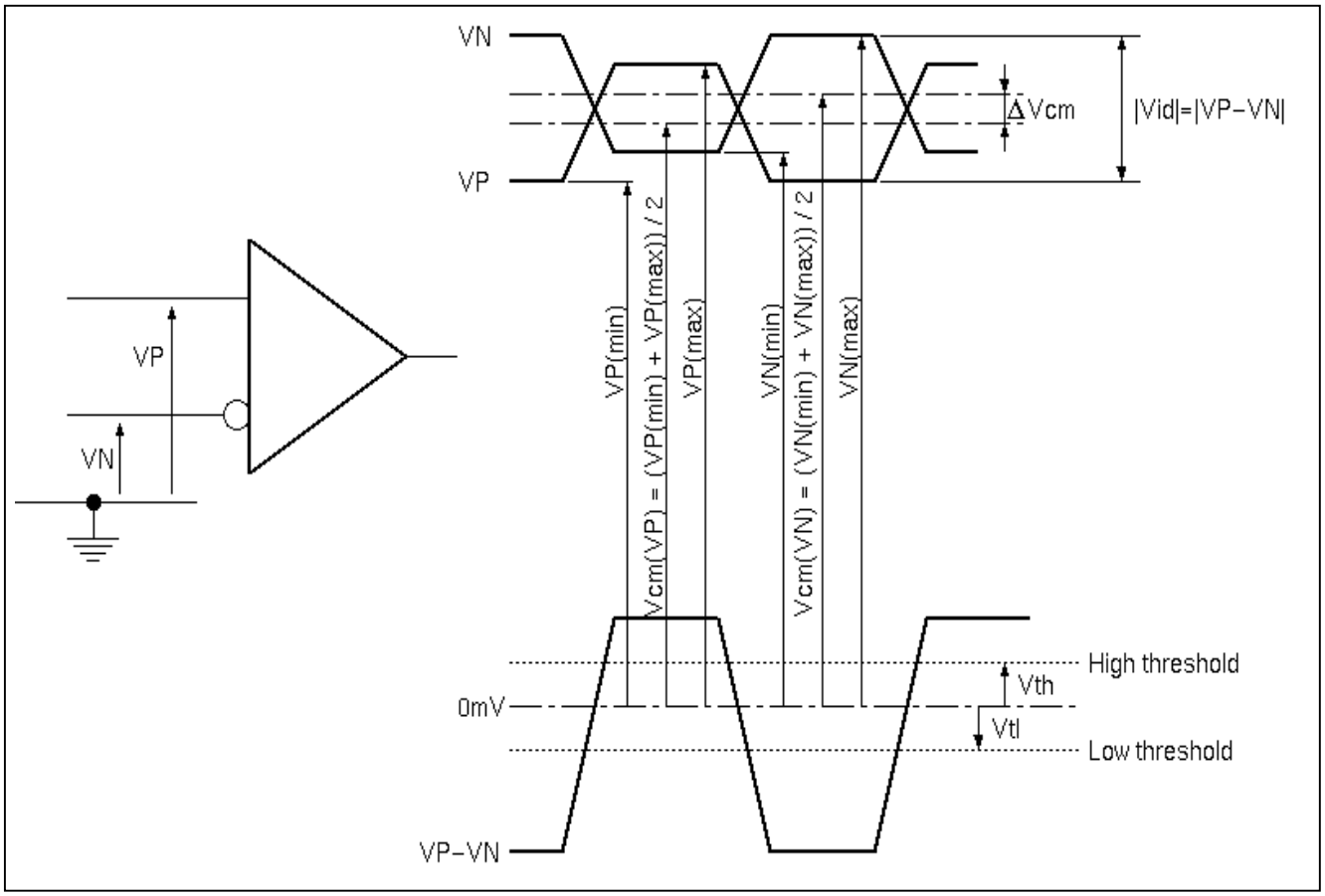


Figure. Measurement system

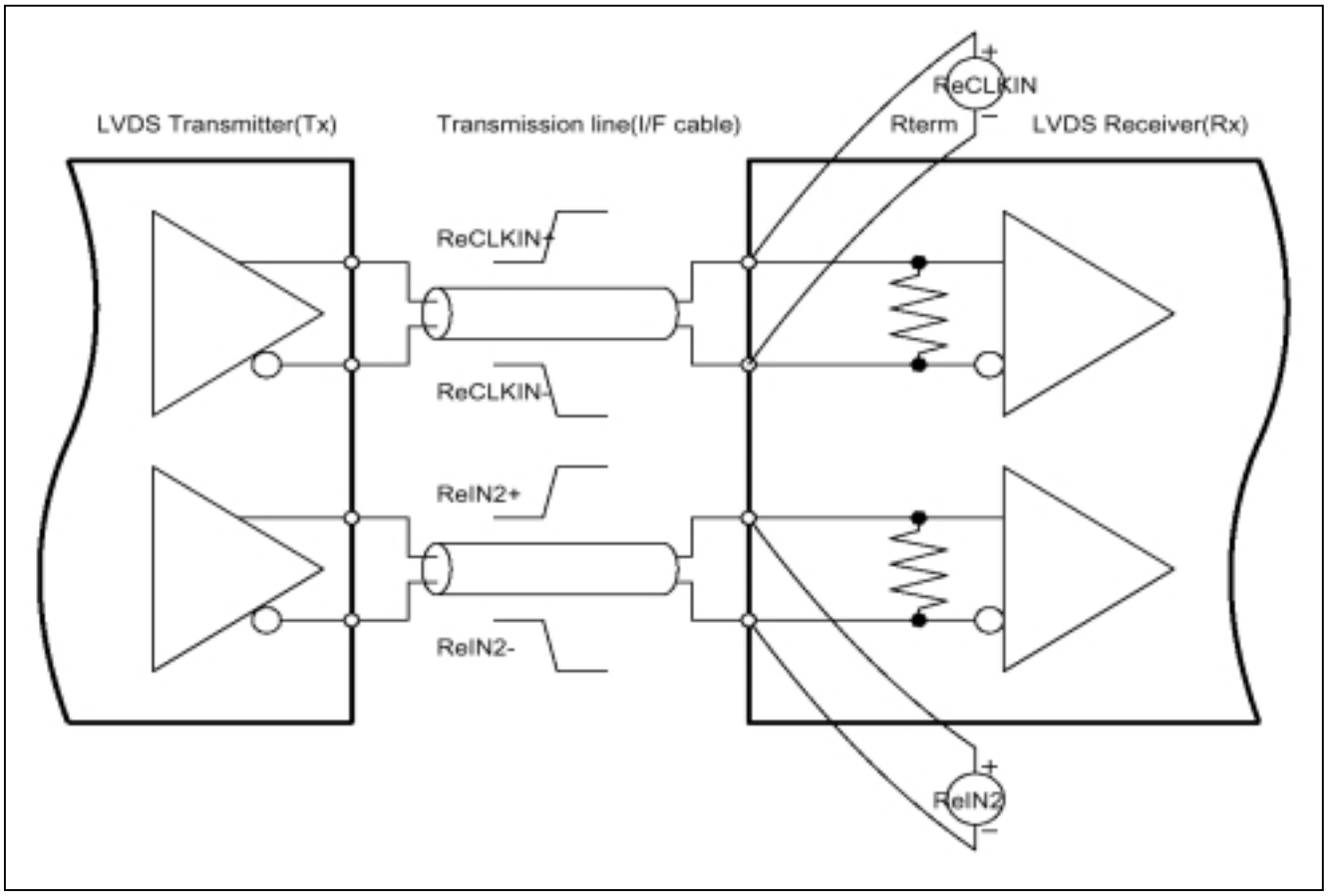


Table. Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	53.0	81.0	83.0	MHz	
Cycle Time	tc	12.0	12.3	18.8	ns	
Data Setup Time **(Note 1)**	Tsu	500			ps	fc = 81MHz, tCCJ < 50ps, Vth-Vtl = 200mV, Vcm = 1.2V, ΔVcm = 0
Data Hold Time **(Note 2)**	Thd	500			ps	
Cycle-to-cycle jitter **(Note 3)**	tCCJ	-150		+150	ps	fc = 81MHz
Cycle Modulation Rate **(Note 4)**	tCJavg			20	ps/clk	fc = 81MHz
Clock Skew between LVDS ODD/EVEN channels				1	ns	

Note 1: All values are at VDD=3.3V, Ta=25 degree C.

Note 2: See figure **"Timing Definition**" and **"Timing Definition (detail A)**" for definition.

Note 3: Jitter is the magnitude of the change in input clock period.

Note 4: This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

Figure. Timing Definition (Even)

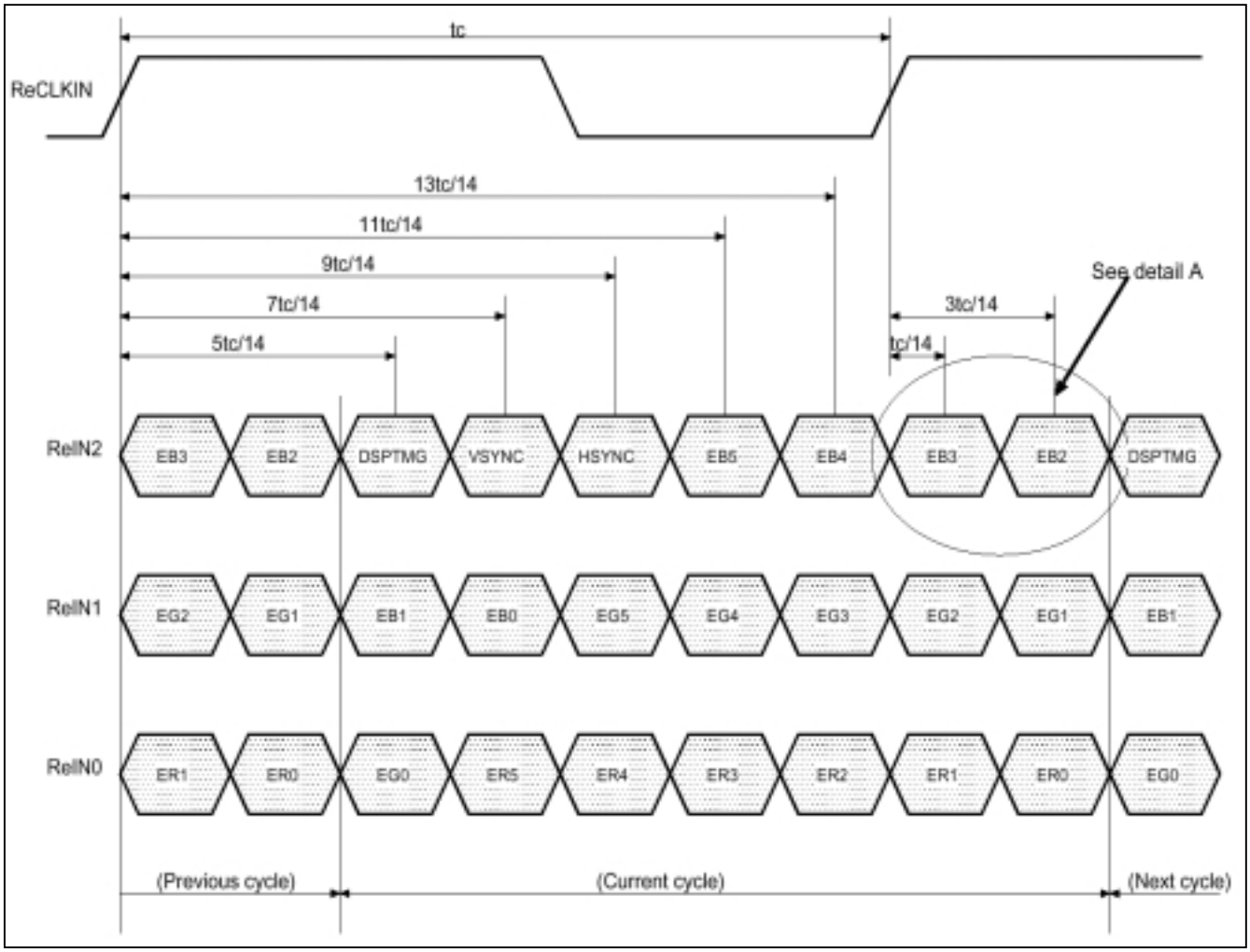


Figure. Timing Definition (Odd)

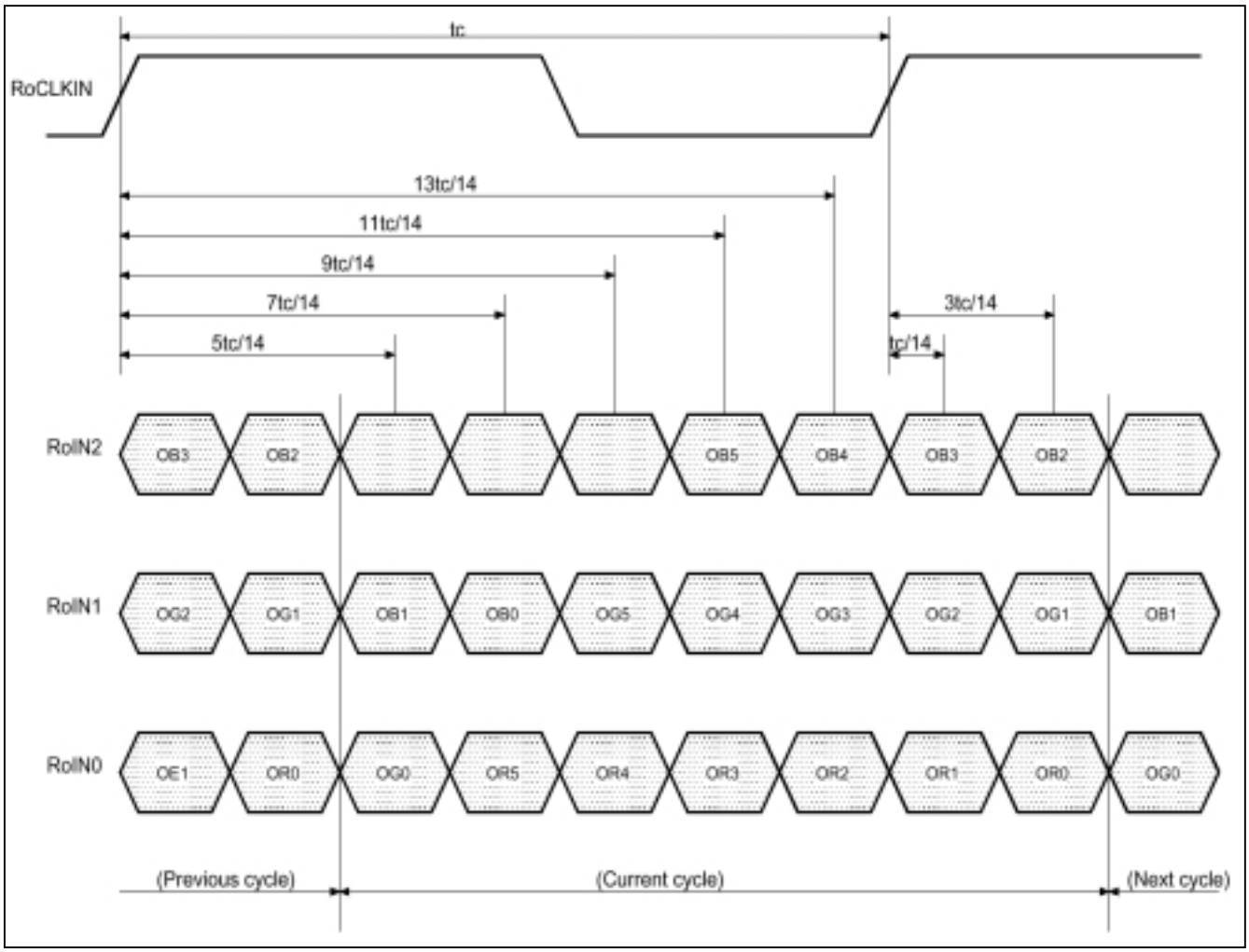
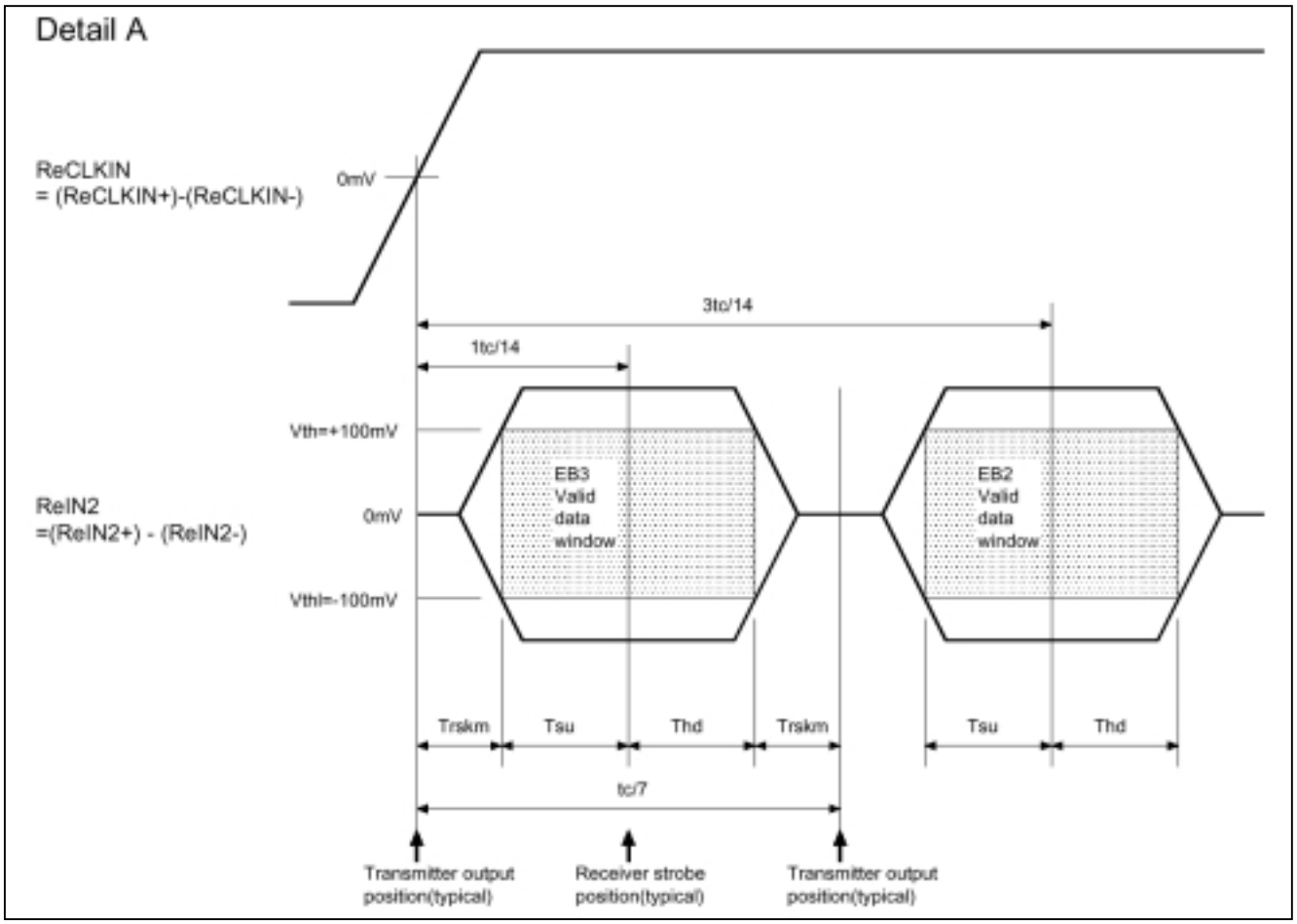


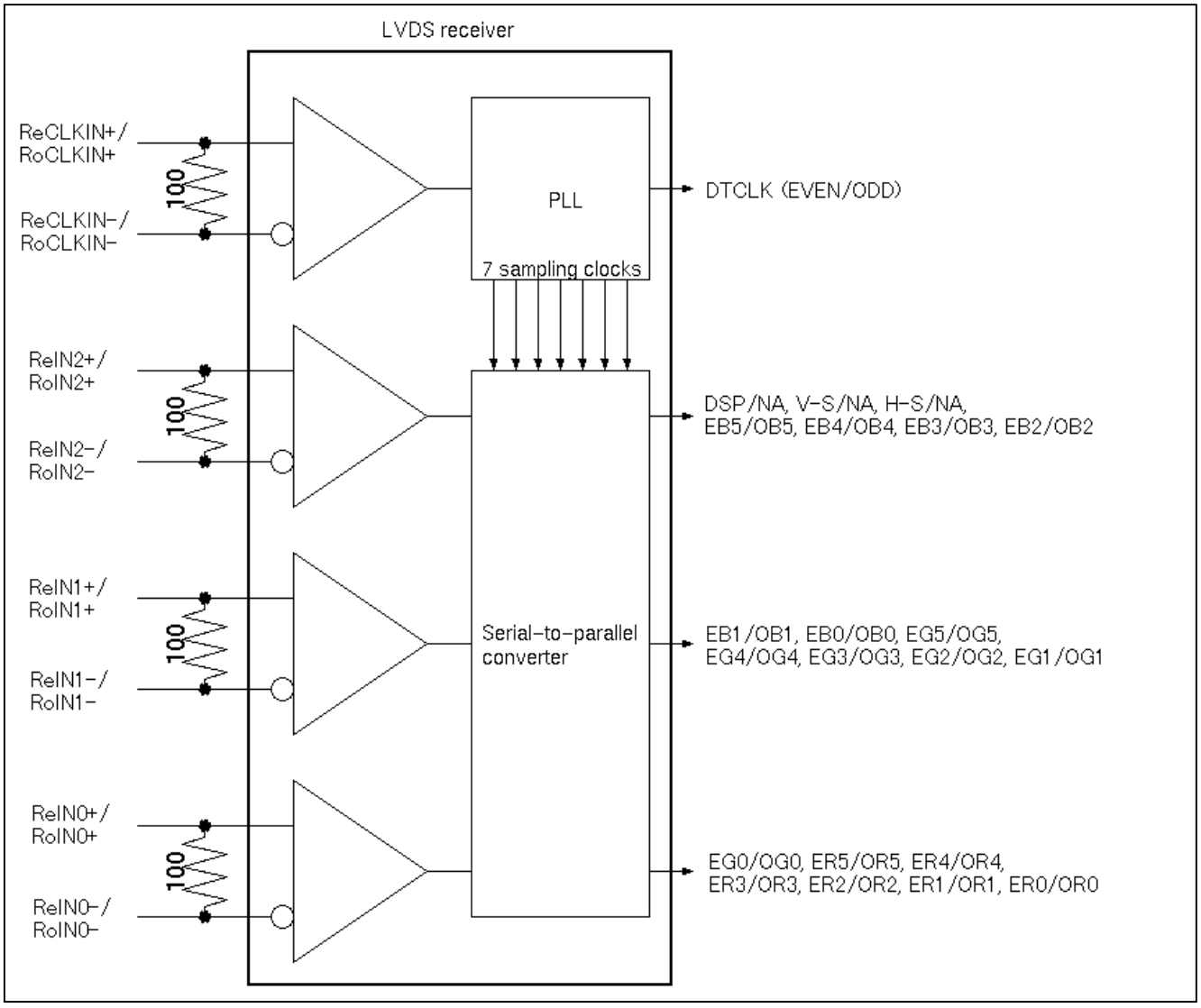
Figure. Timing Definition (detail A)



Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

5.4.2 LVDS Receiver Internal Circuit

Below figure shows the internal block diagram of the LVDS receiver.



5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

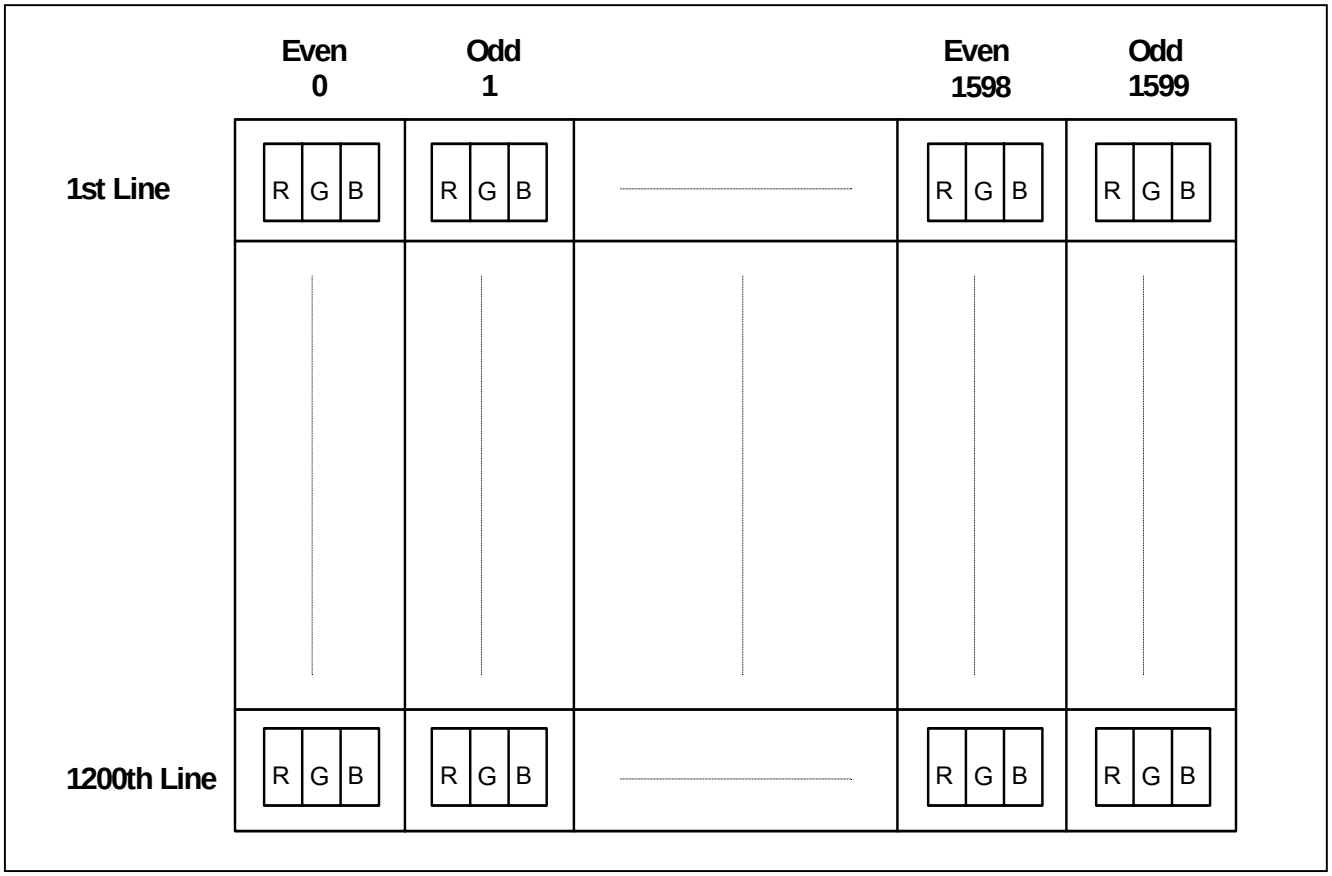
- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image.
Even and odd pair of RGB data are sampled at a time.



7.0 Parameter guide line for CFL Inverter

PARAMETER	MIN	DP-1	MAX	UNITS	CONDITION
White Luminance	-	200 **Note 6**	-	cd/m^2	(Ta=25 deg.C)
CFL current (ICFL)	TBD	6.5 **Note 5**	7.0	mArms	(Ta=25 deg.C)
CFL Frequency (FCFL)	40	-	70	KHz	(Ta=25 deg.C) **Note 1**
CFL Ignition Voltage (Vs)	1,600	-	-	Vrms	(Ta= 0 deg.C) **Note 3**
CFL Voltage (Reference)(VCFL)	-	630	-	Vrms	(Ta=25 deg.C) **Note 2**
CFL Power consumption (PCFL)	-	4.1	4.5	W	(Ta=25 deg.C) **Note 2**

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,600 voltage. Lamp units need 1,600 voltage minimum for ignition.

Note 4: DP-1 (Design Point-1) is IDTech recommended Design Point.

*1 All of characteristics listed are measured under the condition using the IDTech Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

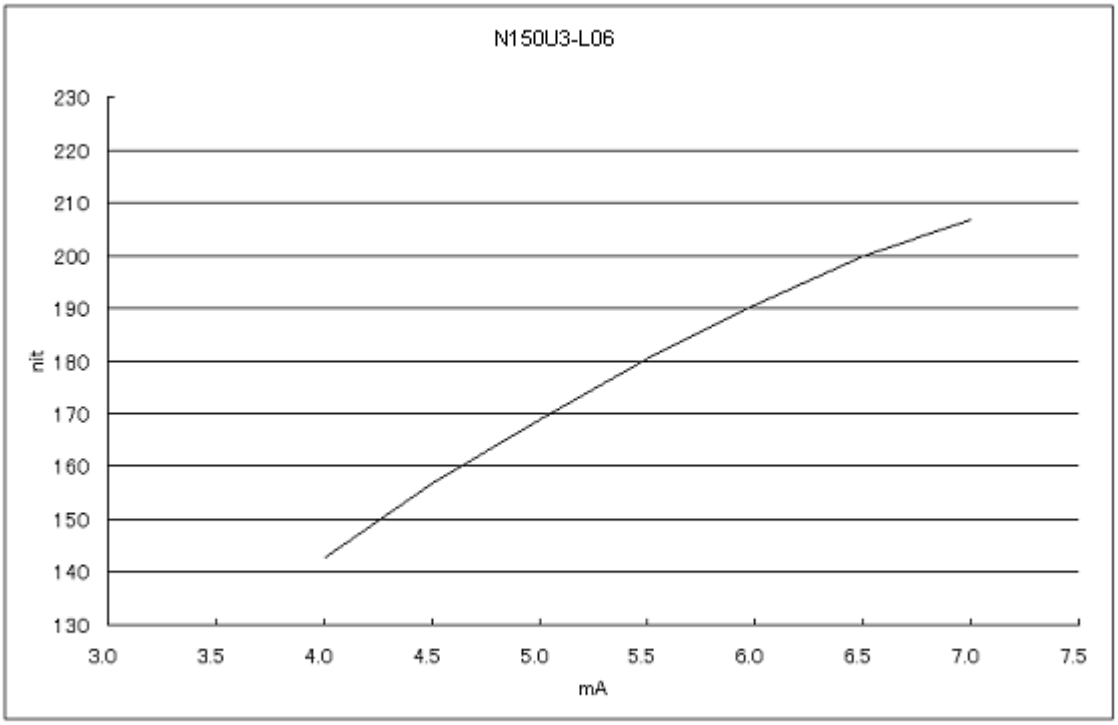
*5 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

*6 It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4[mA].

Note 5: To use inverter card of SANKEN SCF-0281.

Note 6: 200 Typ. (center), 170 Min. (center), 185 Typ. (5 point average)

The following chart is Luminance versus Lamp Power for your reference.



8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86 (Texas Instruments) or equivalent.

8.1 Timing Characteristics

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK (ECLK/OCLK)	Freqency	Fdck	53.0	81.0	83.0	[MHz]
		Tck	12.0	12.3	18.8	[ns]
+V-Sync	Frame Rate	Fv	-	60.0	-	[Hz]
		Tv	-	16.67	-	[ms]
		Nv	1208	1250	2046	[lines]
	V-Active Level	Tva	13.33	40.0	839.8	[us]
		Nva	1	3	63	[lines]
	V-Back Porch	Nvb	6	46	125	[lines]
	V-Front Porch	Nvf	1	1	125	[lines]
+DSPTMG	V-Line	m		1200		[lines]
+H-Sync	Scan Rate	Fh	-	75.0	-	[KHz]
		Th	-	13.33	-	[usec]
		Nh	1024	1080	2046	[Tck]
	H-Active Level	Tha		1.185		[usec]
		Tha	8	96	255	[Tck]
	H-Back Porch	Thb	8	152	511	[Tck]
	H-Front Porch	Thf	8	32		[Tck]
+DSPTMG	Display	Thd	-	9.877	-	[usec]
+DATA	Data Even/Odd	n		1600		[dots]

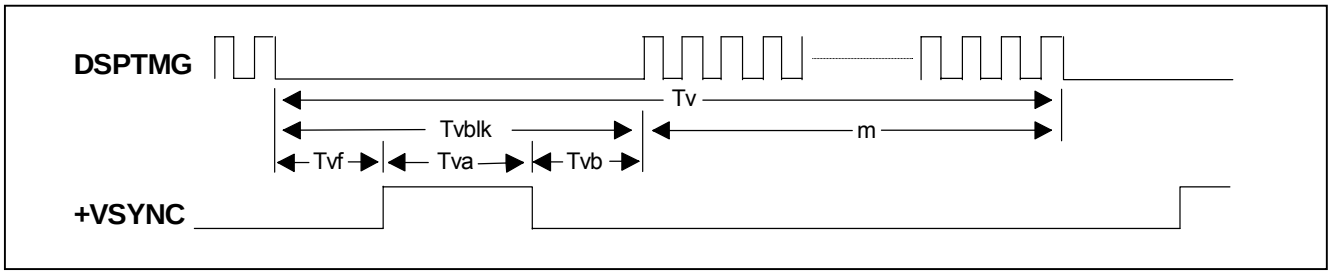
Note: Both positive Hsync and positive Vsync polarity is recommended.

Disp Timing Period (Th, Nh) must be constant by each every line.
If Disp timing are not constant due to Spread Spectrum, the following expression has to be satisfied.
DeltaDT x Tvblk < 300 [Tck]
DTmax : Disp Timing Period MAX [Tck]
DTmin : Disp Timing Period MIN [Tck]
DeltaDT = DTmax - DTmin
Tvblk : V Blanking [lines]
Tck : DTCLK

8.2 Timing Definition

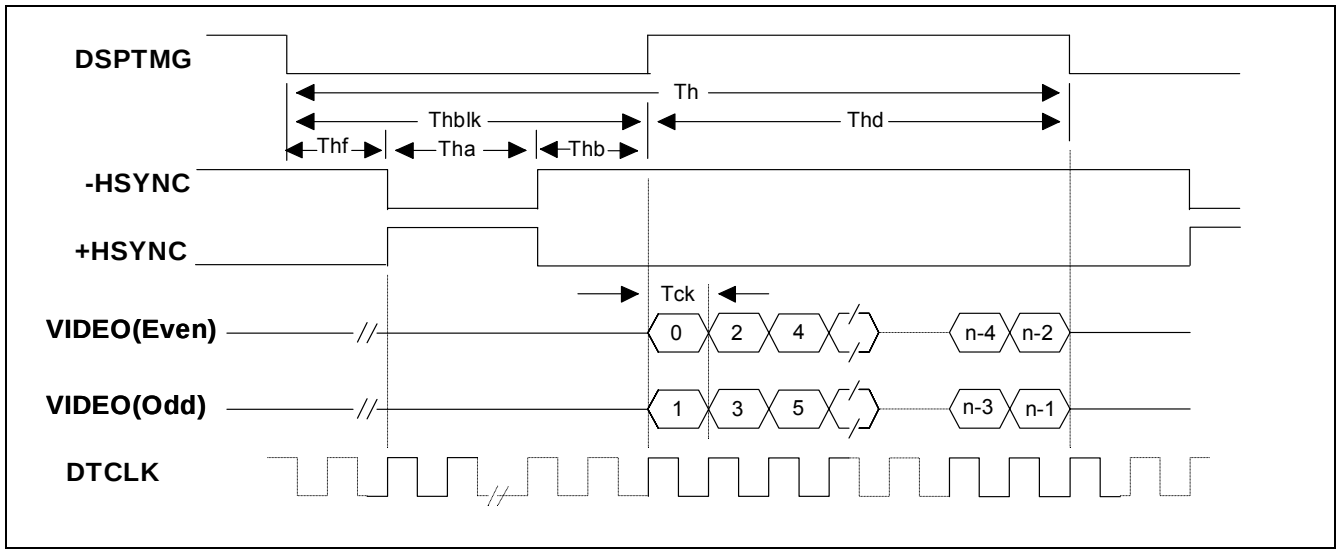
Vertical Timing

Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1600 x 1200 at 60Hz (H line rate : 13.3 us)	0.667 ms (50 lines)	16.000 ms (1200 lines)	0.013 ms (1 line)	16.667 ms (1250 lines)	0.040 ms (3 lines)	0.613 ms (46 lines)



Horizontal Timing

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1600 x 1200 Dotclock : 162.000 MHz (81.000MHz x2)	3.457 us (560 dots)	9.877 us (1600 dots)	0.395 us (64 dots)	13.333 us (2160 dots)	1.185 us (192 dots)	1.877 us (304 dots)



9.0 Power Specifications

Input power specifications are as follows;

Operating Input Voltage Conditions: +3.0V to +3.6V

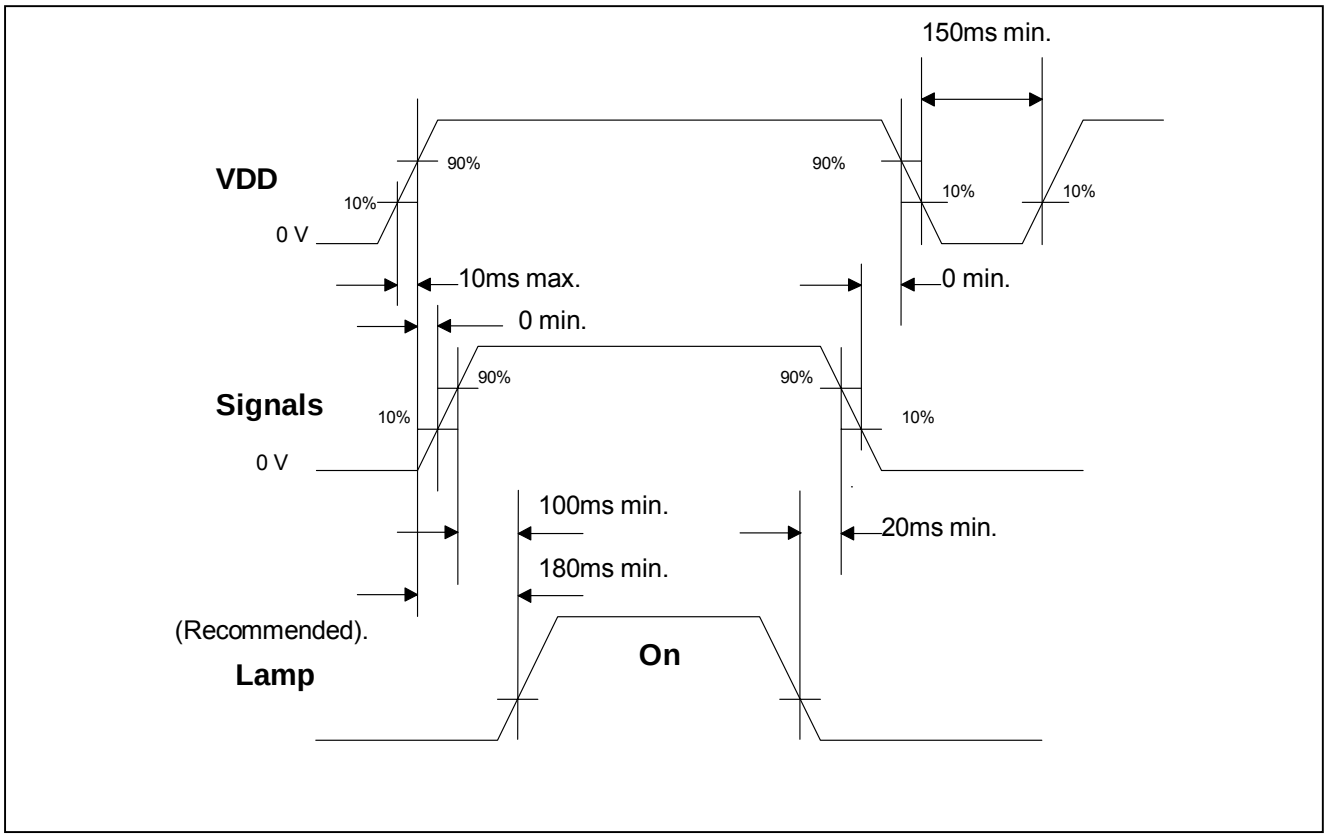
Power Characteristics

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	Load Capacitance 68 uF
PDD	VDD Power			4.4	[W]	MAX.Pattern, VDD=3.6[V]
PDD	VDD Power		3.1		[W]	All White Pattern, VDD=3.3[V]
IDD	VDD Current			1.44	[A]	MAX.Pattern, VDD=3.0[V]
IDD	VDD Current		0.95		[A]	All White Pattern, VDD=3.3[V]
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mVp-p]	

Note: VDD Line impedance of between system side and LCD panel should be minimized for meeting the above requirements.

10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart.
Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics

<Refer to the attached drawing. >

12.0 National Test Lab Requirement

The display module will satisfy all requirements for compliance to

UL 60950, 3rd Edition	U.S.A. Information Technology Equipment
CAN/CSA-C22.2 No.60950-00	Canada, Information Technology Equipment
IEC 60950 (3rd. Ed.)	International, Information Technology Equipment
EN 60950 (3rd. Ed.)	International, Information Processing Equipment (European Norm for IEC60950)

Conditions of Acceptability

For use only in or with complete equipment where the acceptability of the combination is determined by Underwriters laboratories Inc.

When installed in an end-product, consideration must be given to the following:

- The terminals and connectors are suitable for factory wiring only.
- The component has been evaluated for use in a Pollution Degree 2 environment.
- Need for fire and/or electrical enclosures hall be considered in end product.
- The unit is intended to be supplied by SELV and Limited Power Source. Also separated from electrical parts, which may produce high temperature that could cause ignition by at least 13 mm of air or by a solid barrier of material of V-1 minimum due to materials having no flammability rating.
- Back light lamp is rated 630 V rms, 6.5 mA, and intended to be supplied by Limited Current Circuit.
- Insulation between Backlight circuit and other SELV circuit has not been evaluated. Additional consideration shall be made if backlight is supplied by a source other than limited current circuit.

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