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16Mb Ultra-Low Power Asynchronous CMOS SRAM

1024K × 16 bit

Overview

The N16L163WC2C is an integrated memory device containing a 8Mbit Static Random Access Memory organized as 1,048,576 words by 16 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with two chip enable ($\overline{CE1}$ and CE2) controls and output enable ($\overline{OE}$) to allow for easy memory expansion. Byte controls ($\overline{UB}$ and $\overline{LB}$) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The N16L163WC2C is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40^{o}C to +85^{o}C and is available in JEDEC standard packages compatible with other standard 1024Kb x 16 SRAMs

Features

- **Single Wide Power Supply Range**
  2.2 to 3.6 Volts
- **Very low standby current**
  2.5µA at 3.0V (Typical)
- **Very low operating current**
  2.0mA at 3.0V and 1µs(Typical)
- **Simple memory control**
  Dual Chip Enables ($\overline{CE1}$ and CE2)
  Byte control for independent byte operation
  Output Enable ($\overline{OE}$) for memory expansion
- **Low voltage data retention**
  Vcc = 1.5V
- **Very fast output enable access time**
  25ns $\overline{OE}$ access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **Ultra Low Power Sort Available**

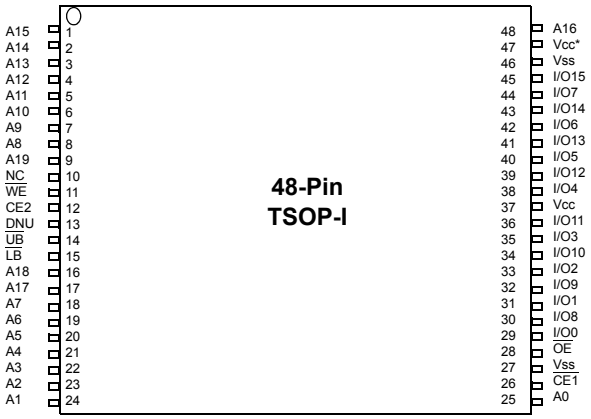
Product Family

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I_{SB}), Typical	Operating Current (Icc), Typical
N16L163WC2CT1	48 TSOP I Pb-Free	-40^{o}C to +85^{o}C	2.2V - 3.6V	55ns	2.5 µA	2 mA @ 1MHz
N16L163WC2CZ1	VFBGA Pb-Free					

Pin Configuration

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CE2
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	DNU	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A18	A_8	A_9	A_{10}	A_{11}	DNU

48 Pin VFBGA (top)
8 x 10 mm

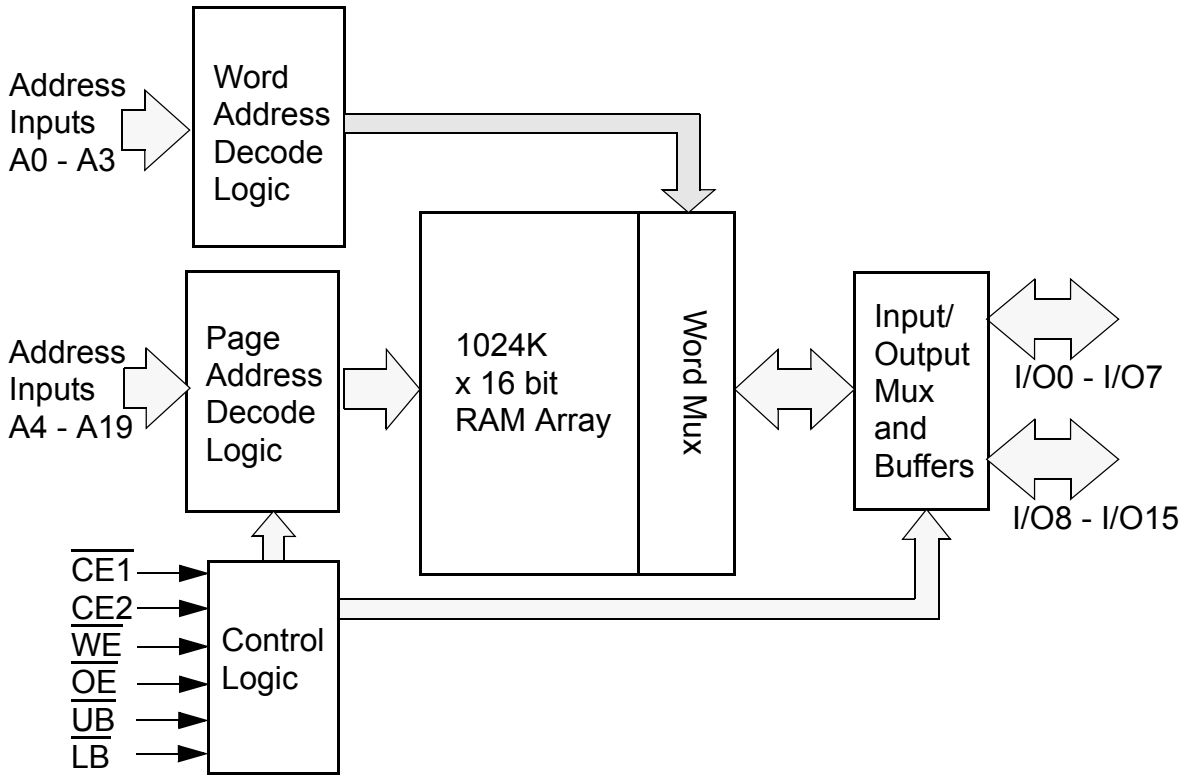


Note: Pin#47 on the TSOP-I Package must be tied to Vcc.

Pin Descriptions

Pin Name	Pin Function
A_0-A_{19}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$, CE2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
NC	Not Connected
DNU	Do Not Use

Functional Block Diagram



Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O_0 - I/O_{15}[1]	MODE	POWER
H	X	X	X	X	X	High Z	Standby[2]	Standby
X	L	X	X	X	X	High Z	Standby[2]	Standby
X	X	X	X	H	H	High Z	Standby[2]	Standby
L	H	L	X[3]	L[1]	L[1]	Data In	Write[3]	Active
L	H	H	L	L[1]	L[1]	Data Out	Read	Active
L	H	H	H	L[1]	L[1]	High Z	Active	Active

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - I/O_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown.
2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		10	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–65 to 150	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec	°C

Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions		Min.	Typ[1]	Max	Unit
Supply Voltage	V_{CC}			2.2	3.0	3.6	V
Data Retention Voltage	V_{DR}	Chip Disabled		1.5			V
Input High Voltage	V_{IH}	Vcc = 2.2V to 2.7V		1.8		V_{CC}+0.3	V
		Vcc = 2.7V to 3.6V		2.2		V_{CC}+0.3	
Input Low Voltage	V_{IL}	Vcc = 2.2V to 2.7V		-0.3		0.6	V
		Vcc = 2.7V to 3.6V		-0.3		0.8	
Output High Voltage	V_{OH}	I_{OH} = -0.1mA, Vcc = 2.2V		2.0			V
		I_{OH} = -1.0mA, Vcc = 2.7V		2.4			
Output Low Voltage	V_{OL}	I_{OL} = 0.1mA, Vcc = 2.2V				0.4	V
		I_{OL} = 0.1mA, Vcc = 2.7V				0.4	
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		-1		1	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled		-1		1	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0			2	4.0	mA
			-L		2	4.0	
Read/Write Operating Supply Current @ fmax	I_{CC2}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0			15	30	mA
			-L		15	30	
Maximum Standby Current	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 85°C, V_{CC} = 3.6 V			2.5	30	µA
			-L		2.5	22	
Maximum Data Retention Current	I_{DR}	Vcc = 1.5V, V_{IN} = V_{CC} or 0				15	µA
		Chip Disabled, t_A= 85°C	-L			10	

1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	1V/ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 50pF
Operating Temperature	-40 to +85 ^{O}C

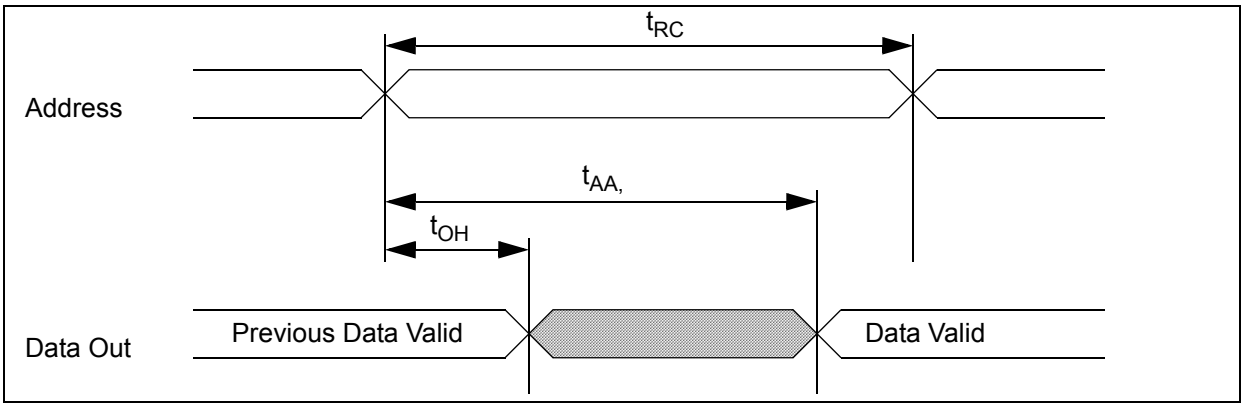
Timing

Item	Symbol	55		Units
		Min	Max	
Read Cycle Time	t_{RC}	55		ns
Address Access Time (Random Access)	t_{AA}		55	ns
Chip Enable to Valid Output	t_{CO}		55	ns
Output Enable to Valid Output	t_{OE}		25	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		55	ns
Chip Enable to Low-Z output	t_{LZ}	10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		ns
Chip Disable to High-Z Output	t_{HZ}		20	ns
Output Disable to High-Z Output	t_{OHZ}		20	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}		20	ns
Output Hold from Address Change	t_{OH}	10		ns
Write Cycle Time	t_{WC}	55		ns
Chip Enable to End of Write	t_{CW}	40		ns
Address Valid to End of Write	t_{AW}	40		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	40		ns
Write Pulse Width	t_{WP}	40		ns
Address Setup Time	t_{AS}	0		ns
Write Recovery Time	t_{WR}	0		ns
Write to High-Z Output	t_{WHZ}		20	ns
Data to Write Time Overlap	t_{DW}	25		ns
Data Hold from Write Time	t_{DH}	0		ns
End Write to Low-Z Output	t_{OW}	10		ns

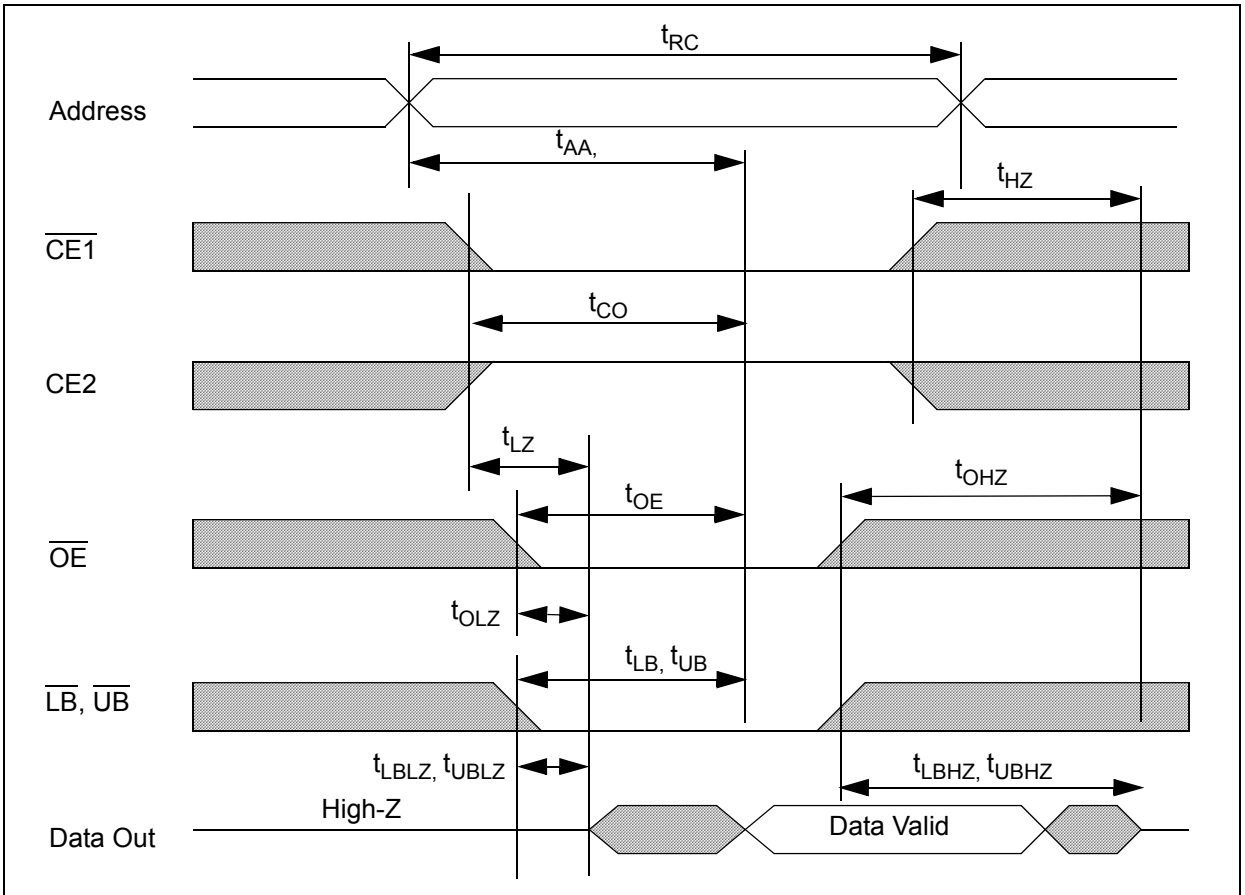
Note:

1. Full Device AC operation requires linear Vcc ramp from 0 to Vcc(min) ≥ 500us.
2. Full Device operation requires linear Vcc ramp from V_{DR} to Vcc(min) ≥ 100 us or stable at Vcc(min) ≥ 100us.
3. Address valid prior to or coincident with $\overline{CE1}$, $\overline{LB}$, $\overline{UB}$ transition LOW and CE2 transition HIGH.

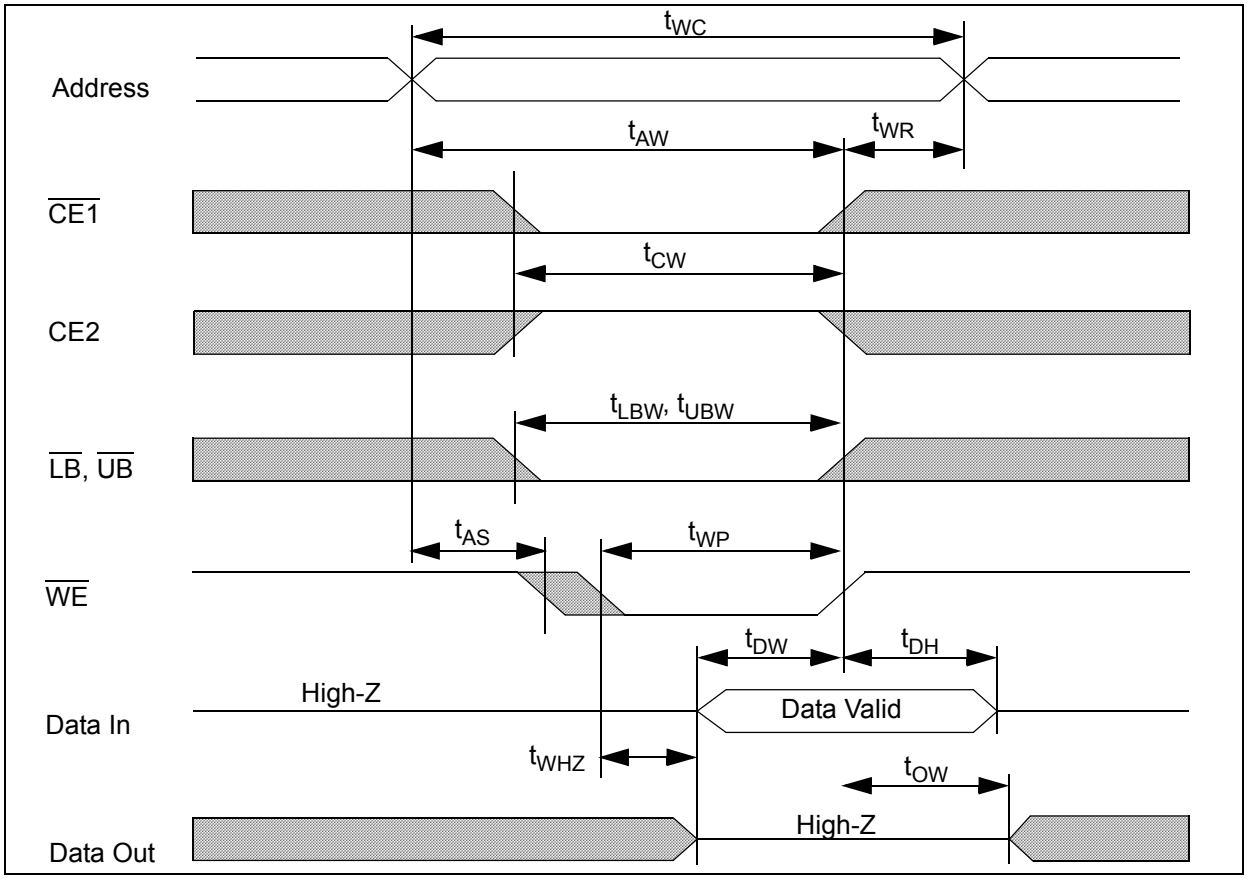
Timing of Read Cycle ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CE2 = V_{IH})



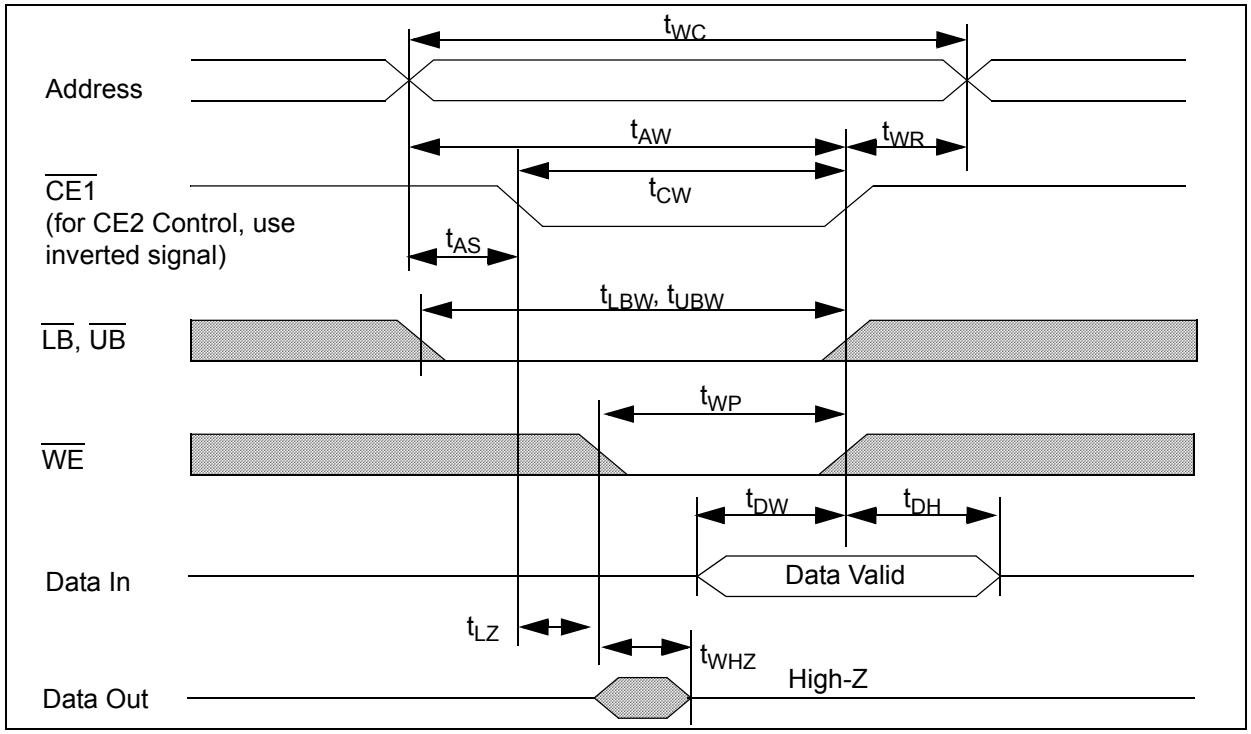
Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})



Timing Waveform of Write Cycle ($\overline{WE}$ control)



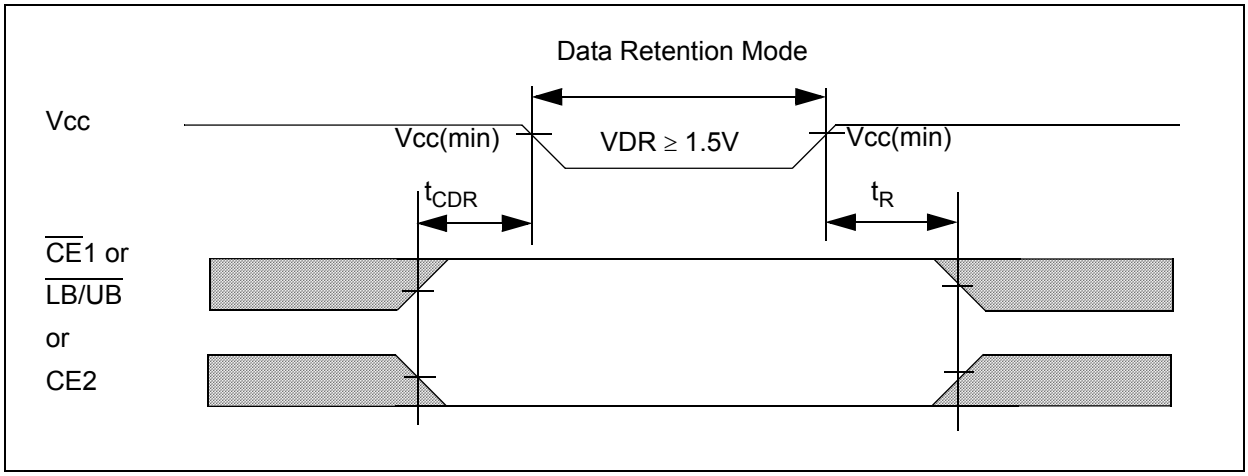
Timing Waveform of Write Cycle ($\overline{CE1}$ Control)



Data Retention Characteristics

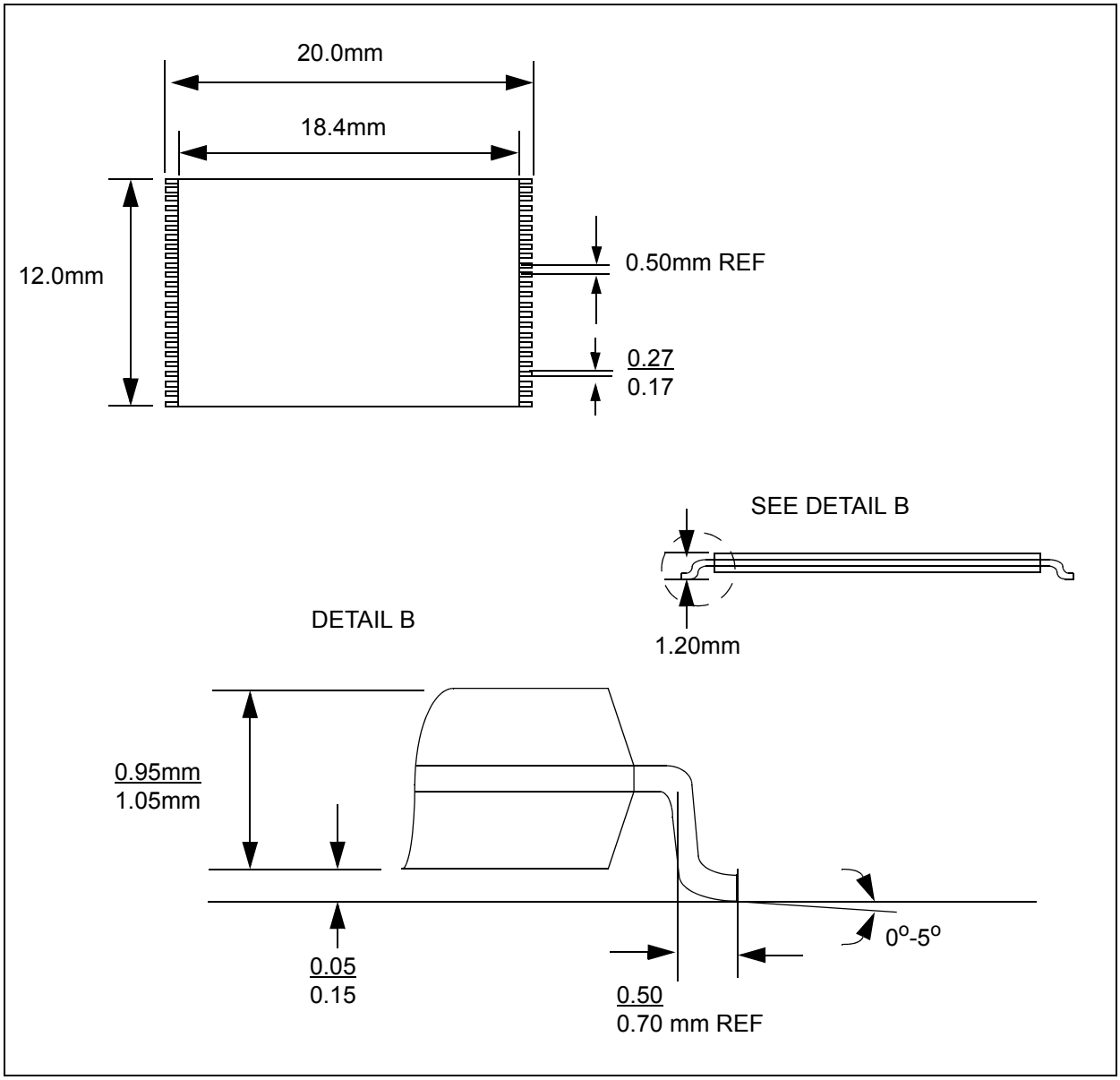
Parameter	Description	Condition		Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	Vcc = 1.5V, CE ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V				15	µA
			-L			10	
t_{CDR}	Chip Deselect to Data Retention Time			0			ns
t_R	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform



Note: Full device operation requires linear Vcc ramp from VDR to Vcc(min) > 100 µs

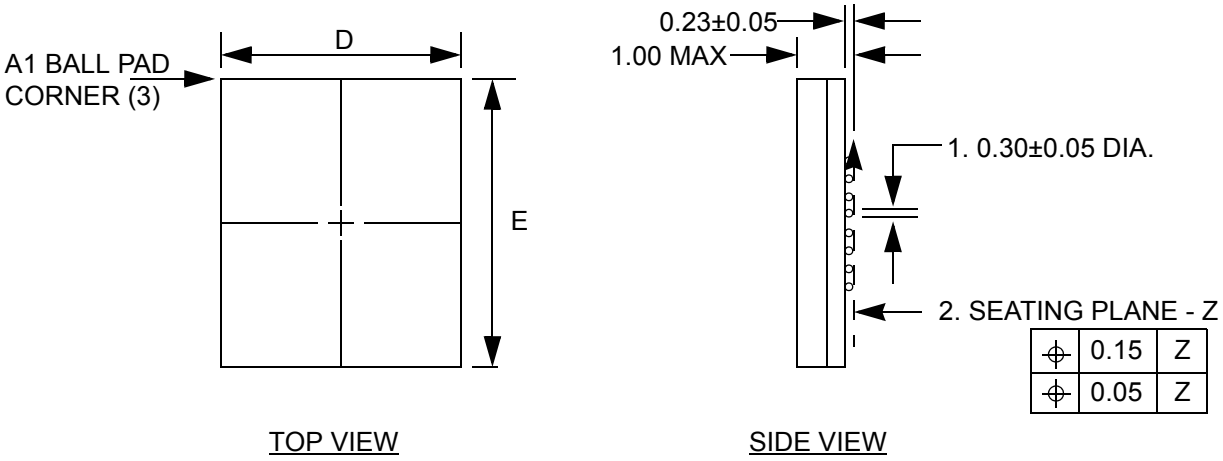
48 TSOP-I Package (Z48A)

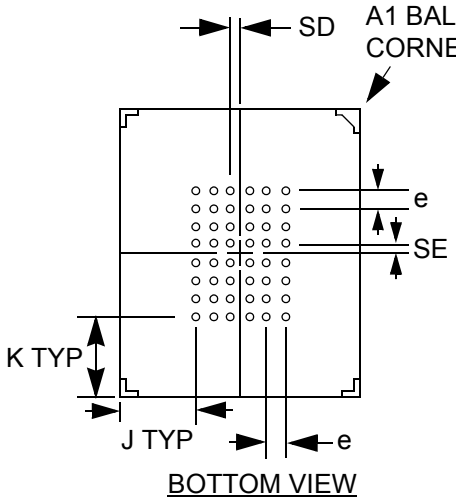


Note:

1. All dimensions in millimeters.

VFBGA Package





1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

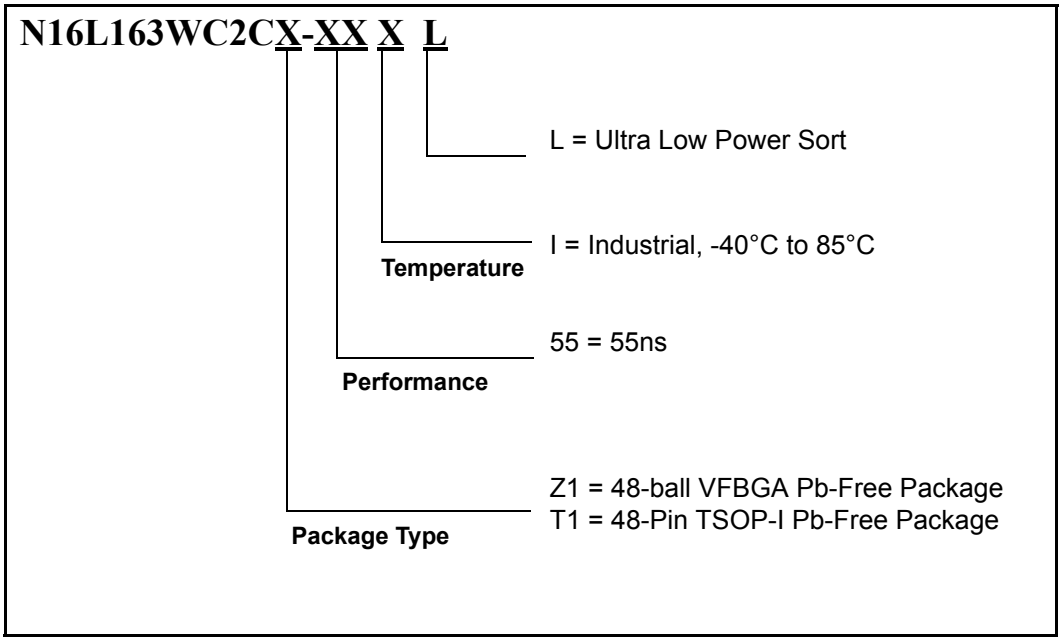
2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
8±0.10	10±0.10	0.375	0.375	2.125	2.375	FULL

Ordering Information



Revision History

Revision	Date	Change Description
A	Oct 6. 2004	Initial Advance Release
B	Nov 10. 2004	General Update
C	Jan 14. 2005	General Update