TFT LCD Approval Specification

MODEL NO.: N170C3 - L02

Customer : JVC

Approved by :

Note :

記錄	工作	審核	角色	投票
2007-08-21 14:15:43 CST	PMMD Director	cs_lee(李志聖 /56510/44926)	Director	Accept

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 3.0	Aug. 10,2007	All	All	Approval Specification was first issued

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N170C3 - L02 is a 17.0" TFT Liquid Crystal Display module with two CCFLs Backlight unit and 30 pins LVDS interface. This module supports 1440 x 900 Wide-XGA+ mode and can display 16,777,216 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

1.2 FEATURES

- Thin and High Brightness
- WXGA+ (1440 x 900 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock
- 2 CCFLs

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	367.2 (H) x 229.5 (V) (17.0" diagonal)	mm	(1)
Bezel Opening Area	371.2 (H) x 233.5 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1440 x R.G.B. x 900	pixel	-
Pixel Pitch	0.255 (H) x 0.255 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Glare Type	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	381.7	382.2	382.7	mm	(1)
	Vertical (V)	246.3	246.8	247.3	mm	
	Depth (D)	---	9.7 / 7.9	10.0~8.2	mm	
Weight		---	930	960	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

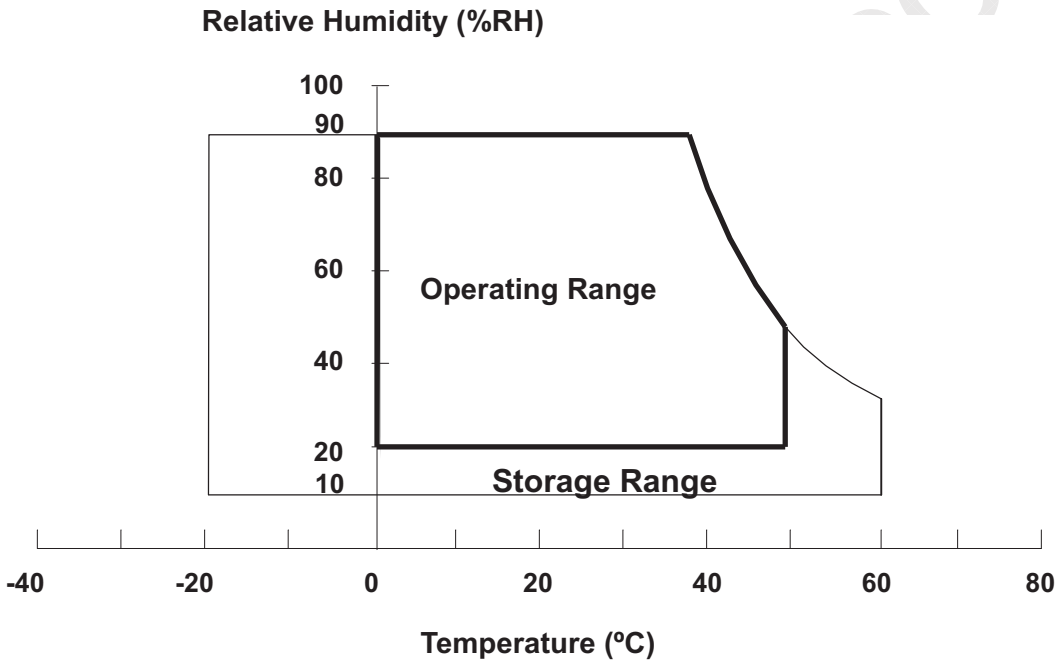
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	H_{ST}	-	200/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.



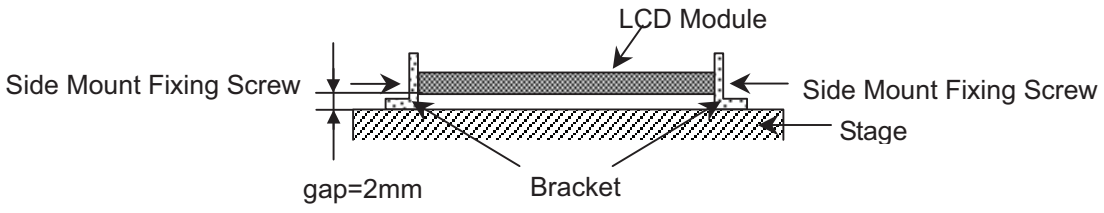
Note (2) The temperature of panel display surface should be 0 ºC Min and 60 ºC Max.

Note (3) 1 time for ± X, ± Y, ± Z. for Condition (200G / 2ms) is half Sine Wave.

Note (4) 10 ~ 500 Hz, 0.5 Hr / Cycle, 1 cycles for each X, Y, Z axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	V_{CC}+0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	—	2.5K	V_{RMS}	(1), (2), I_L = 6.0 mA
Lamp Current	I_L	2	6.0	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	50	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

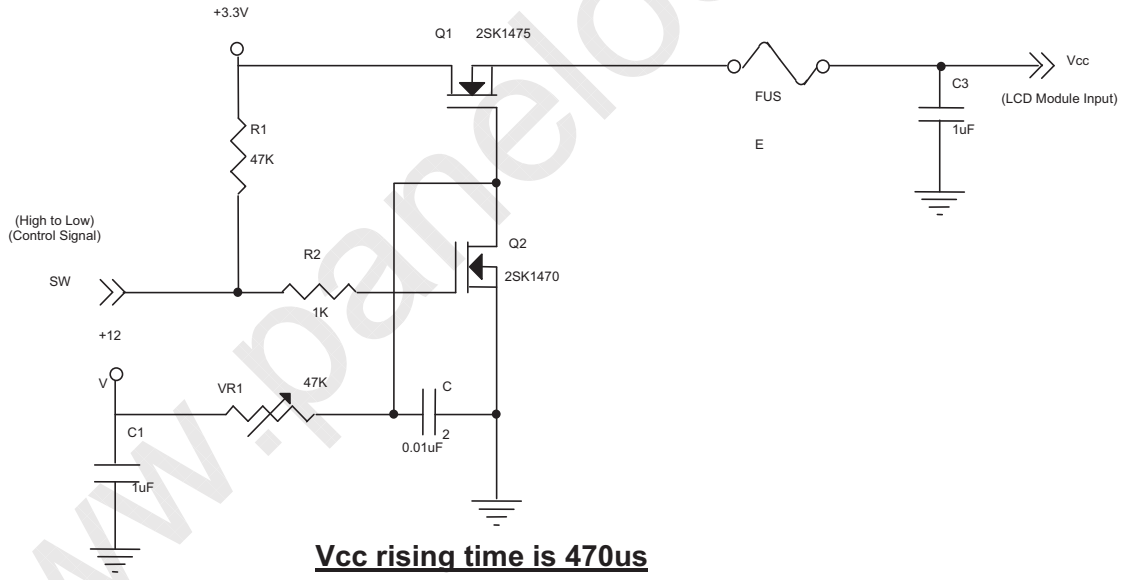
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}		100		mV	-
Rush Current		I_{RUSH}			1.5	A	(2)
Power Supply Current	White	Icc		450		mA	(3)a
	Black			570		mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$	-	-	+100	mV	(5), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100	-	-	mV	(5), V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125	-	1.375	V	(5)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100	-	600	mV	(5)
Terminating Resistor		R_T		100		Ohm	
Power per EBL WG		P_{EBL}	-	4.52	-	W	(4)

Note (1) The module should be always operated within above ranges.

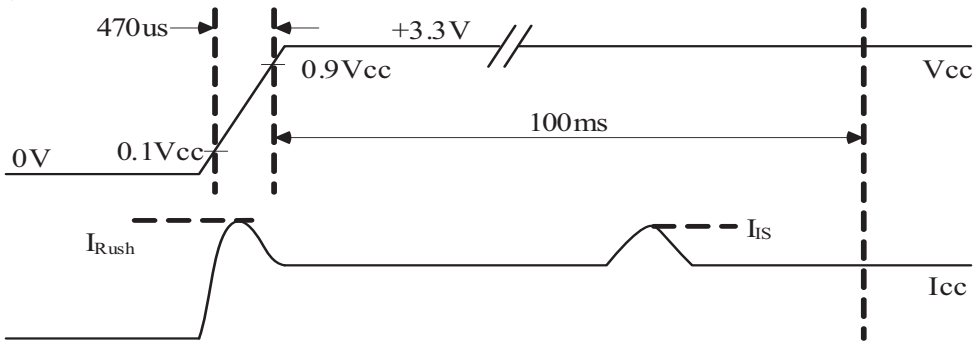
Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

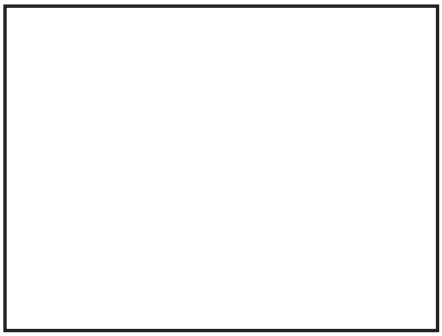


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

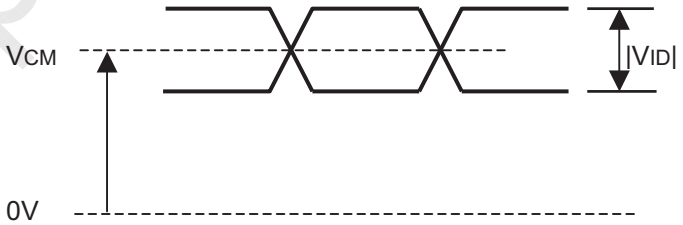
(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

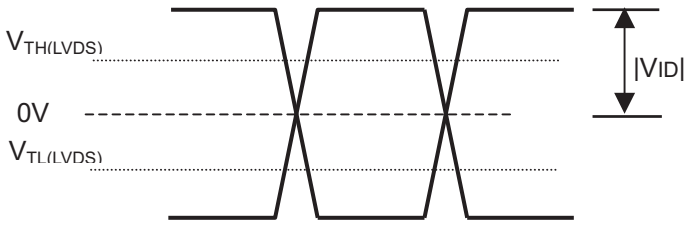
(d) The inverter used is provided from Sumida. Please contact them for detail information. CMO doesn't provide the inverter in this product.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential

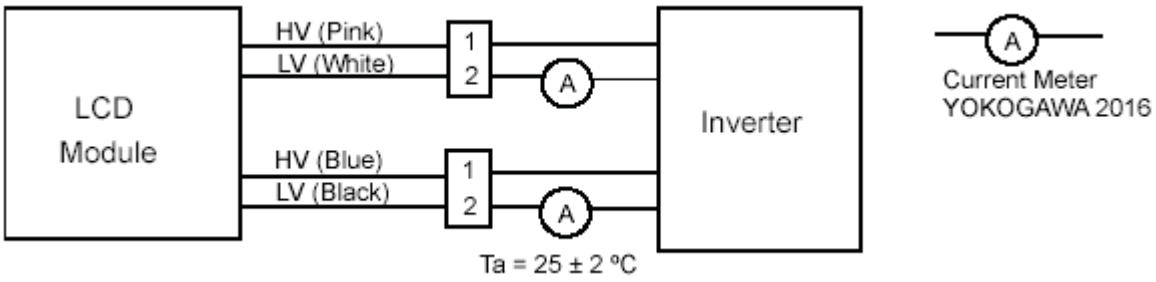


3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	675	750	825	V_{RMS}	I_L = 6.0 mA
Lamp Current	I_L	2.0	6.0	6.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	—	—	1290 (25 °C)	V_{RMS}	(2)
		—	—	1560 (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	50	—	80	KHz	(3)
Lamp Life Time	L_{BL}	12,000	20,000	—	Hrs	(5)
Power Consumption	P_L	—	9.0	—	W	(4), I_L = 6.0 mA

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L \times 2$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I_L = 6.0 mArms until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

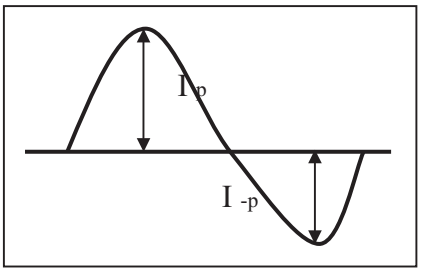
Requirements for a system inverter design, which is intended to have a better display performance, a

better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within $\sqrt{2}$ ± 10%;

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

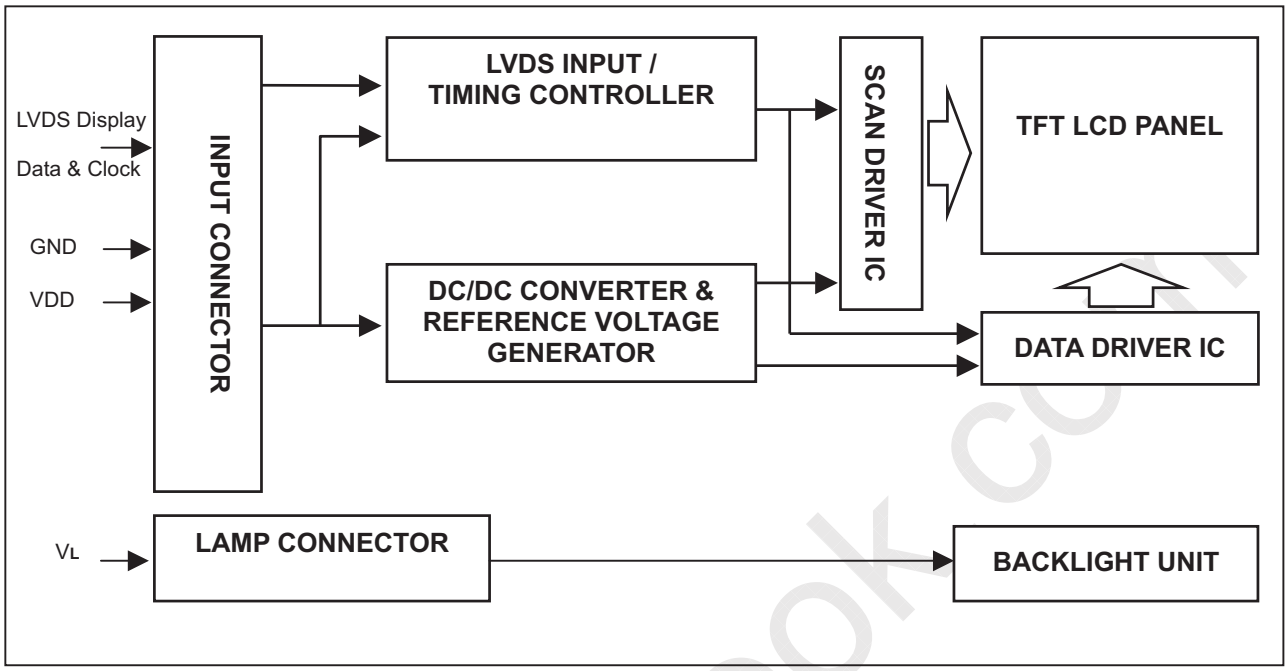
$$| I_p - I_{-p} | / I_{rms} * 100\%$$

* Distortion rate

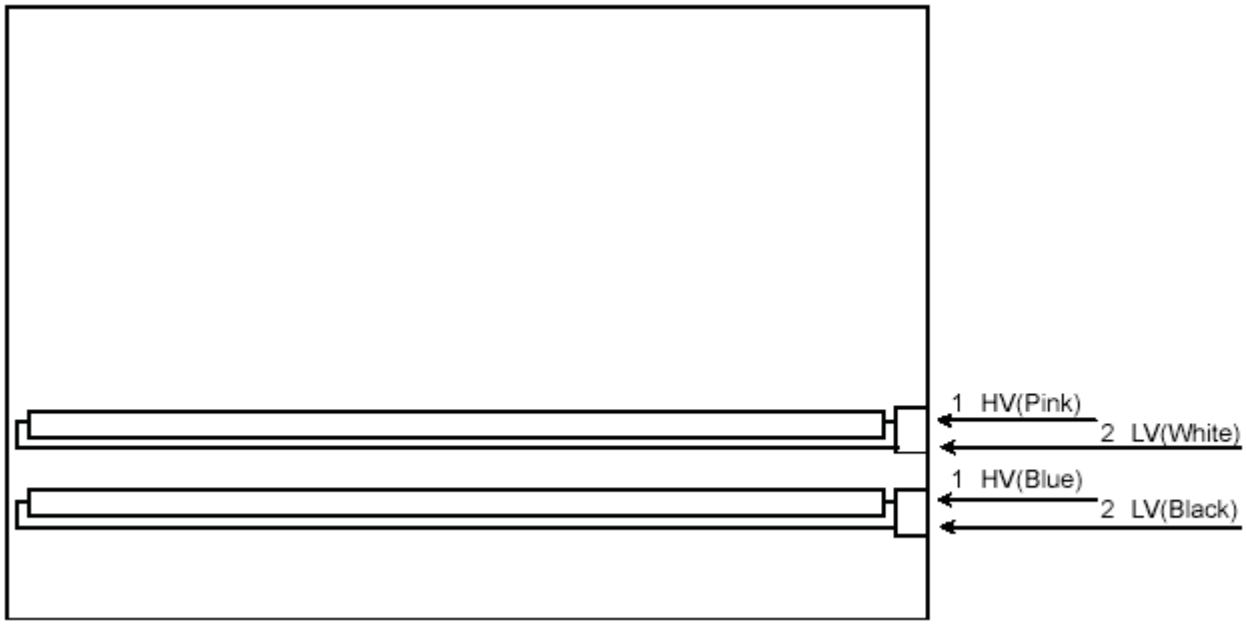
$$I_p \text{ (or } I_{-p}) / I_{rms}$$

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

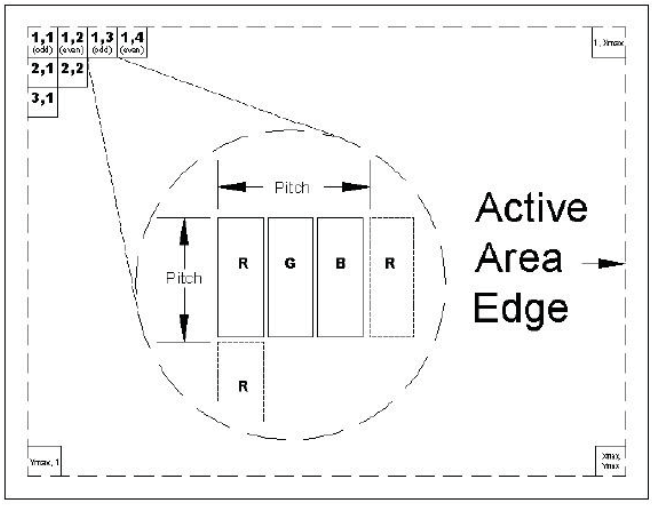
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	RXO0-	LVDS Differential Data Input (Odd)	Negative	
2	RXO0+	LVDS Differential Data Input (Odd)	Positive	
3	RXO1-	LVDS Differential Data Input (Odd)	Negative	
4	RXO1+	LVDS Differential Data Input (Odd)	Positive	
5	RXO2-	LVDS Differential Data Input (Odd)	Negative	
6	RXO2+	LVDS Differential Data Input (Odd)	Positive	
7	GND	Ground		
8	RXOC-	LVDS Differential Clock Input (Odd)	Negative	
9	RXOC+	LVDS Differential Clock Input (Odd)	Positive	
10	RXO3-	LVDS Differential Data Input (Odd)	Negative	
11	RXO3+	LVDS Differential Data Input (Odd)	Positive	
12	RXE0-	LVDS Differential Data Input (Even)	Negative	
13	RXE0+	LVDS Differential Data Input (Even)	Positive	
14	GND	Ground		
15	RXE1-	LVDS Differential Data Input (Even)	Negative	
16	RXE1+	LVDS Differential Data Input (Even)	Positive	
17	GND	Ground		
18	RXE2-	LVDS Differential Data Input (Even)	Negative	
19	RXE2+	LVDS Differential Data Input (Even)	Positive	
20	RXEC-	LVDS Differential Data Clock (Even)	Negative	
21	RXEC+	LVDS Differential Data Clock (Even)	Positive	
22	RXE3-	LVDS Differential Data Input (Even)	Negative	
23	RXE3+	LVDS Differential Data Input (Even)	Positive	
24	GND	Ground		
25	NC	Non-Connection		
26	NC	Non-Connection		
27	NC	Non-Connection		
28	VDD	Power Supply +3.3 V (typical)		
29	VDD	Power Supply +3.3 V (typical)		
30	VDD	Power Supply +3.3 V (typical)		

Note (1) Connector Part No.: JAE-FI-XB30SRL-HF11 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

Note (3) The first pixel is odd as shown in the following figure.



5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	White
1	HV	High Voltage	Blue
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL

LVDS RXE0+/-	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS RXE1+/-	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS RXE2+/-	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS RXE3+/-	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6
LVDS RXO0+/-	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS RXO1+/-	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS RXO2+/-	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS RXO3+/-	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	G5	G4	G3	G2	G1	G0	R7	R6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

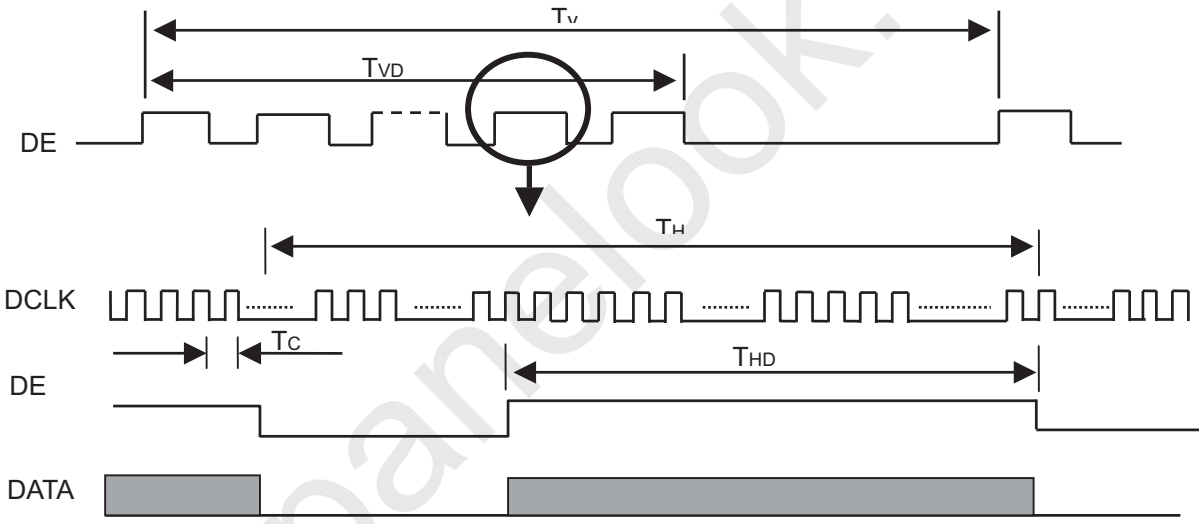
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	42	44.5	52	MHz	(2)
DE	Vertical Total Time	TV	910	926	980	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	26	TV-TVD	TH	
	Horizontal Total Time	TH	760	800	880	Tc	(2)
	Horizontal Active Display Period	THD	720	720	720	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	80	TH-THD	Tc	(2)

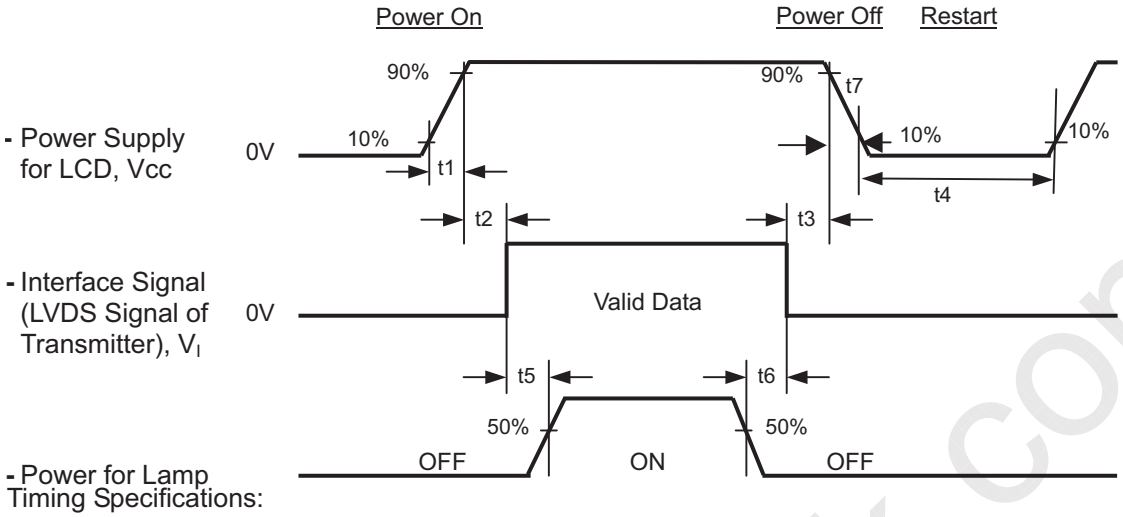
Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

(2) 2 channels LVDS input.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5 ≦ t1 ≦ 10 ms

0 ≦ t2 ≦ 50 ms

0 ≦ t3 ≦ 50 ms

t4 ≧ 500 ms

t5 ≧ 200 ms

t6 ≧ 200 ms

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 5≦t7≦300 ms

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

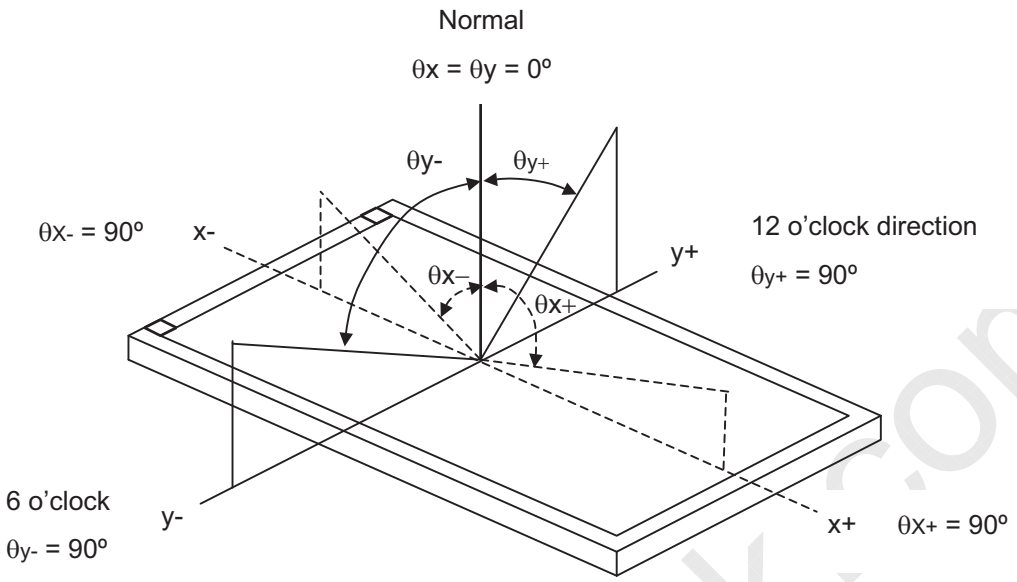
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	6.0	mA
Inverter Driving Frequency	F_L	61	KHz
Inverter	(Sumida-H05-4915)		

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	θ_x=0°, θ_Y =0° Viewing Normal Angle	Typ – 0.03	0.643	Typ + 0.03	—	(1), (6)
		Ry			0.349			
	Green	Gx			0.281			
		Gy			0.609			
	Blue	Bx			0.142			
		By			0.068			
	White	Wx			0.313			
		Wy			0.329			
Center Luminance of White		Lcen		340	400	—	cd/m^2	(4), (6)
Contrast Ratio		CR		400	600	—	—	(2), (6)
Response Time		T_R		—	3	8	ms	(3)
		T_F		—	7	12	ms	
White Variation		δW		—	1.25	1.40	—	(5)
Viewing Angle	Horizontal	θ_x+	CR ≧ 10	70	80	—	Deg.	(1)
		θ_x-		70	80	—		
	Vertical	θ_Y+		60	70	—		
		θ_Y-		60	70	—		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

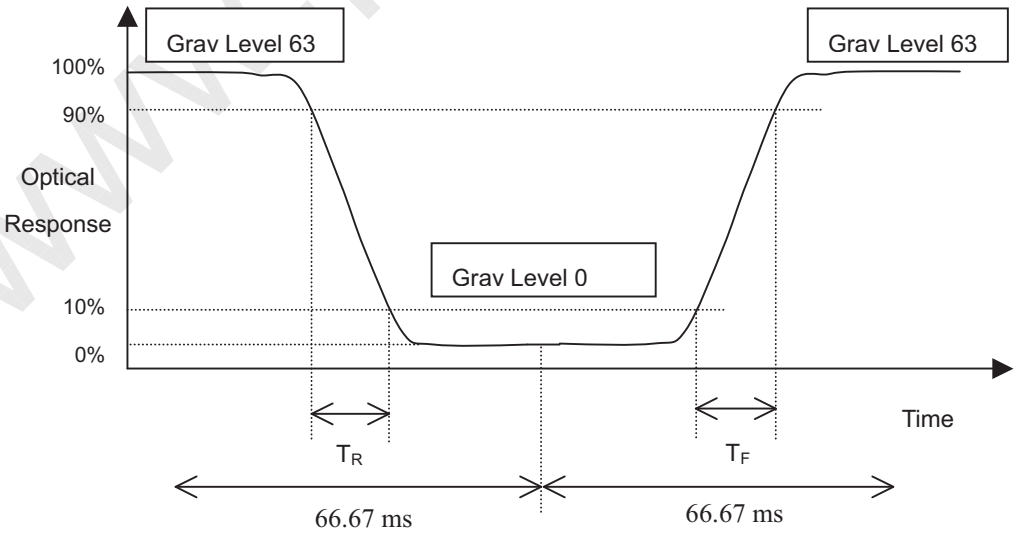
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

Note (3) Definition of Response Time (T_R, T_F) and measurement method:



Note (4) Definition of Center Luminance of White (L_{CEN}):

Measure the luminance of gray level 63 at center points

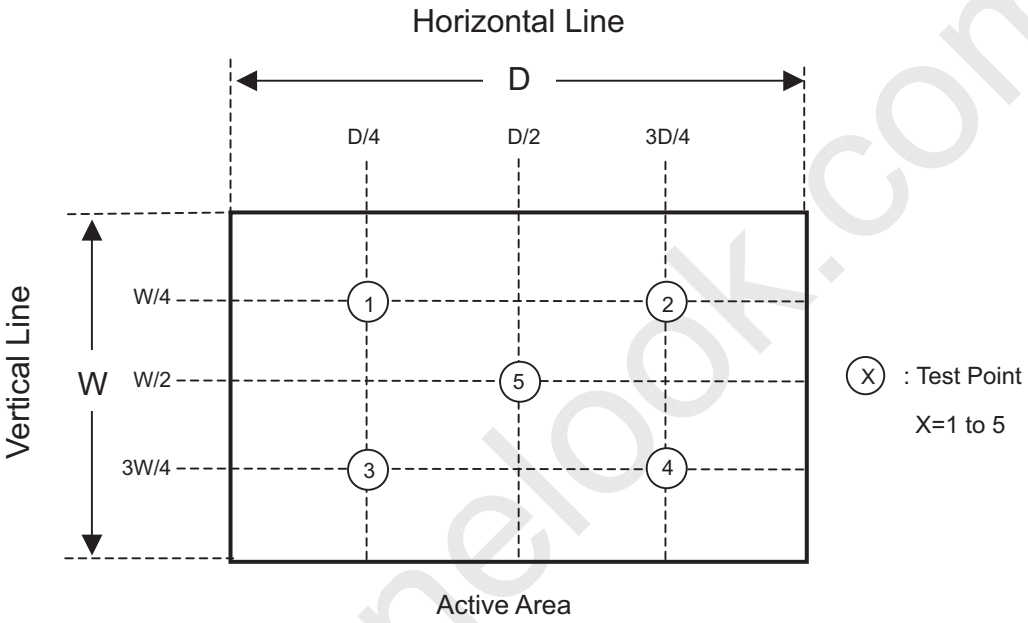
L_{CEN} = L (5)

L (x) is corresponding to the luminance of the point X at Figure in Note (5)

Note (5) Definition of White Variation (δW):

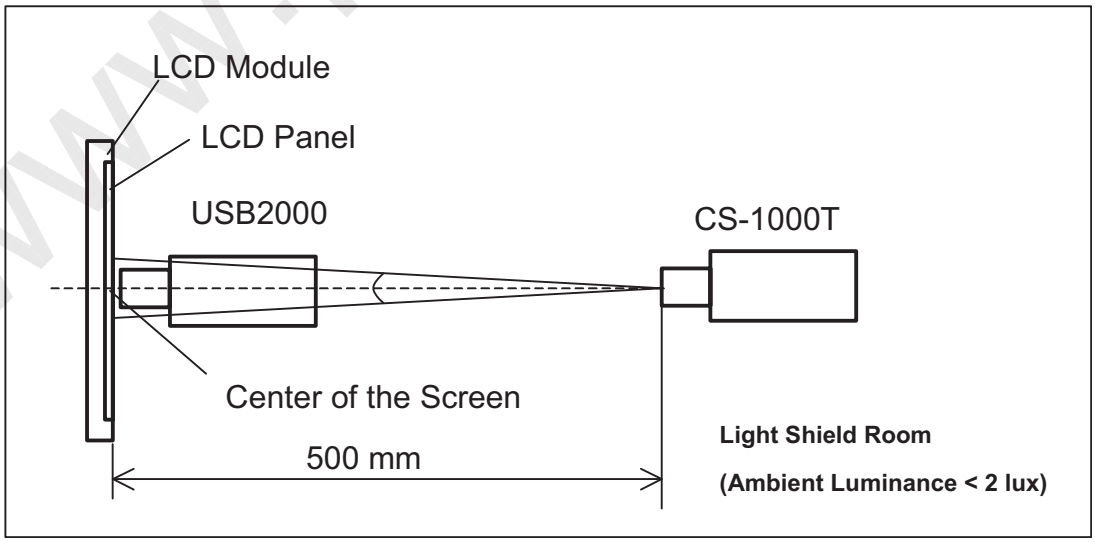
Measure the luminance of gray level 63 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(10) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

8.2 SAFETY PRECAUTIONS

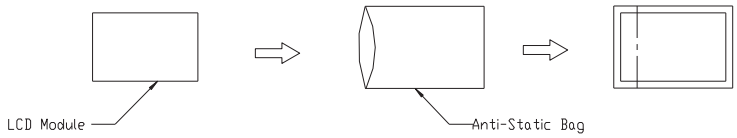
(1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

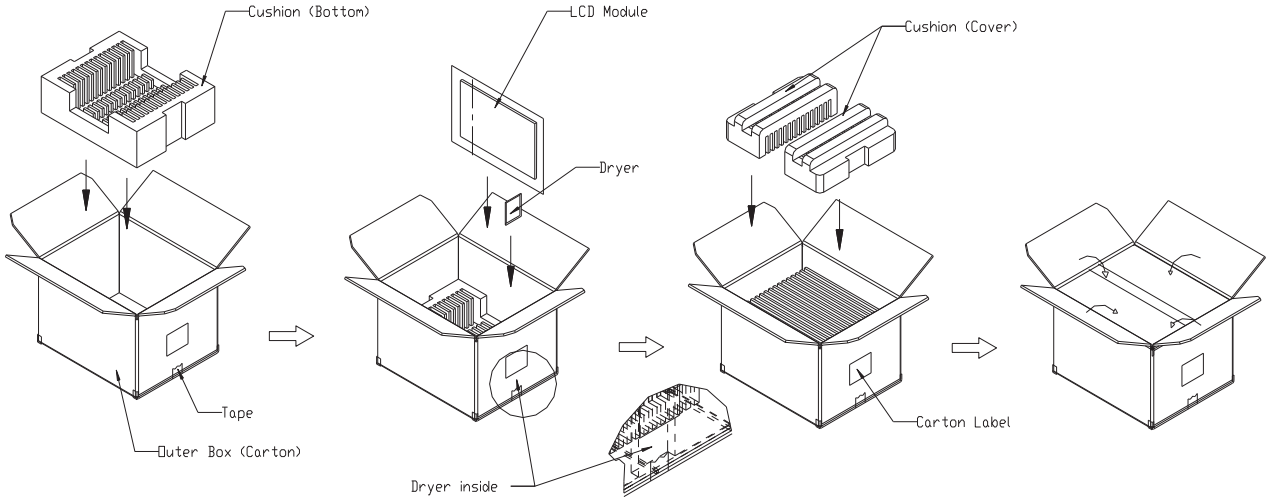
(3) After the module's end of life, it is not harmful in case of normal operation and storage.

9. PACKING

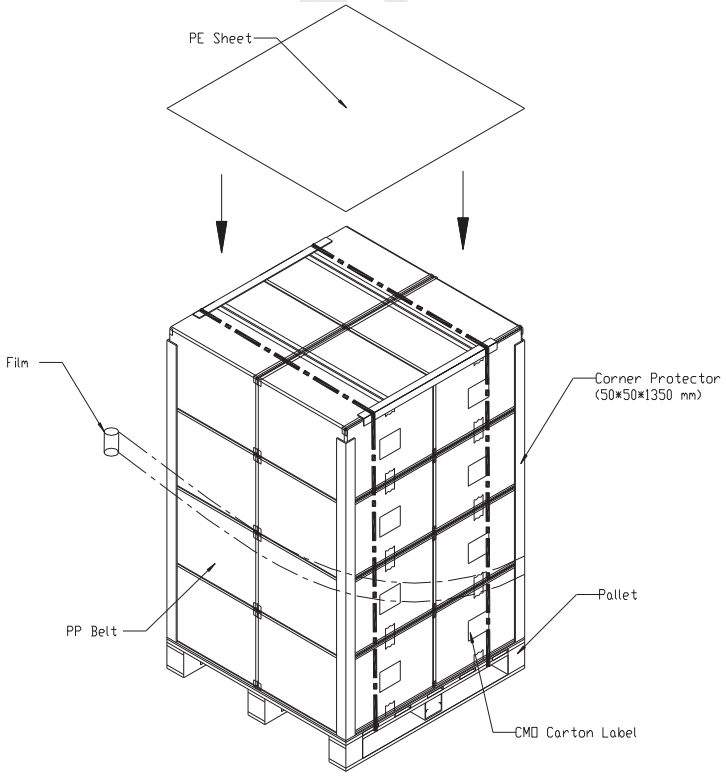
9.1CARTON



Box Dimensions: 511(L)*420(W)*360(H) mm
Weight: Approx. 16.5kg (15 module .per. 1 box)



9.2 PALLET



NOTES:
Pallet:L1050*W870*H135mm
Pallet Stock Dim:L1050*W870*H1585mm
Weight:Approx.287kg

10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N170C3 - L02

(b) Revision: Rev. XX, for example: A1, …, C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D X N N N N

- Serial No.
- CMO Internal Use
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U

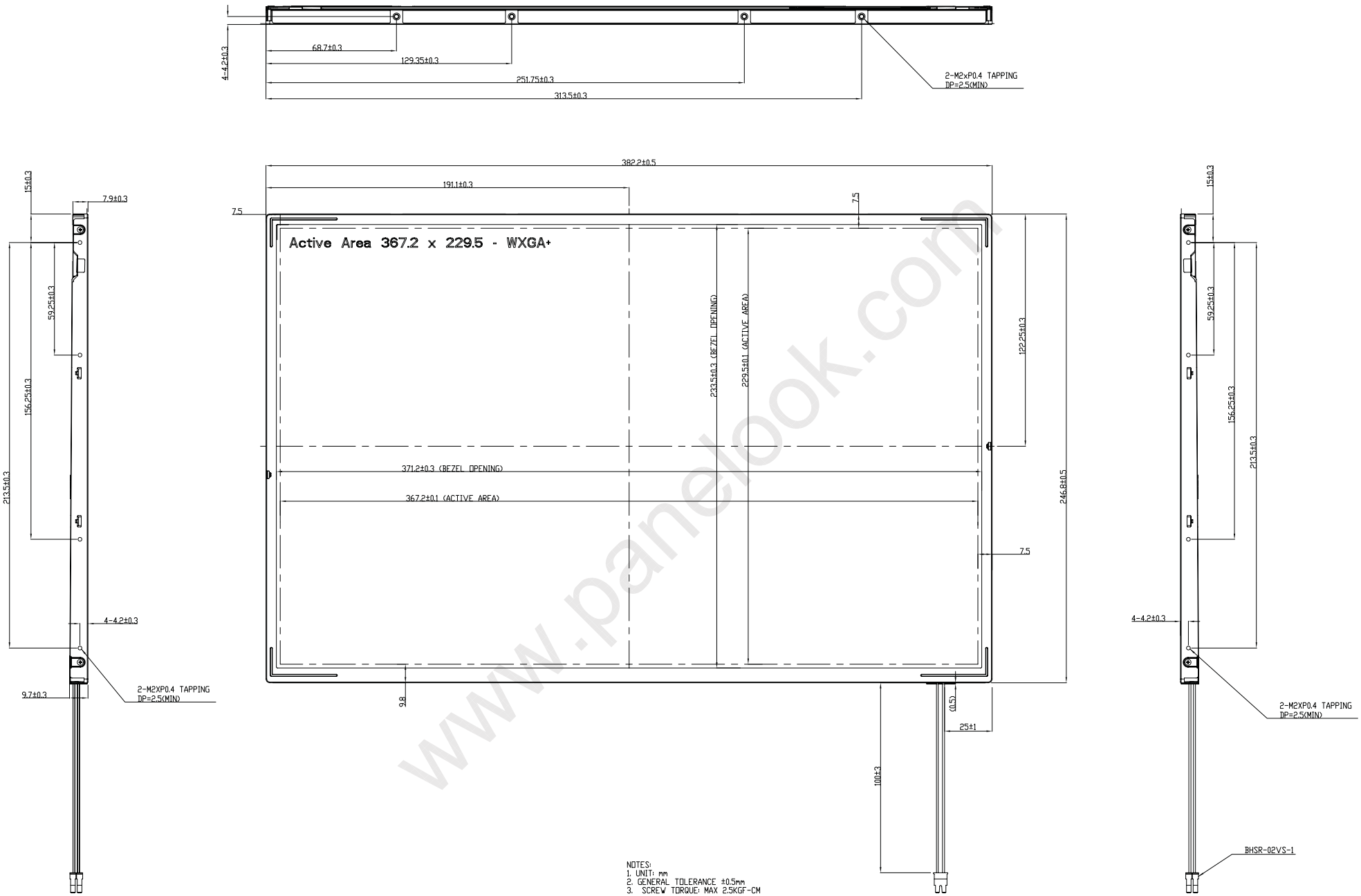
(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Customer's barcode definition:

Serial ID: QLD0525-XXX , XXX follows CMO's product revision, for example: 001, 002…etc.

10.2 CARTON LABEL



NOTES:
1. UNIT: mm
2. GENERAL TOLERANCE ±0.5mm
3. SCREW TORQUE: MAX 2.5KGF-CM

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	OUTLINE DRAWING N170C3-L02				2D REV.	A
					3D REV.	NA
Approved	CLIFF_TSAI	Drawing No.	N17034106A			
Checked	CHINESE_WU	Part No.	NA			
Drawer	FRANK_CHANG	Material	NA	Sheet	1 / 2	A1
Designer	FRANK_CHANG	Date	16-Jul-2007	Scale	1/1	Unit:mm

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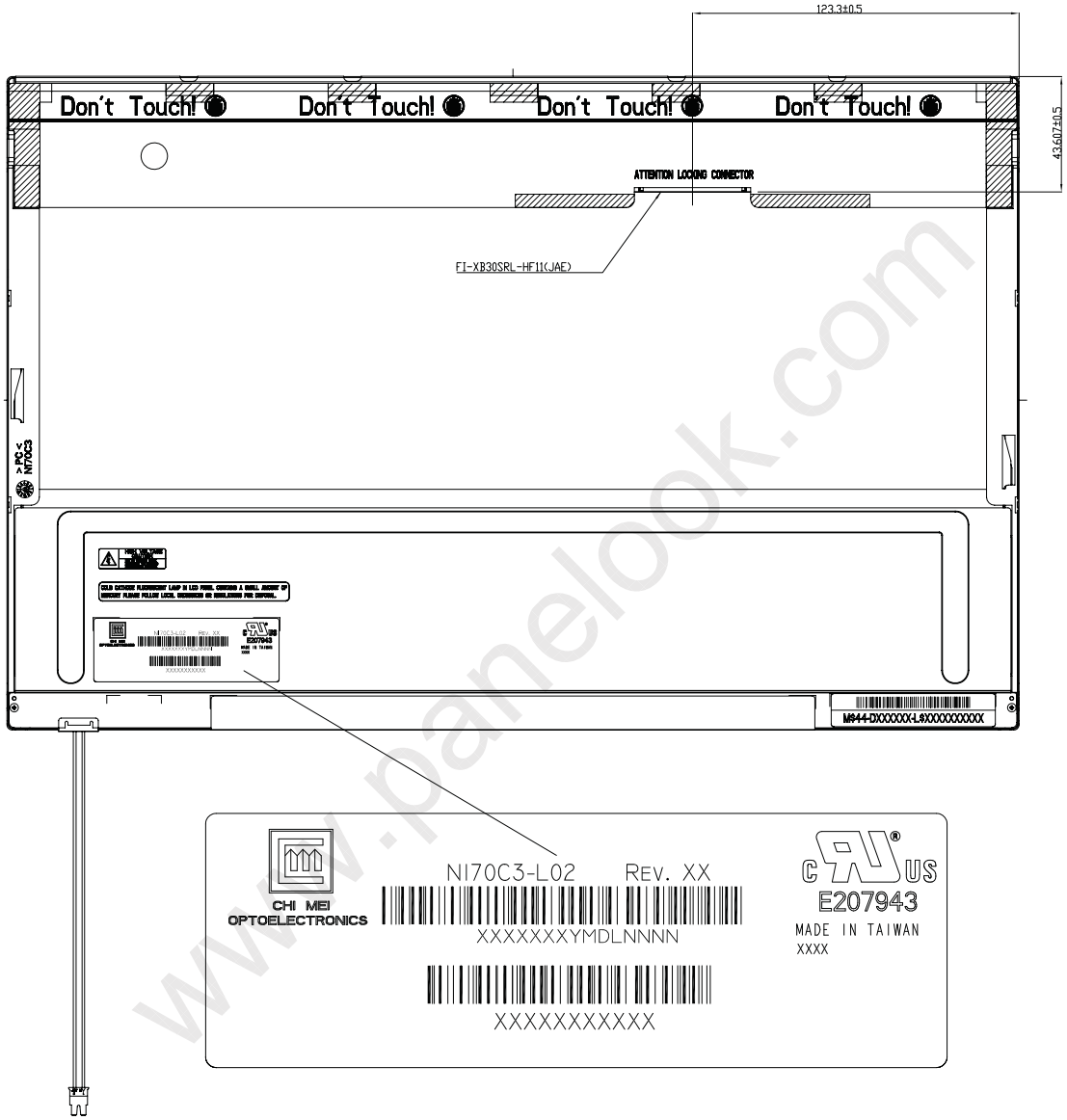

NOTES:
1. UNIT: mm
2. GENERAL TOLERANCE ±0.5mm
3. SCREW TORQUE: MAX 2.5KGF-CM

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	OUTLINE DRAWING N170C3-L02					2D REV.	A
						3D REV.	NA
Approved	CLIFF_TSAI	Drawing No.	N17034106A				
Checked	CHINESE_WU	Part No.	NA				
Drawer	FRANK_CHANG	Material	NA	Sheet	2 / 2	A1	
Designer	FRANK_CHANG	Date	16-Jul-2007	Scale	1/1	Unit	mm

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