



PRELIMINARY

T-46-13-29

## 27C220 2M (128K x 16) CHMOS EPROM

- JEDEC Approved EPROM Pinouts
  - 40-Pin DIP
  - 44-Pin PLCC
- Versatile EPROM Features
  - CMOS and TTL Compatibility
  - Two Line Control
- High-Performance
  - 150 ns  $\pm 10\%$   $V_{CC}$
  - 50 mA  $I_{CC}$  Active
- Fast Programming
  - Quick-Pulse Programming™ Algorithm
  - Programming Times As Fast As 15 Seconds
- Surface Mount Packaging Available
- Complete Upgrade to Higher Densities

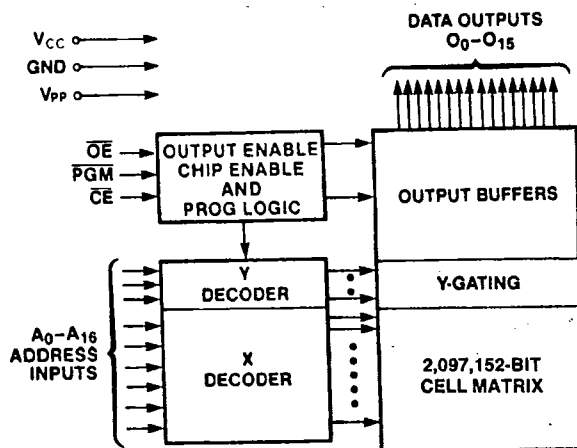
Intel's 27C220 is a 5V only, 2,097,152-bit Erasable Programmable Read Only Memory. Organized as 131,072 words of 16 bits each. It is pin compatible with Intel's 1 Mbit 27C210 and provides for a simple upgrade to 4 Mbits in the future.

The 27C220 represents state-of-the-art 1 micron CMOS manufacturing technology while providing unequalled performance. Its 150 ns speed ( $t_{ACC}$ ) offers no-wait-state operation with high performance CPUs in applications ranging from numerical control to office automation to telecommunications.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic dip (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic dip (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

In addition to the JEDEC 40-pin DIP package, Intel also offers a 44-lead PLCC version of the 27C220. This one-time-programmable surface mount device is ideal where board space consumption is a major concern or where surface mount manufacturing technology is being implemented across an entire production line.

The 27C220 is equally at home in both a TTL or CMOS environment. And like Intel's other high density EPROMs, the 27C220 programs quickly using Intel's industry leading Quick-Pulse Programming algorithm.



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Figure 1. Block Diagram



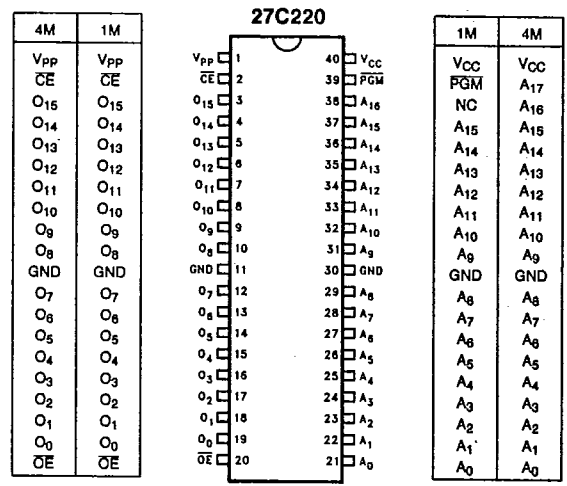
27C220

PRELIMINARY

T-46-13-29

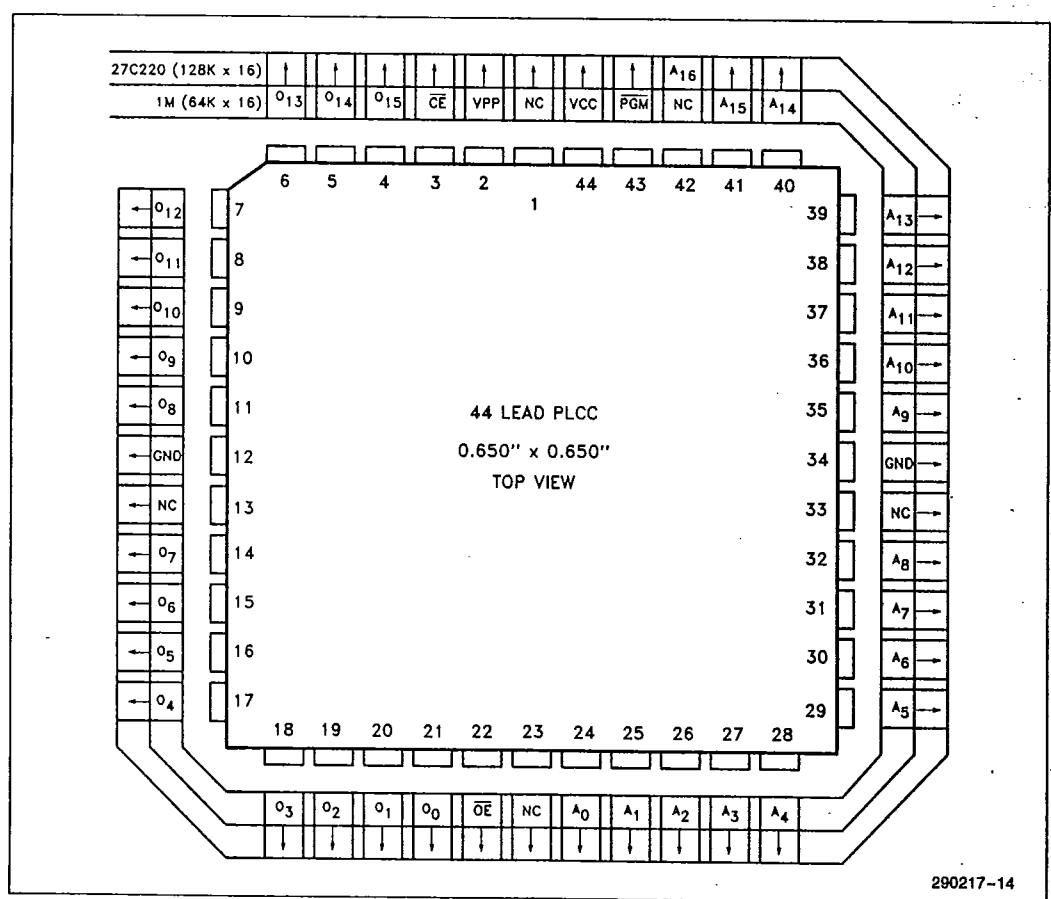
**Pin Names**

A <sub>0</sub> -A <sub>16</sub>	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O <sub>0</sub> -O <sub>15</sub>	OUTPUTS
PGM	PROGRAM
NC	NO INTERNAL CONNECT



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Figure 2. DIP Pin Configurations



290217-14

Figure 3. PLCC Lead Configuration  
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27C220

PRELIMINARY

T-46-13-29

**ABSOLUTE MAXIMUM RATINGS\***

Operating Temperature .....	0°C to 70°C(1)
Temperature Under Bias .....	-10°C to 80°C
Storage Temperature .....	-65°C to 125°C
Voltages on Any Pin (except A <sub>g</sub> , V <sub>CC</sub> and V <sub>PP</sub> ) with Respect to GND .....	-0.6V to 6.5V(2)
Voltage on A <sub>g</sub> with Respect to GND .....	-0.6V to 13.0V(2)
V <sub>PP</sub> Supply Voltage with Respect to GND .....	-0.6V to 14V(2)
V <sub>CC</sub> Supply Voltage with Respect to GND .....	-0.6V to 7.0V(2)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

**READ OPERATION DC CHARACTERISTICS** V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I <sub>LI</sub>	Input Load Current	7		0.01	1.0	μA	V <sub>IN</sub> = 0V to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current				± 10	μA	V <sub>OUT</sub> = 0V to V <sub>CC</sub>
I <sub>SB</sub>	V <sub>CC</sub> Standby Current				1.0	mA	$\overline{CE} = V_{IH}$
					100	μA	$\overline{CE} = V_{CC} \pm 0.2V$
I <sub>CC</sub>	V <sub>CC</sub> Operating Current	3			50	mA	$\overline{CE} = V_{IL}$ f = 5 MHz, I <sub>OUT</sub> = 0 mA
I <sub>PP</sub>	V <sub>PP</sub> Operating Current	3			10	μA	V <sub>PP</sub> = V <sub>CC</sub>
I <sub>OS</sub>	Output Short Circuit Current	4, 6			100	mA	
V <sub>IL</sub>	Input Low Voltage		-0.5		0.8	V	
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage				0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage		2.4			V	I <sub>OH</sub> = -400 μA
V <sub>PP</sub>	V <sub>PP</sub> Operating Voltage	5	V <sub>CC</sub> - 0.7		V <sub>CC</sub>	V	

**NOTES:**

- Operating temperature is for commercial product defined by this specification.
- Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V<sub>CC</sub> + 0.5V which, during transitions, may overshoot to V<sub>CC</sub> + 2.0V for periods < 20 ns.
- Maximum active power usage is the sum I<sub>PP</sub> + I<sub>CC</sub>. Maximum current is with outputs O<sub>0</sub> to O<sub>15</sub> unloaded.
- Output shorted for no more than one second. No more than one output shorted at a time.
- V<sub>PP</sub> may be connected directly to V<sub>CC</sub>, or may be one diode voltage drop below V<sub>CC</sub>. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.
- Sampled, not 100% tested.
- Typical limits are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

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27C220

PRELIMINARY

T-46-13-29

READ OPERATION AC CHARACTERISTICS(1)  $V_{CC} = 5.0V \pm 10\%$ 

Versions(4)		$V_{CC} \pm 10\%$	27C220-150V10		27C220-200V10 P27C220-200V10 N27C220-200V10		Units
Symbol	Parameter	Notes	Min	Max	Min	Max	
$t_{ACC}$	Address to Output Delay			150		200	ns
$t_{CE}$	$\overline{CE}$ to Output Delay	2		150		200	ns
$t_{OE}$	$\overline{OE}$ to Output Delay	2		60		70	ns
$t_{DF}$	$\overline{OE}$ High to Output High Z	3		50		60	ns
$t_{OH}$	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		ns

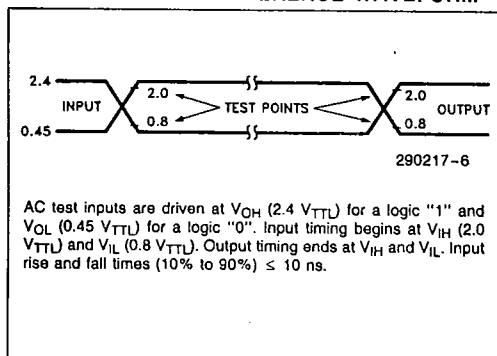
## NOTES:

- See AC Input/Output Reference Waveform for timing measurements.
- $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
- Sampled, not 100% tested.
- Model Number Prefixes: No Prefix = CERDIP, P = PDIP, N = PLCC.
- Typical limits are for  $T_A = 25^\circ C$  and nominal supply voltages.

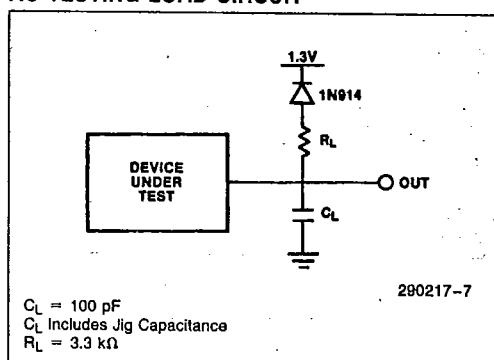
CAPACITANCE(3)  $T_A = 25^\circ C, f = 1MHz$ 

Symbol	Parameter	Typ(5)	Max	Unit	Conditions
$C_{IN}$	Input Capacitance	4	8	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{VPP}$	$V_{PP}$ Capacitance	18	25	pF	$V_{PP} = 0V$

## AC INPUT/OUTPUT REFERENCE WAVEFORM



## AC TESTING LOAD CIRCUIT



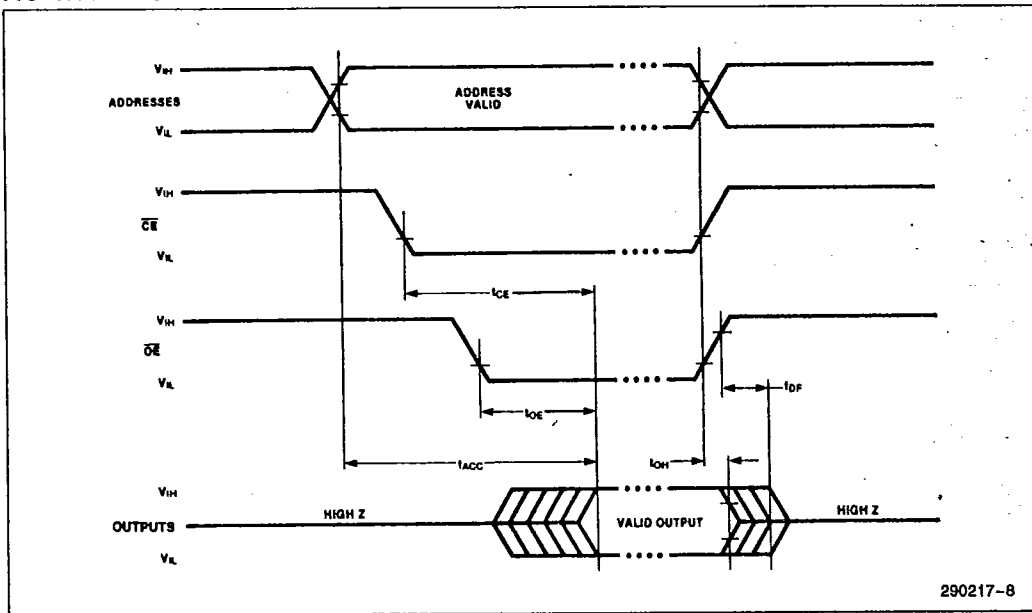
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27C220

PRELIMINARY

T-46-13-29

## AC WAVEFORMS



## DEVICE OPERATION

The Mode Selection table lists 27C220 operating modes. Read Mode requires a single 5V power supply. All inputs, except  $V_{CC}$  and  $V_{PP}$ , and  $A_9$  during intelligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode	Notes	CE	OE	PGM	$A_9$	$A_0$	$V_{PP}$	$V_{CC}$	Outputs	
Read	1	$V_{IL}$	$V_{IL}$	X(1)	X	X	$V_{CC}$	$V_{CC}$	$D_{OUT}$	
Output Disable		$V_{IL}$	$V_{IH}$	X	X	X	$V_{CC}$	$V_{CC}$	High Z	
Standby		$V_{IH}$	X	X	X	X	$V_{CC}$	$V_{CC}$	High Z	
Program	2	$V_{IL}$	$V_{IH}$	$V_{IL}$	X	X	$V_{PP}$	$V_{CP}$	$D_{IN}$	
Program Verify		$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	$V_{CP}$	$D_{OUT}$	
Program Inhibit		$V_{IH}$	X	X	X	X	$V_{PP}$	$V_{CP}$	High Z	
intelligent Identifier	Manufacturer	2, 3	$V_{IL}$	$V_{IL}$	X	$V_{ID}$	$V_{IL}$	$V_{CC}$	$V_{CC}$	0089 H.
	Device		$V_{IL}$	$V_{IL}$	X	$V_{ID}$	$V_{IH}$	$V_{CC}$	$V_{CC}$	22EEH

## NOTES:

- X can be  $V_{IL}$  or  $V_{IH}$
- See DC Programming Characteristics for  $V_{CP}$ ,  $V_{PP}$  and  $V_{ID}$  voltages.
- $A_1-A_8$ ,  $A_{10}-A_{18} = V_{IL}$

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27C220

PRELIMINARY

T-46-13-29

## Read Mode

The 27C220 has two control functions; both must be enabled to obtain data at the outputs.  $\overline{CE}$  is the power control and device select.  $\overline{OE}$  controls the output buffers to gate data to the outputs. With addresses stable, the address access time ( $t_{ACC}$ ) equals the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Outputs display valid data  $t_{OE}$  after  $\overline{OE}$ 's falling edge, assuming  $t_{ACC}$  and  $t_{CE}$  times are met.

$V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

## Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

- lowest possible memory power dissipation
- complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable  $\overline{CE}$ , while  $\overline{OE}$  should be connected to all memory devices and the system's  $\overline{READ}$  control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

## Standby Mode

Standby Mode substantially reduces  $V_{CC}$  current. When  $\overline{CE} = V_{IH}$ , the outputs are in a high impedance state, independent of  $\overline{OE}$ .

## Program Mode

**Caution: Exceeding 14V on  $V_{PP}$  will permanently damage the device.**

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when  $V_{PP}$  is raised to 12.75V. Data is introduced by applying a 16-bit word to the output pins. Pulsing  $\overline{PGM}$  low while  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IH}$  programs that data into the device.

## Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With  $V_{CC}$  at 6.25V, a substantial pro-

gram margin is ensured. The verify is performed with  $\overline{CE}$  at  $V_{IL}$  and  $\overline{PGM}$  at  $V_{IH}$ . Valid data is available  $t_{OE}$  after  $\overline{OE}$  falls low.

## Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data.  $\overline{CE}$ -high inhibits programming of non-targeted devices. Except for  $\overline{CE}$ , parallel EPROMs may have common inputs.

## Intelligent Identifier™ Mode

The Intelligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces  $12V \pm 0.5V$  on  $A_9$ . With  $\overline{CE}$ ,  $\overline{OE}$ ,  $A_1$ - $A_8$ , and  $A_{10}$ - $A_{16}$  at  $V_{IL}$ ,  $A_0 = V_{IL}$  will present the manufacturer code and  $A_0 = V_{IH}$  the device code. This mode functions in the  $25^\circ C \pm 5^\circ C$  ambient temperature range required during programming.

## UPGRADE PATH

Future upgrade to the 4-Mbit density is easily accomplished due to the standardized pin configuration of the 27C220. When the 27C220 is in Read Mode, the  $\overline{PGM}$  input becomes non-functional. This allows address line  $A_{17}$  to be routed directly to this input in anticipation of future density upgrades. Systems designed for 2-Mbit program memories today can be upgraded to 4-Mbit in the future with no circuit board changes.



## SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels ( $I_{SB}$ ), active current levels ( $I_{CC}$ ), and transient current peaks produced by falling and rising edges of  $\overline{CE}$ . Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu F$  ceramic capacitor connected between its  $V_{CC}$  and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7  $\mu F$  electrolytic capacitor should be placed at the array's power supply connection between  $V_{CC}$  and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

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27C220

PRELIMINARY

T-46-13-29

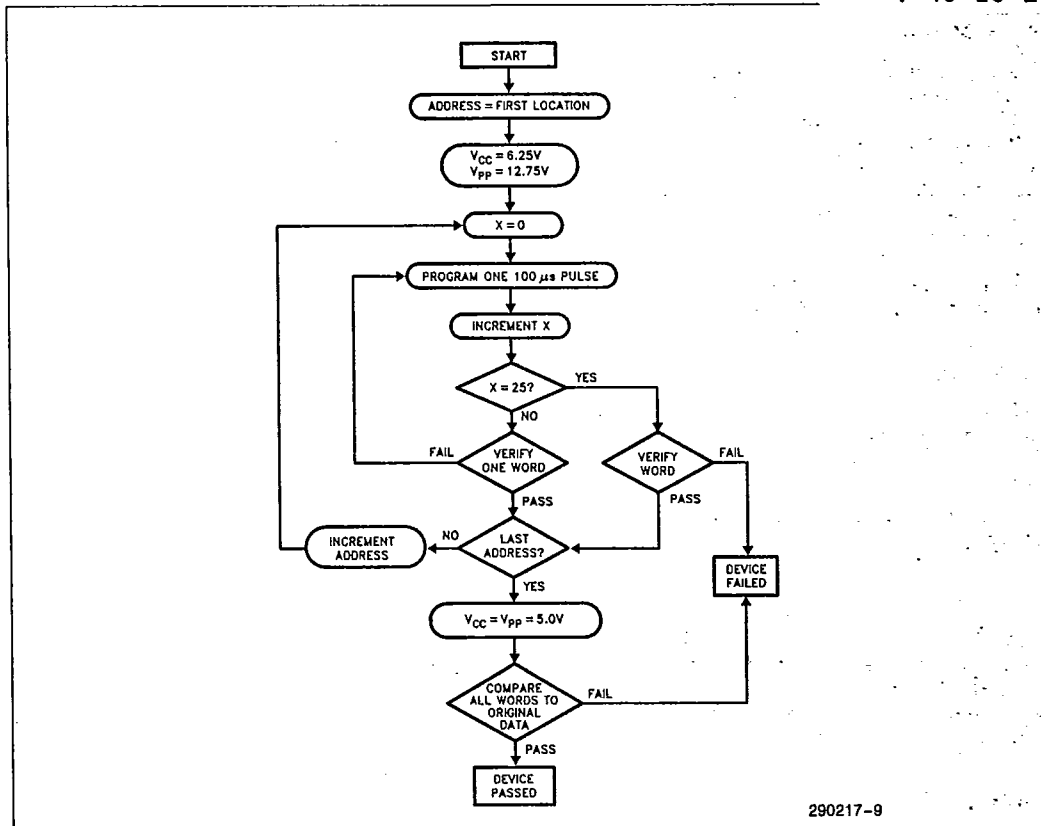


Figure 4. Quick-Pulse Programming™ Algorithm

## ERASURE CHARACTERISTICS

Erase begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm<sup>2</sup>. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm<sup>2</sup> power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently dam-

aged if the integrated dose exceeds 7258 Wsec/cm<sup>2</sup> (1 week @ 12000 μW/cm<sup>2</sup>).

## Quick-Pulse Programming™ Algorithm

The Quick-Pulse programming algorithm programs Intel's 27C220. Developed to substantially reduce programming throughput, this algorithm can program the 27C220 as fast as 15 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse programming algorithm employs a 100 μs pulse followed by a word verification to determine when the addressed word has been successfully programmed. The algorithm terminates if 25 attempts fail to program a word.

The entire program pulse/word verify sequence is performed with V<sub>pp</sub> = 12.75V and V<sub>CC</sub> = 6.25V. When programming is complete, all words are compared to the original data with V<sub>CC</sub> = V<sub>pp</sub> = 5.0V.

T-46-13-29

DC PROGRAMMING CHARACTERISTICS  $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ 

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
$I_{LI}$	Input Load Current				1	$\mu\text{A}$	$V_{IN} = V_{IL}$ or $V_{IH}$
$I_{CP}$	$V_{CC}$ Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
$I_{PP}$	$V_{PP}$ Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
$V_{IL}$	Input Low Voltage		-0.1		0.8	V	
$V_{IH}$	Input High Voltage		2.4		6.5	V	
$V_{OL}$	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1 \text{ mA}$
$V_{OH}$	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5 \text{ mA}$
$V_{ID}$	$A_g$ intelligent Identifier Voltage		11.5	12.0	12.5	V	
$V_{PP}$	$V_{PP}$ Program Voltage	2, 3	12.5	12.75	13.0	V	
$V_{CP}$	$V_{CC}$ Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4)  $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ 

Symbol	Parameter	Notes	Min	Typ	Max	Unit
$t_{VCS}$	$V_{CP}$ Setup Time	2	2			$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ Setup Time	2	2			$\mu\text{s}$
$t_{CES}$	$\overline{CE}$ Setup Time		2			$\mu\text{s}$
$t_{AS}$	Address Setup Time		2			$\mu\text{s}$
$t_{DS}$	Data Setup Time		2			$\mu\text{s}$
$t_{PW}$	$\overline{PGM}$ Program Pulse Width		95	100	105	$\mu\text{s}$
$t_{DH}$	Data Hold Time		2			$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ Setup Time		2			$\mu\text{s}$
$t_{OE}$	Data Valid from $\overline{OE}$	5			150	ns
$t_{DFP}$	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
$t_{AH}$	Address Hold Time		0			$\mu\text{s}$

## NOTES:

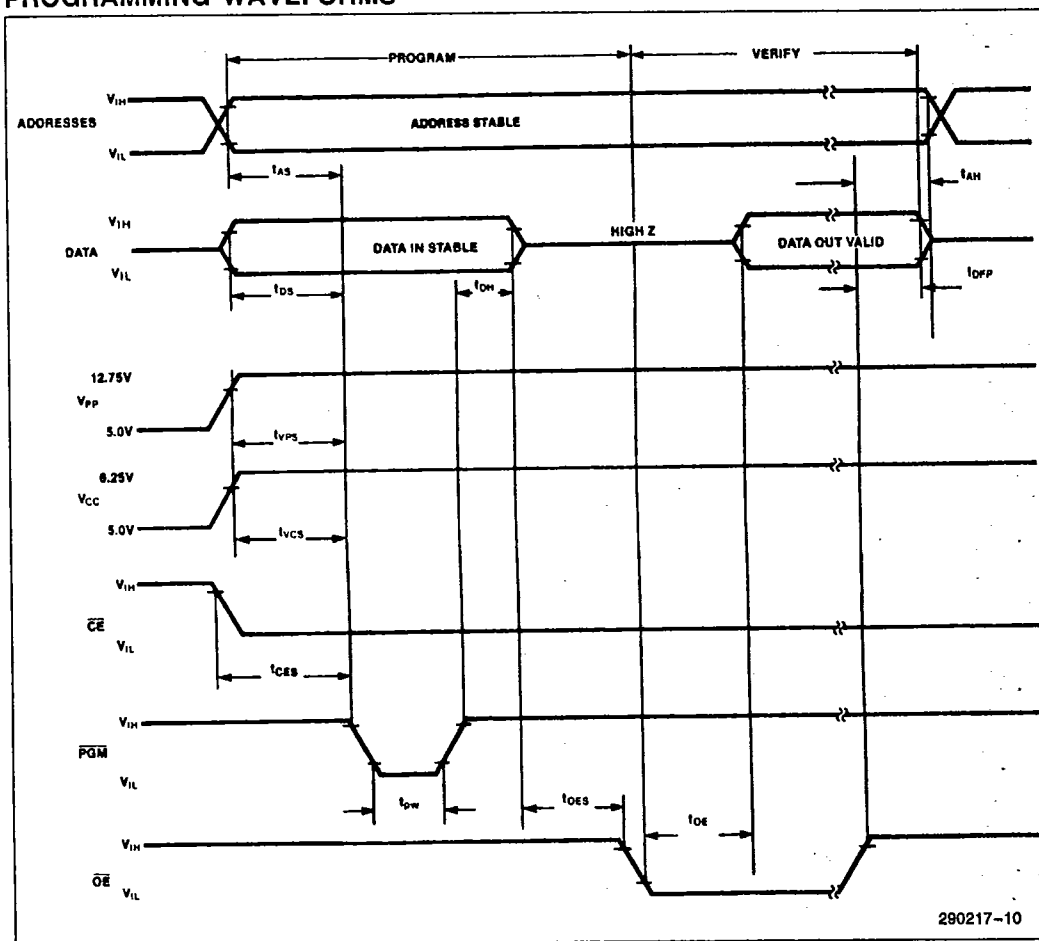
- Maximum current is with outputs  $O_0$ - $O_{15}$  unloaded.
- $V_{CP}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- When programming, a 0.1  $\mu\text{F}$  capacitor is required across  $V_{PP}$  and GND to suppress spurious voltage transients which can damage the device.
- See AC Input/Output Reference Waveform for timing measurements.
- $t_{OE}$  and  $t_{DFP}$  are device characteristics but must be accommodated by the programmer.
- Sampled, not 100% tested.





T-46-13-29

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
005	Deleted -150 PDIP, PLCC packages