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N32T1630C1C

32Mb Ultra-Low Power Asynchronous CMOS Pseudo SRAM

w/ Page Mode Operation (2M x 16 bit)

Overview

The N32T1630C1C is an integrated memory device containing a 32 Mbit SRAM built using a self-refresh DRAM array organized as 2,097,152 words by 16 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide both high-speed performance and ultra-low power. It is designed to be identical in operation and interface to standard 6T SRAMS. Byte controls ($\overline{UB}$ and $\overline{LB}$) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The N32T1630C1C offers a very high speed page mode operation for improved performance and operating power savings. The device is optimal for various applications where low-power is critical such as battery backup and hand-held devices. Also included are several power savings modes: a deep sleep mode and partial array refresh mode where data is retained in a portion of the array. The device can operate over a very wide temperature range of -25°C to +85°C and is available in a JEDEC standard VFRBGA package compatible with other standard 2Mb x 16 SRAMs.

Features

- **Dual voltage for Optimum Performance:**
  VccQ - 2.7 to 3.6 Volts
  Vcc - 2.7 to 3.6 Volts (Vcc ≤ VccQ)
- **Fast random access time**
  70ns at 2.7V
- **Very fast page mode access time**
  25ns page cycle and access
- **Very low standby current**
  80µA V (Typical)
- **Very low operating current**
  1.0mA at 1µs (Typical)
- **Simple memory control**
  Byte control for independent byte operation
  Output Enable ($\overline{OE}$) for memory expansion
- **Automatic power down to standby mode**
- **PAR and RMS power saving modes**
- **Deep sleep option**
- **TTL compatible three-state output driver**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply	Speed	Standby Current (I_{SB}), Max	Operating Current (Icc), Max
N32T1630C1CZ	48-VFRBGA	-25°C to +85°C	2.7V - 3.6V (V_{CC})	70ns	135 µA @ 3.3V	3 mA @ 1MHz

Pin Configuration (Top View)

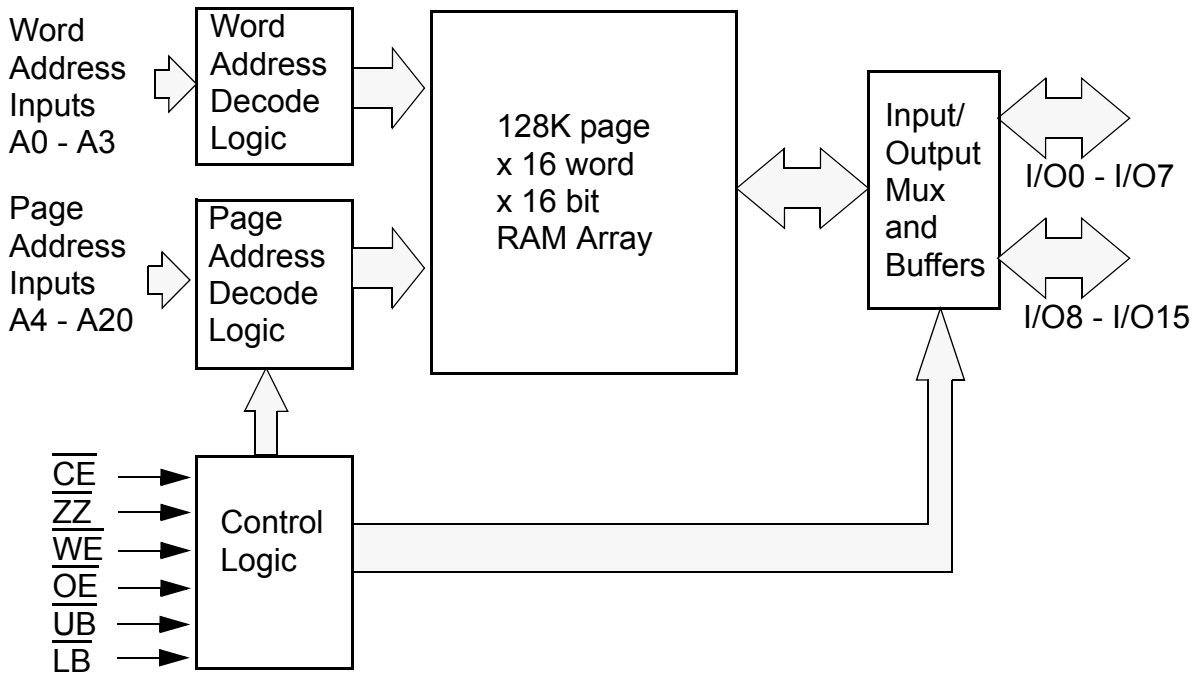
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	$\overline{ZZ}$
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SSQ}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CCQ}	I/O_{12}	DNU/ VSS	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{20}

48 Ball VFRBGA
6 x 8 mm

Pin Descriptions

Pin Name	Pin Function
A_0-A_{20}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{UB}$,$\overline{LB}$	Byte Enable Inputs
$\overline{ZZ}$	Deep Sleep Input
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	Core Power
V_{CCQ}	I/O Power
V_{SS}	Ground
V_{SSQ}	I/O Ground
DNU	Do Not Use

Functional Block Diagram



Functional Description

$\overline{CE}$	$\overline{ZZ}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O_0 - I/O_{15}[1]	MODE	POWER
H	H	X	X	X	X	High Z	Standby[2]	Standby
X	H	X	X	H	H	High Z	Standby[2]	Standby
L	H	L	X[3]	L[1]	L[1]	Data In	Write	Active
L	H	H	L	L[1]	L[1]	Data Out	Read	Active
L	H	H	H	L	L	High Z	Active	Active
X	L	X	X	X	X	High Z	Deep Sleep	Deep Sleep

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - I/O_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown.

2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		6	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.2 to V_{CCQ}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.2 to 4.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–55 to 125	°C
Operating Temperature	T_A	-25 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	240°C, 10sec(Lead Only)	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min.	Typ[1]	Max	Unit
Supply Voltage	V_{CC}		2.7	3.0	3.6	V
Supply Voltage for I/O	V_{CCQ}	$V_{CC} = V_{CCQ}$ (Note 4)	2.7	3.0	3.6	V
Input High Voltage	V_{IH}		$0.8V_{CCQ}$		V_{CCQ}+0.2	V
Input Low Voltage	V_{IL}		–0.2		0.4	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	0.8VccQ			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA			0.2	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled			0.5	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}= 3.3V, V_{IN}=CMOS levels-Chip Enabled, I_{OUT} = 0			3.0	mA
Read/Write Operating Supply Current @ 70 ns Cycle Time[2]	I_{CC2}	V_{CC}= 3.3V, V_{IN}=CMOS levels Chip Enabled, I_{OUT} = 0			25.0	mA
Maximum Standby Current[3]	I_{SB1}	V_{CC}= 3.3V, V_{IN}=CMOS levels Chip Disabled		80	135.0	µA

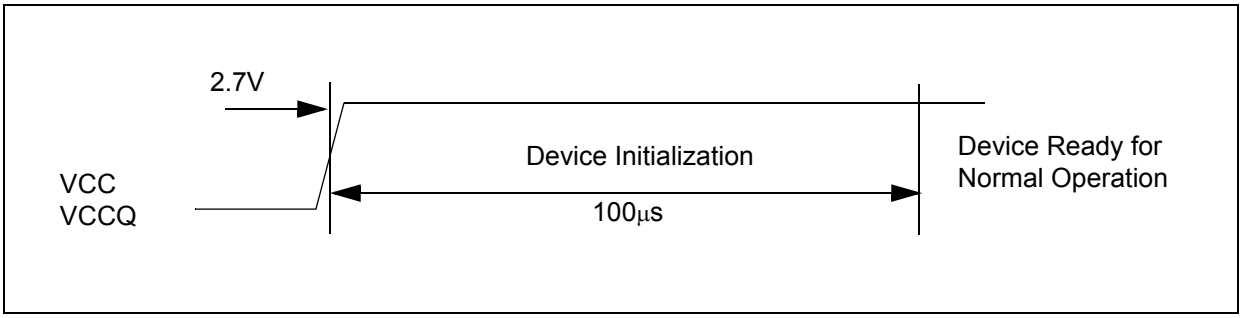
1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. This device assumes a standby mode if the chip is disabled (either $\overline{CE}$ high or both $\overline{UB}$ and $\overline{LB}$ high). In order to achieve low standby current all inputs must be within 0.2V of either VCC or VSS

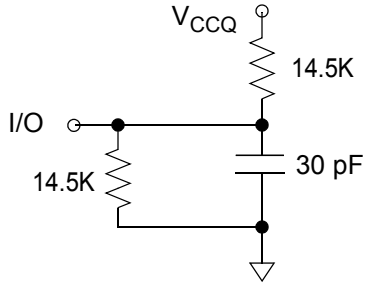
4. During testing, Vcc = VccQ.

Power Up Initialization Timing



The device will require 100 μs to complete its self-initialization process. During the initialization period, CE# pin should remain HIGH.

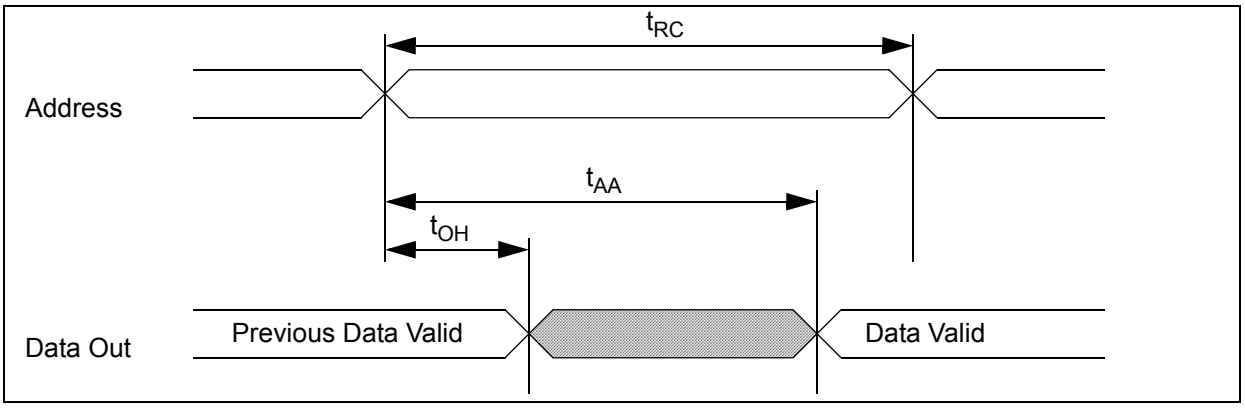
FIGURE 1: Output Load Circuit



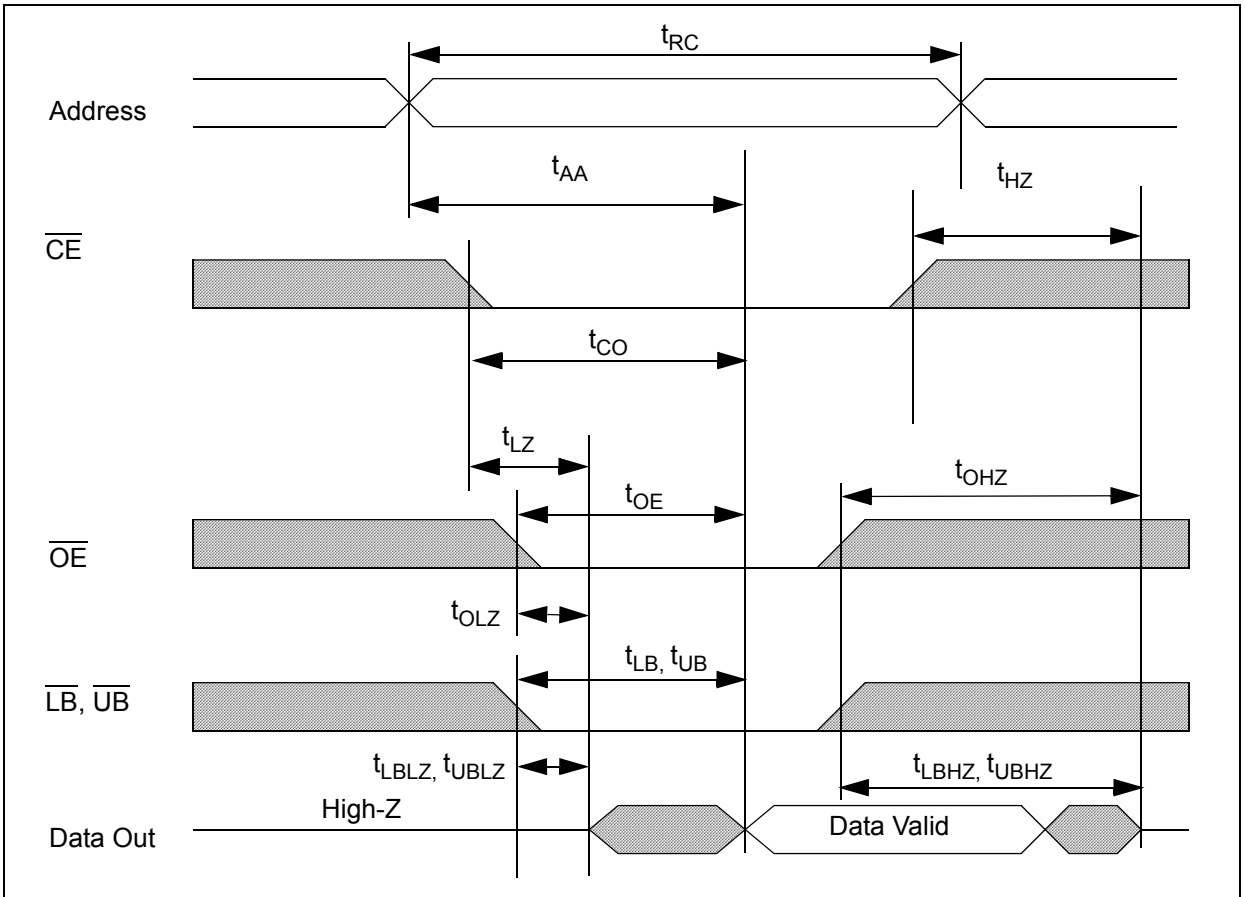
Timing

Item	Symbol	70ns		Units
		Min.	Max.	
Read Cycle Time	t_{RC}	70		ns
Address Access Time	t_{AA}		70	ns
Page Mode Read Cycle Time	t_{PC}	25	20000	ns
Page Mode Access Time	t_{PA}		25	ns
Chip Enable to Valid Output	t_{CO}		70	ns
Output Enable to Valid Output	t_{OE}		20	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		70	ns
Chip Enable to Low-Z output	t_{LZ}	10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	0	20	ns
Output Hold from Address Change	t_{OH}	5		ns
Write Cycle Time	t_{WC}	70		ns
Page Mode Write Cycle Time	t_{PWC}	25	20000	ns
Chip Enable to End of Write	t_{CW}	60		ns
Address Valid to End of Write	t_{AW}	60		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	60		ns
Write Pulse Width	t_{WP}	55	20000	ns
Address Setup Time	t_{AS}	0		ns
Write Recovery Time	t_{WR}	0		ns
Write to High-Z Output	t_{WHZ}		20	ns
Data to Write Time Overlap	t_{DW}	25		ns
Page Mode Data to Write Time Overlap	t_{PDW}	20		ns
Data Hold from Write Time	t_{DH}	0		ns
Page Mode Data Hold from Write Time	t_{PDH}	0		ns
End Write to Low-Z Output	t_{OW}	5		ns
CE Precharge	t_{CP}	10		ns
Maximum Page Mode Cycle	t_{PGMAX}		20000	ns

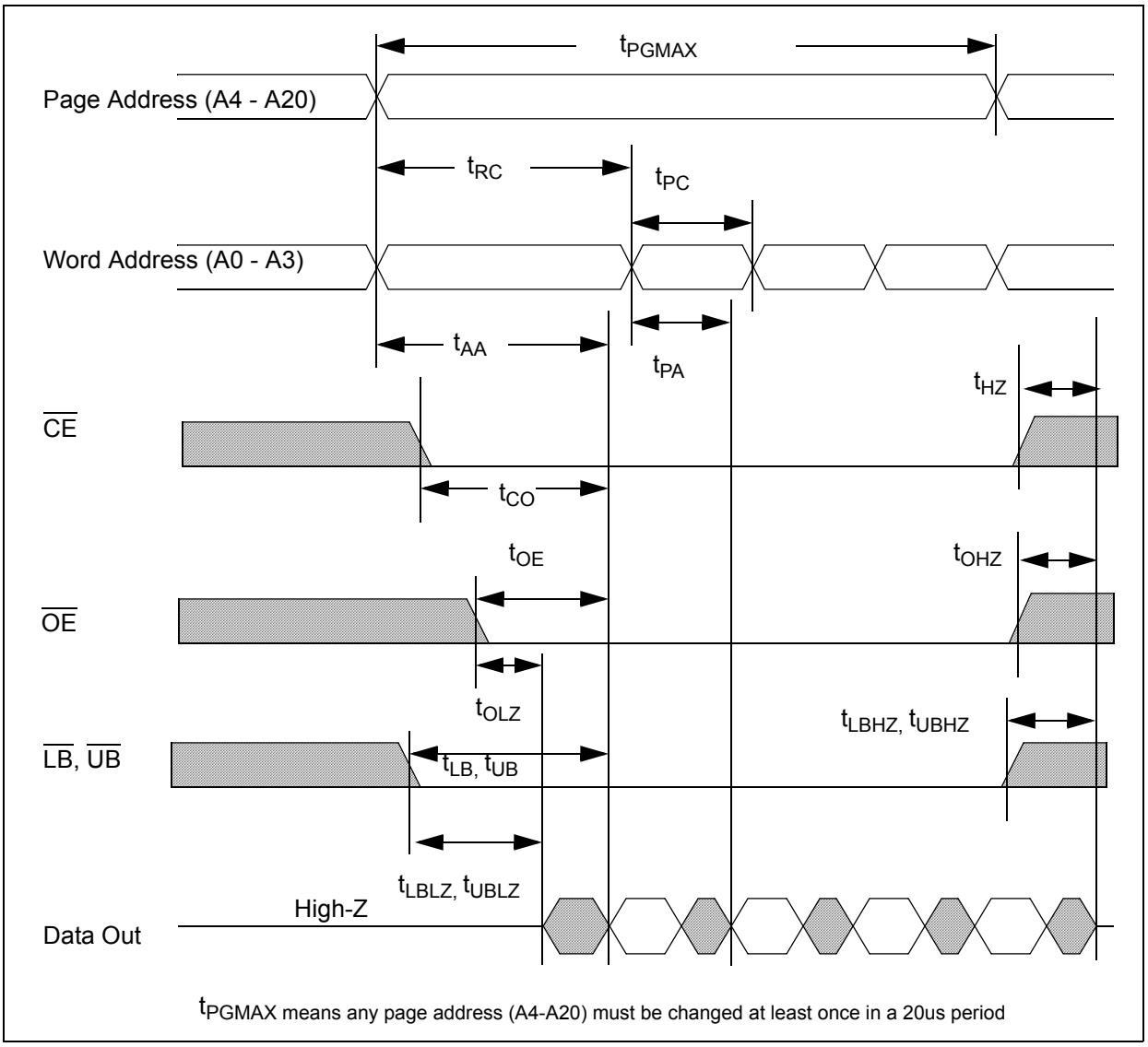
Timing of Read Cycle ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})

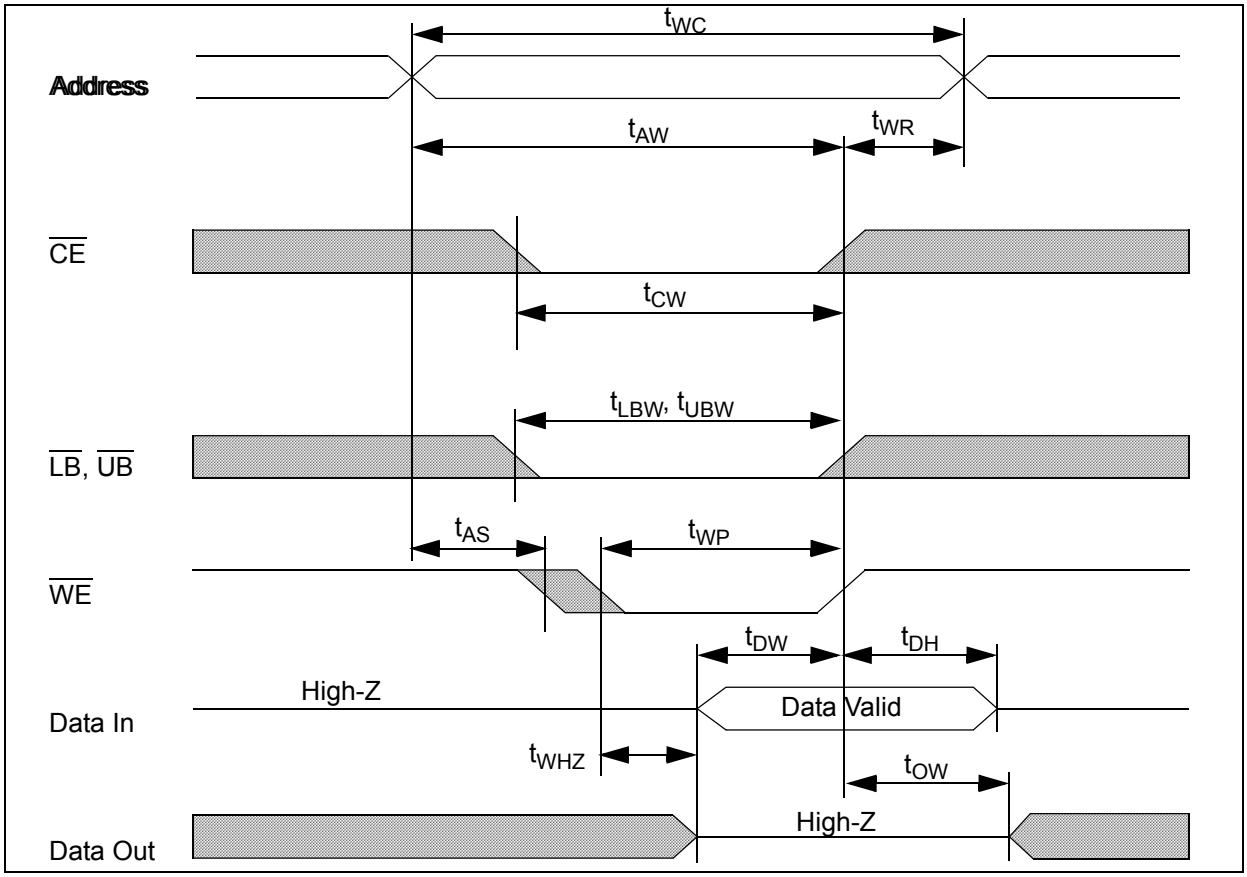


Timing Waveform of Page Mode Read Cycle ($\overline{WE}$ = V_{IH})

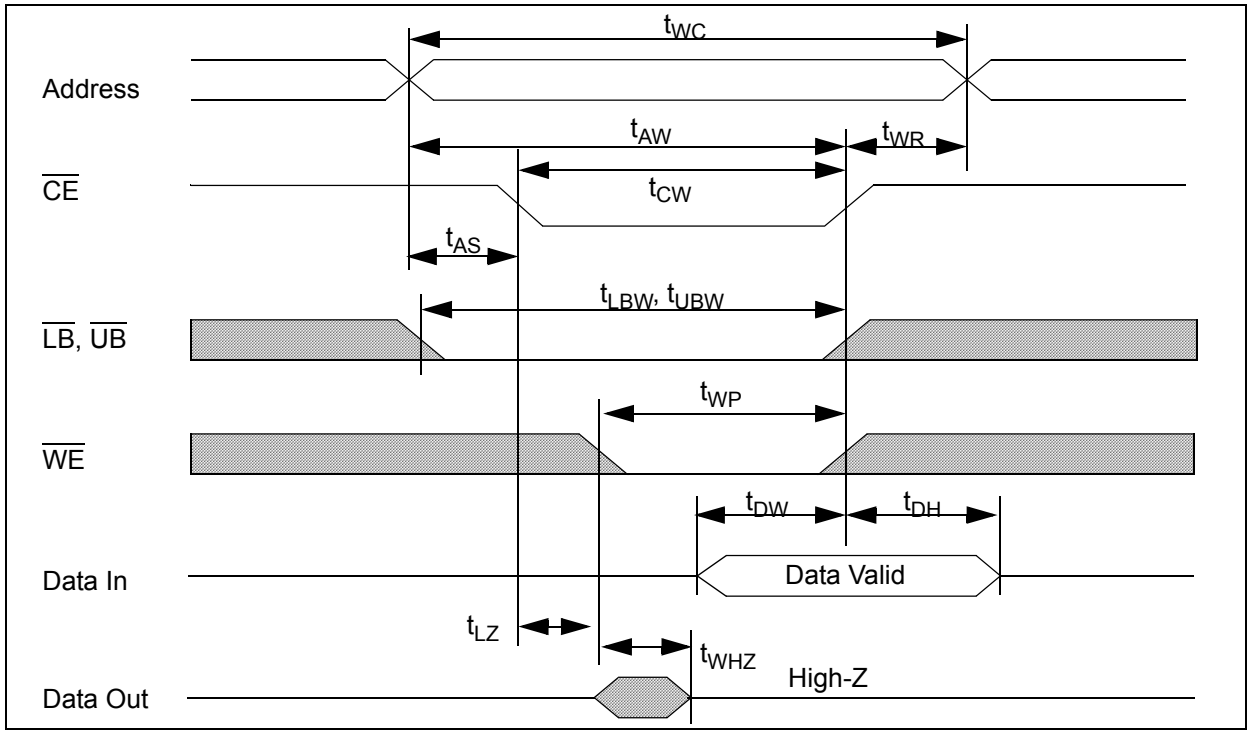


t_{PGMAX} means any page address (A4-A20) must be changed at least once in a 20us period

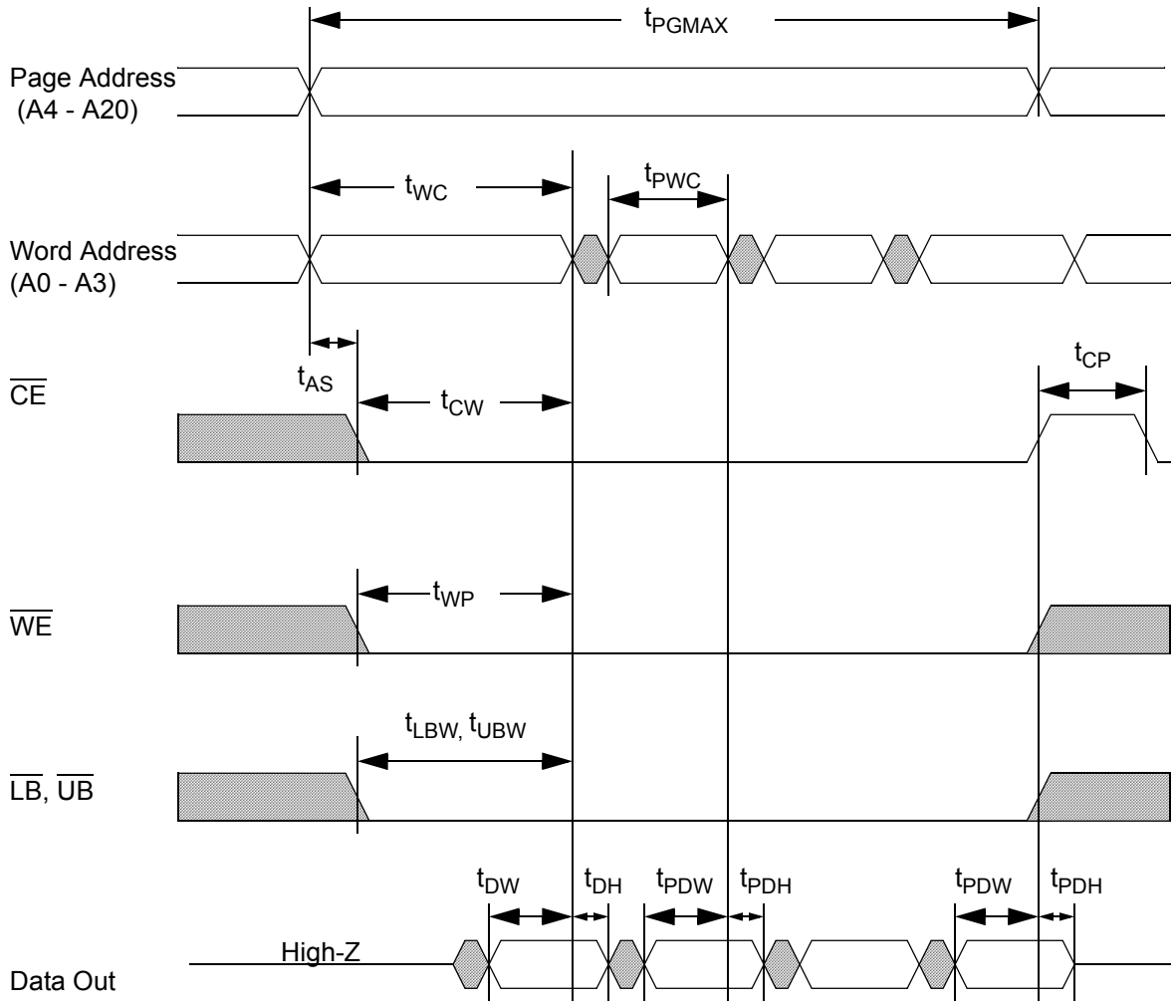
Timing Waveform of Write Cycle ($\overline{WE}$ Control)



Timing Waveform of Write Cycle ($\overline{CE}$ Control)



Timing Waveform of Page Mode Write Cycle



t_{PGMAX} means any page address (A4-A20) must be changed at least once in a 20us period

Power Savings Modes

The N32T1630C1C has several power savings modes and the three modes are:
Reduced Memory Size
Partial Array Refresh
Deep Sleep Mode

The operation of the power saving modes is controlled by setting the Variable Address Register (VAR). This VAR is shown in Figure 8 and is used to enable/disable the various low power modes.
The VAR is set by using the timings defined in figure 9. The register must be set in less then 1us after $\overline{ZZ}$ is enabled low.

1) Reduced Memory Size (RMS)

In this mode of operation, the 32Mb PSRAM can be operated as a 8Mb or 16Mb device. The mode and array size are determined by the settings in the VA register. The VA register is set according to the timings of Figure 9 and the bit setting of Table 12. The RMS mode is enabled at the time of ZZ transitioning high and the mode remains active until the register is updated. To return to the full 32Mb address space, the VA register must be reset using the previously defined procedures.

2) Partial Array Refresh (PAR)

In this mode of operation, the internal refresh operation can be restricted to a 8Mb or 16Mb portion of the array. The mode and array partition to be refreshed are determined by the settings in the VAR register. The VAR register is set according to the timings of Figure 9 and the bit settings of Table 11. In this mode, when $\overline{ZZ}$ is taken low, only the portion of the array that is set in the register is refreshed. The operating mode is only available during standby time and once $\overline{ZZ}$ is returned high, the device resumes full array refresh. All future PAR cycles will use the contents of the VA register. To change the address space of the PAR mode, the VA register must be reset using the previously defined procedures.

There are two different device versions that have different default settings for the PAR mode.

In the first version, the default state for the $\overline{ZZ}$ enable/disable register will be $\overline{ZZ}$ enabled where $\overline{ZZ}$ low will initiate a deep sleep mode after 1us. This device is referred to as Deep Sleep Active, or DSA device. In the second version, the default state for the $\overline{ZZ}$ register will be such that $\overline{ZZ}$ low will put the device into PAR mode after 1us and never initiate a deep sleep mode unless appropriate register is updated. This device is referred to as Deep Sleep Inactive, or DSI device. In either device, once the SRAM enters Deep Sleep Mode, the VAR contents are destroyed and the default register settings are reset.

3) Deep Sleep Mode

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing $\overline{ZZ}$ low. After 1 us, if the VAR register corresponding to A4 is not set to Deep Sleep Disabled, the device will enter Deep Sleep Mode. The device will remain in this mode as long as $\overline{ZZ}$ remains low.

FIGURE 2: Variable Address Register

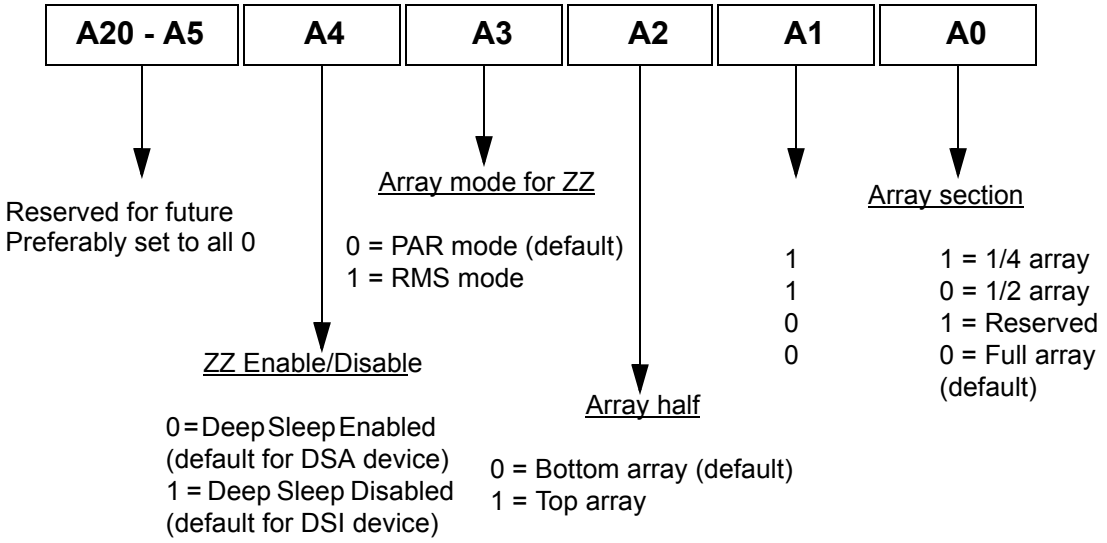


FIGURE 3: Variable Address Register (VAR) Update Timings

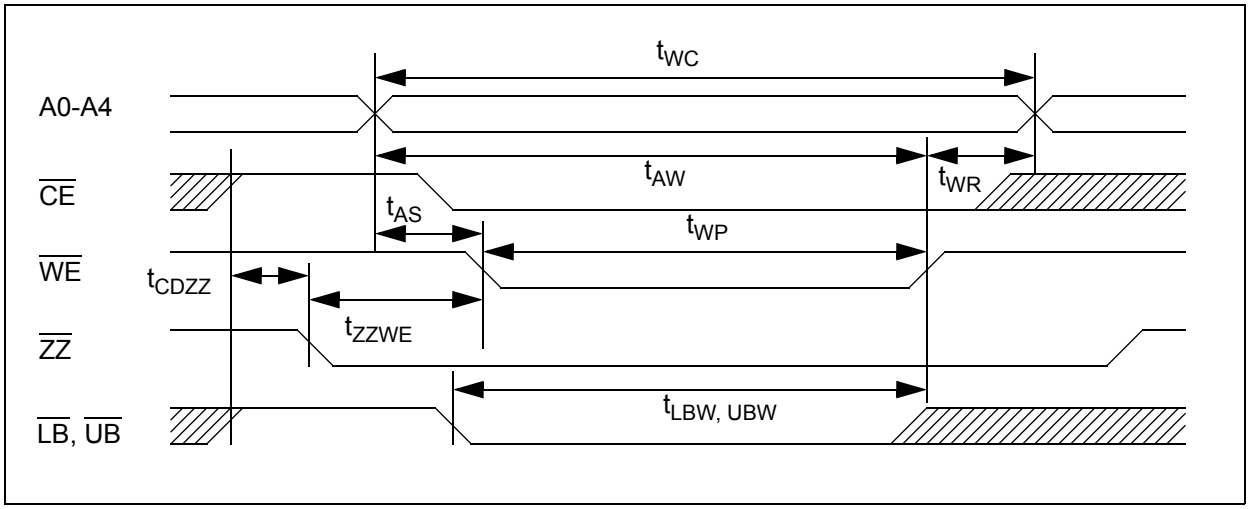


FIGURE 4: Deep Sleep Mode - Entry/Exit Timings

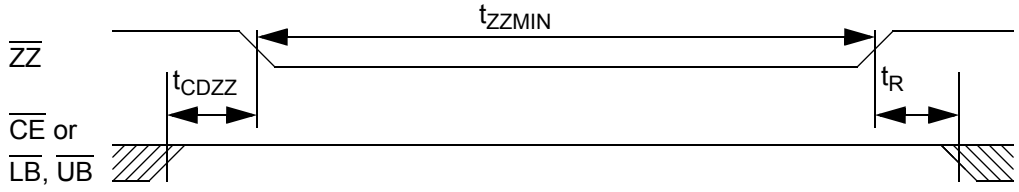


Table 1: VAR Update and Deep Sleep Timings

Item	Symbol	Min	Max	Unit
PAR and RMS $\overline{ZZ}$ low to $\overline{WE}$ low	t_{zzwe}		1000	ns
Chip ($\overline{CE}$, $\overline{UB}$/$\overline{LB}$) deselect to ZZ low	t_{cdzz}	0		ns
Deep Sleep Mode	t_{zzmin}	10		us
Deep Sleep Recovery	t_r	200		us

TABLE 2: Address Patterns for PAR (A3 = 0, A4 = 1)

A2	A1	A0	Active Section	Address space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

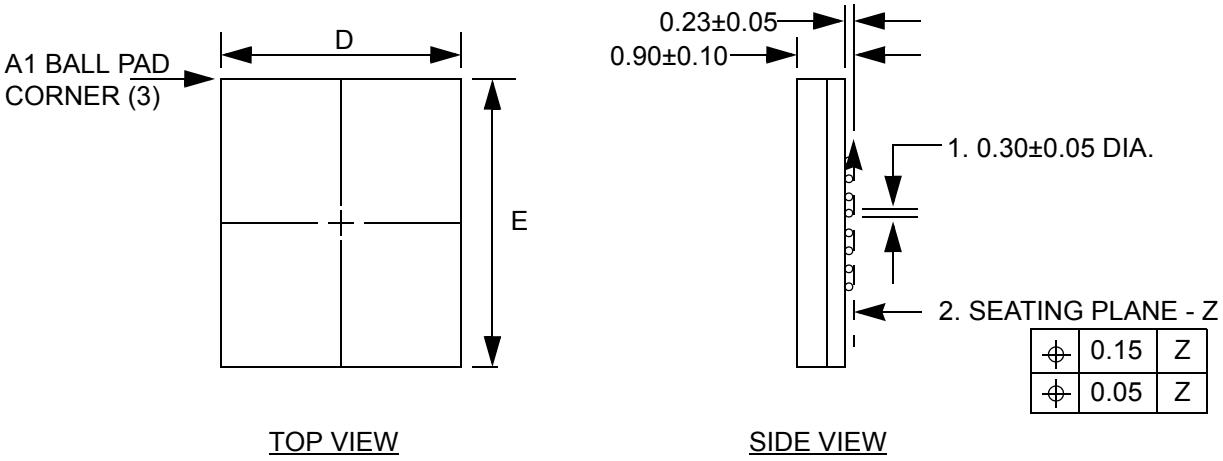
TABLE 3: Address patterns for RMS (A3 = 1, A4 = 1)

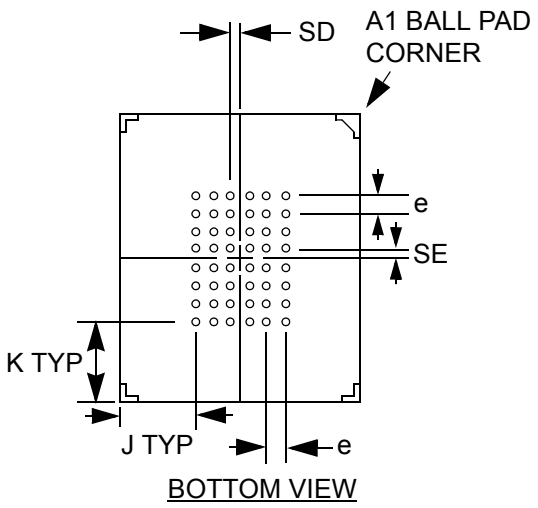
A2	A1	A0	Active Section	Address space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
0	0	0	Full die	000000h - 1FFFFFh	2Mb x 16	32Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb
1	0	0	Full die	000000h - 1FFFFFh	2Mb x 16	32Mb

TABLE 4: Low Power ICC Characteristics for N32T1630C1C

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PAR Mode Standby Current	I_{PAR}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85^oC$	1/4 Array		tbd	uA
			1/2 Array		tbd	
RMS Mode Standby Current	I_{RMSSB}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85^oC$	8Mb Device		tbd	uA
			16Mb Device		tbd	
Deep Sleep Current	I_{ZZ}	$V_{IN} = V_{CC}$ or 0V, Chip in $\overline{ZZ}$ mode, $t_A = 85^oC$			10	uA

VFRBGA Package Dimension





1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

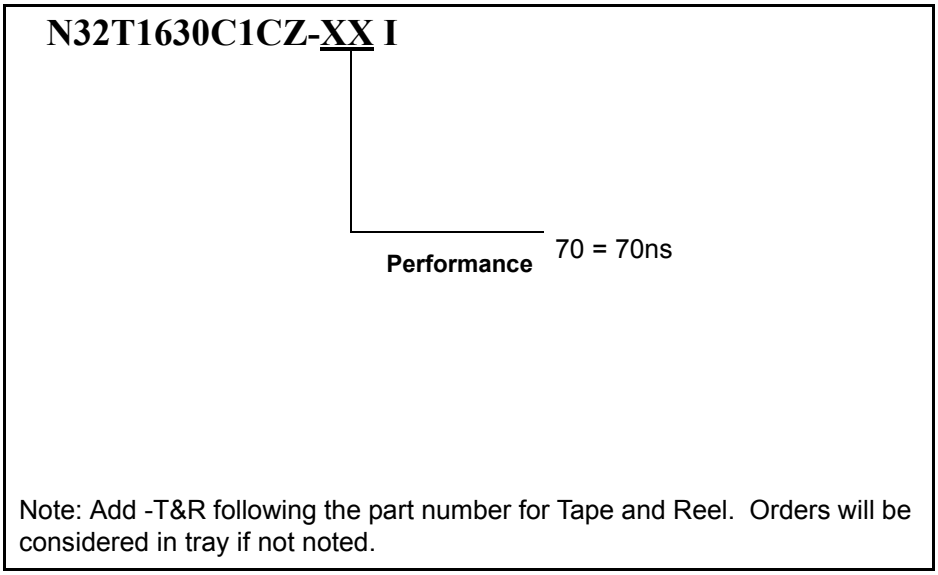
2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Ordering Information



Note: Add -T&R following the part number for Tape and Reel. Orders will be considered in tray if not noted.

Revision History

Revision	Date	Change Description
A	July 2004	Initial Release
B	July 2004	General Update
C	August 2004	Changed Ball (E3) from Vss to DNU/VSS Changed Max Vcc/VccQ from 3.3V to 3.6V