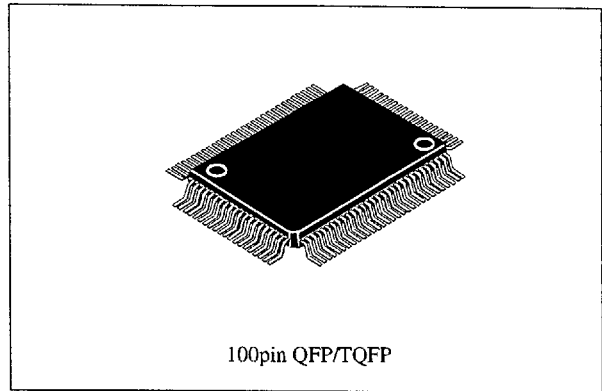
	<h2 style="margin: 0;">CMOS Low Voltage SRAM</h2> <p style="margin: 0;">Fast Synchronous with Burst Counter</p> <p style="margin: 0;">1M-BIT(32KX32)</p>	<h2 style="margin: 0;">N343532L</h2> <p style="margin: 0;">-K, -N</p>
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**■ Features**

- CMOS SRAM organized as 32,768 x 32bits
- Single +3.3V Power Supply
- Fast Clock Access time : 8ns/66MHz
- Synchronous operation
- Burst Read/Write :
  - Pentium™ Burst and Linear Burst Sequence
- Fully Registers Inputs and Outputs for Pipelined Operation
- All Registers triggered off Positive Clock Edge
- Asynchronous Output Enable :  $\overline{BW1}$  -  $\overline{BW4}$ ,  $\overline{BWE}$   
and Global Write Enable :  $\overline{GW}$
- Three Chip Enables for Easy Depth Expansion
- 2 Clock Enable and 1 Clock Disable to eliminate multiple bank bus contention
- Common I/O Using Three State Outputs
- 5V Tolerant Clock Pin (-K, -N Versions)
- Flow-Through Mode (-N Version)
- Sleep Mode (-N Version)
- Package
  - 100pin QFP
  - 100pin TQFP (1.6mm Max.)



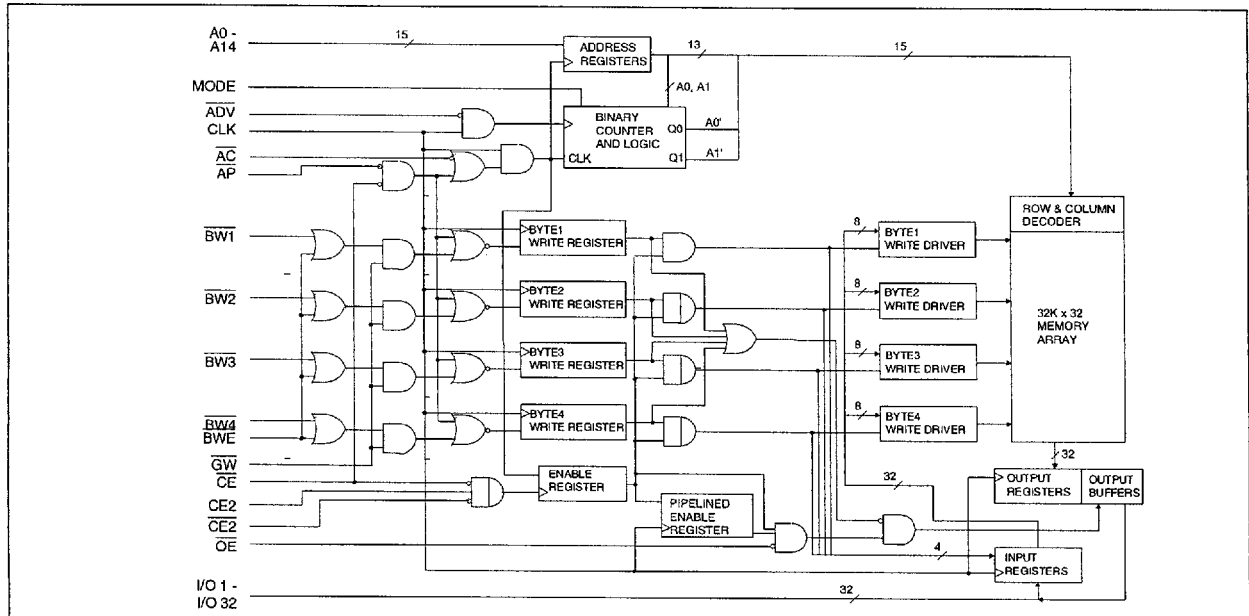
**■ Description**

The N343532L is a 32,768 x 32bit synchronous static RAM fabricated with NKK's advanced CMOS technology.

N343532L a high-speed device. The N343532L is suitable for applications which require high-speed device, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

This technology and unique peripheral circuits make the

**■ Functional Block Diagram**



■ Pin Configuration

100 pin QFP/TQFP

■ Pin Description

SYMBOL	PIN NAME
A0-A14	Address input
I/O0-I/O32	Data input/output
ADV	Burst Address Advance
AC	Controller Address Status
AP	Processor Address Status
CE	Chip Enable input
CE2	Chip Enable input
CE2	Chip Enable input
BW1 - BW4	Byte Write Enable, BW1 Controls I/O1-8, BW2 Controls I/O9-16, BW3 Controls I/O17-24, BW4 Controls I/O25-32
BWE	
GW	Global Write Enable
OE	Output Enable input
CLK	System Clock input
MODE	Mode Select
FT	Flow-Through Pin (-N Version)
ZZ	Sleep Mode Pin (-N Version)
VCC	Power Supply Pin (+3.3V)
GND	Ground Pin
VCCQ	Power Supply Pin for Outputs (+3.3V)
GNDQ	Ground Pin for Outputs
NC	No Connection

■ Pentium™ Burst Sequence Table (MODE = NC or VCC)

External Address	A14 - A2, A1, A0
1st Burst Address	A14 - A2, A1, $\overline{A0}$
2nd Burst Address	A14 - A2, $\overline{A1}$ , A0
3rd Burst Address	A14 - A2, $\overline{A1}$ , $\overline{A0}$

■ Linear Burst Sequence Table (MODE = GND)

External Address	A14 - A2, 0, 0	A14 - A2, 0, 1	A14 - A2, 1, 0	A14 - A2, 1, 1
1st Burst Address	A14 - A2, 0, 1	A14 - A2, 1, 0	A14 - A2, 1, 1	A14 - A2, 0, 0
2nd Burst Address	A14 - A2, 1, 0	A14 - A2, 1, 1	A14 - A2, 0, 0	A14 - A2, 0, 1
3rd Burst Address	A14 - A2, 1, 1	A14 - A2, 0, 0	A14 - A2, 0, 1	A14 - A2, 1, 0

NOTE : The burst sequence wraps around to its initial state upon completion.

MODE and FT are DC operated pins. Do not alter input state while device is operating.

**■ Asynchronous Truth Table**

(Standard, -K Versions)

Operation	$\overline{OE}$	I/O
Read Cycle	L	Dout
Read Cycle	H	Hi-Z
Write Cycle	X	Hi-Z - Din
Deselected	X	Hi-Z

(-N Version)

Operation	ZZ	$\overline{OE}$	$\overline{FT}$	I/O
Non-Pipelined Read Cycle	L	L	L	Dout
Non-Pipelined Read Cycle	L	H	L	Hi-Z
Pipelined Read Cycle	L	L	H	Dout
Pipelined Read Cycle	L	H	H	Hi-Z
Write Cycle	L	X	X	Hi-Z - Din
Deselected	L	X	X	Hi-Z
Sleep	H	X	X	Hi-Z

## NOTE

- (1) : X means "don't care".
- (2) : For a write operation following a read operation,  $\overline{OE}$  must be high before the input data required setup time and held through the input data hold time.
- (3) : Normally,  $\overline{FT}$  is pulled to High or NC.  $\overline{FT}$  = Low input is only used for a test mode.

**■ Synchronous Truth Table**

Operation	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{AP}$	$\overline{AC}$	$\overline{ADV}$	WRITE	CLK	Address	I/O
Deselected	H	X	X	X	L	X	X	↑	N/A	Hi-Z
Deselected	L	X	L	L	X	X	X	↑	N/A	Hi-Z
Deselected	L	H	X	L	X	X	X	↑	N/A	Hi-Z
Deselected	L	X	L	H	L	X	X	↑	N/A	Hi-Z
Deselected	L	H	H	H	L	X	X	↑	N/A	Hi-Z
Read Cycle / Begin Burst	L	L	H	L	X	X	X	↑	External	Hi-Z
Read Cycle / Begin Burst	L	L	H	H	L	X	H	↑	External	Hi-Z
Read Cycle / Continue Burst	X	X	X	H	H	L	H	↑	Next	Data/Hi-Z
Read Cycle / Continue Burst	H	X	X	X	H	L	H	↑	Next	Data/Hi-Z
Read Cycle / Suspend Burst	X	X	X	H	H	H	H	↑	Current	Data/Hi-Z
Read Cycle / Suspend Burst	H	X	X	X	H	H	H	↑	Current	Data/Hi-Z
Write Cycle / Begin Burst	L	L	H	H	L	X	L	↑	External	Hi-Z
Write Cycle / Continue Burst	X	X	X	H	H	L	L	↑	Next	Hi-Z
Write Cycle / Continue Burst	H	X	X	X	H	L	L	↑	Next	Hi-Z
Write Cycle / Suspend Burst	X	X	X	H	H	H	L	↑	Current	Hi-Z
Write Cycle / Suspend Burst	H	X	X	X	H	H	L	↑	Current	Hi-Z

## NOTE

- (1) : X means "don't care",  $\overline{WRITE} = L$  means any one or more byte write enables ( $\overline{BW1}$ ,  $\overline{BW2}$ ,  $\overline{BW3}$  or  $\overline{BW4}$ ) and  $\overline{BWE}$  are Low or  $\overline{GW}$  is Low.

$\overline{WRITE} = H$  means all byte write enables and  $\overline{GW}$  are High.

- (2) :  $\overline{ADV}$  must be High at the rising edge of the first clock after a  $\overline{AP}$  cycle is initiated if a WRITE cycle is desired. (to ensure use of correct address)
- (3) : Data/Hi-Z means that the condition of the I/O's are controlled by  $\overline{OE}$ , I/O outputs data when  $\overline{OE} = L$ , otherwise I/O = Hi-Z.


**■ Partial Truth Table for Write Enable**

Operation	$\overline{\text{GW}}$	$\overline{\text{BWE}}$	$\overline{\text{BW1}}$	$\overline{\text{BW2}}$	$\overline{\text{BW3}}$	$\overline{\text{BW4}}$
Read Cycle	H	H	X	X	X	X
Read Cycle	H	L	H	H	H	H
Write Cycle / Byte 1 only	H	L	L	H	H	H
Write Cycle / All Bytes	H	L	L	L	L	L
Write Cycle / All Bytes	L	X	X	X	X	X

## NOTE

- (1) : X means " don't care".  
 (2) : Using  $\overline{\text{BWE}}$  and  $\overline{\text{BW1}}$ , through  $\overline{\text{BW4}}$ , any one or more bytes may be written.

**■ Absolute Maximum Ratings**

Symbol	Rating	Min.	Max.	Unit	Note	
VCC	Supply Voltage	GND - 0.5	4.6	V		
VTERM	Terminal Voltage with Respect to GND	CLK	GND - 0.5	VCC + 0.5 (Max. 4.6)	V	
			GND - 0.5	VCC + 2.4 (Max. 6.0)	V	1
		All Other Pins	GND - 0.5	VCC + 0.5 (Max. 4.6)	V	
TA	Operating Temperature	0	70	°C		
TBIAS	Temperature Under Bias	-55	125	°C		
TSTG	Storage Temperature	-55	125	°C		

## NOTICE

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indication in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## NOTE

- (1) : -K, -N Versions.

**■ Recommended Operating Conditions**

Recommended DC Operating Conditions (TA = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
Vcc, Vccq	Supply Voltage	3.1	3.3	3.6	V	
GND	Supply Voltage	0	0	0	V	
VIH	Input High Voltage	I/O - I/O32		Vccq + 0.3	V	
			CLK	2.0	Vcc + 0.3	V
			2.0	Vcc + 2.4 (Max. 5.5)	V	1
		All Other Pins	2.0	Vcc + 0.3	V	
VIL	Input Low Voltage	-0.3		0.8	V	2

## Note

- (1) : -K, -N Versions  
 (2) : VIL(min) = -2.0V for pulse width less than 10ns.


**■ Capacitance**

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE : These parameters are periodically sampled and not 100% tested.

**■ DC Electrical Characteristics**

(TA = 0 to +70°C, VCC = 3.3V + 0.3V / - 0.2V)

Symbol	Parameter	66MHz	Unit	Note
ICC	Operating Supply Current Device selected, VIN ≤ VIL or ≥ VIH, I(I/O) = 0	250	mA	
		185	mA	1
ISB	Standby Supply Current Device deselected, VIN ≤ VIL or ≥ VIH (0MHz)	20	mA	2
ISB1	Standby Supply Current Device deselected, VIN ≤ 0.2V or ≥ Vcc - 0.2V VIN(I/O) ≥ Vccq - 0.2V or ≤ 0.2V (0MHz)	2	mA	2
ISB2	Standby Supply Current Device deselected, VIN ≤ VIL or ≥ VIH	50	mA	
ISB3	Sleep Mode Supply Current ZZ ≥ Vcc - 0.2V	2	mA	1

NOTE

(1) : -N Version only

(2) : All Inputs Static.

## DC Electrical Characteristics(1)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
ILI	Input Leakage Current	VIN = 0 to VCC	-2	2	μA
ILO	I/O Leakage Current	V/I/O = 0 to VCC, Output Disabled	-2	2	μA
VOL	Output low voltage	IOL = 8mA	-	0.4	V
VOH	Output high voltage	IOH = -5mA	2.4	-	V

NOTE

 (1) : MODE,  $\overline{FT}$  and ZZ are internally biased and exhibit an input leakage current of ± 400 μA.



■ AC Test Conditions

Input pulse levels	GND to 3V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	See figure 1 and 2

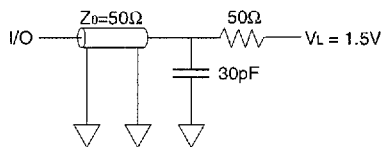


Figure 1. Output load Equivalent

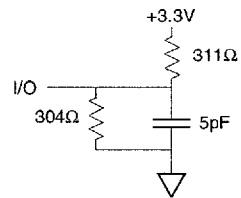


Figure 2. Output load Equivalent  
(for tDC1, tOLZ, tOHZ, tCZ)


**■ AC Electrical Characteristics**

(TA = 0 to +70°C, VCC = 3.3V + 0.3V/ - 0.2V)

## Read and Write Cycle

Parameter	Symbol		66MHz		Unit
	Standard	Standard	Min.	Max.	
Cycle Time	t <sub>KHKH</sub>	t <sub>CYC</sub>	15.0		ns
Clock Access Time(Std load)	t <sub>KHOV</sub>	t <sub>CD</sub>		8.0	ns
Output Enable to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		5.0	ns
Clock High to Output Active	t <sub>KHQX1</sub>	t <sub>DC1</sub>	0.0		ns
Clock High to Output Change	t <sub>KHQX2</sub>	t <sub>DC2</sub>	2.0		ns
Output Enable to Output Active	t <sub>GLQX</sub>	t <sub>OLZ</sub>	0.0		ns
Output Disable to output Hi-Z	t <sub>GHQZ</sub>	t <sub>OHZ</sub>	2.0	5.0	ns
Clock High to Output Hi-Z	t <sub>KHQZ</sub>	t <sub>CZ</sub>	2.0	6.0	ns
Clock High Pulse Width	t <sub>KHKL</sub>	t <sub>CH</sub>	5.0		ns
Clock Low Pulse Width	t <sub>KLKH</sub>	t <sub>CL</sub>	5.0		ns
Setup Times : Address	t <sub>AVKH</sub>	t <sub>AS</sub>	2.5		ns
Address Status	t <sub>ADSVKH</sub>	t <sub>SS</sub>	2.5		ns
Data In	t <sub>DVKH</sub>	t <sub>DS</sub>	2.5		ns
Write Enable	t <sub>WVKH</sub>	t <sub>WS</sub>	2.5		ns
Address Advance	t <sub>ADVVKH</sub>		2.5		ns
Chip Enable	t <sub>EVKH</sub>		2.5		ns
Hold Times : Address	t <sub>KHAX</sub>	t <sub>AH</sub>	0.5		ns
Address Status	t <sub>KHADSX</sub>	t <sub>SH</sub>	0.5		ns
Data In	t <sub>KHDX</sub>	t <sub>DH</sub>	0.5		ns
Write Enable	t <sub>KHWX</sub>	t <sub>WH</sub>	0.5		ns
Address Advance	t <sub>KHADVX</sub>		0.5		ns
Chip Enable	t <sub>KHEX</sub>		0.5		ns
ZZ Standby Time	t <sub>ZZS</sub>			60.0	ns
ZZ Recovery Time	t <sub>ZZREC</sub>		60.0		ns

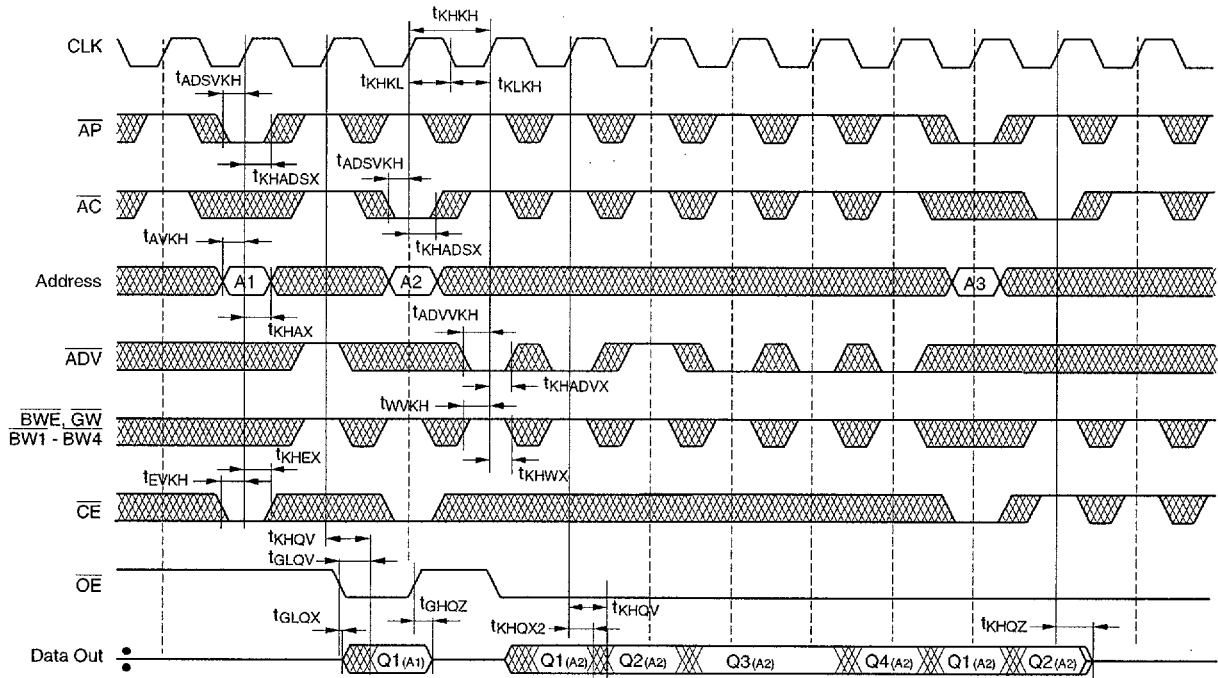
**NOTE**

- (1) : t<sub>ZZS</sub> and t<sub>ZZREC</sub> is for -N Version only.  
 (2) : t<sub>DC1</sub>, t<sub>OLZ</sub>, t<sub>OHZ</sub> and t<sub>CZ</sub> are sampled and not 100% tested.



■ AC Timing Waveforms

Read Cycle



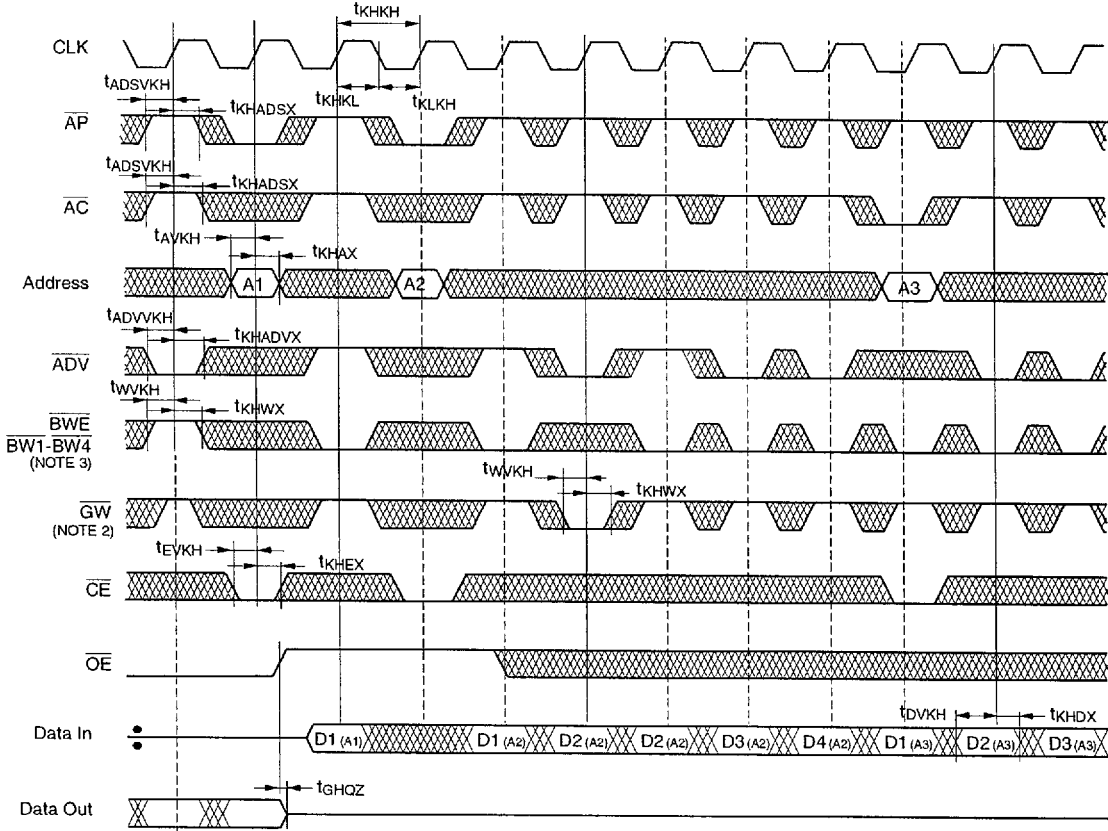
NOTE

- (1) : Qn(2) refer to output from address A2. Q1 - Q4 refer to output burst sequence.
- (2) :  $\overline{CE2}$  and CE2 have the same timing as  $\overline{CE}$ . In this timing, When  $\overline{CE}$  Low,  $\overline{CE2}$  is Low and CE2 is High. When  $\overline{CE}$  is High,  $\overline{CE2}$  is High and CE2 is Low.

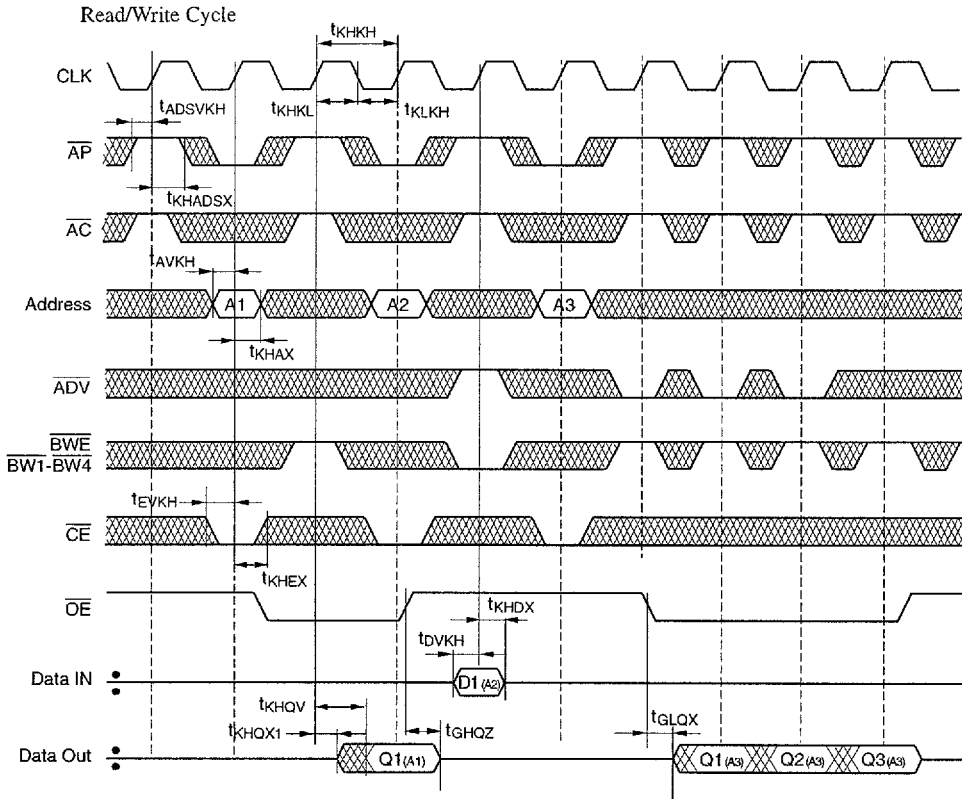




Write Cycle

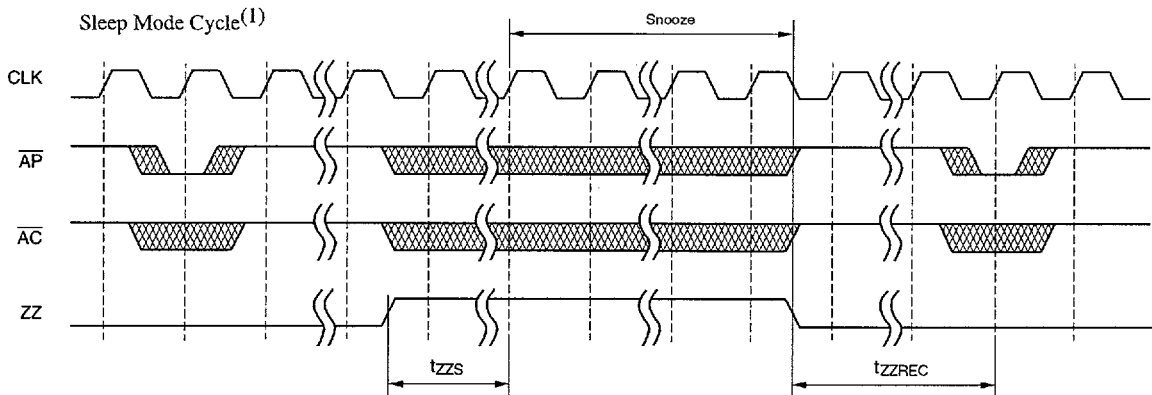


- NOTE
- (1) :  $\overline{CE2}$  and  $CE2$  have the same timing as  $\overline{CE}$ . In this timing, When  $\overline{CE}$  Low,  $\overline{CE2}$  is Low and  $CE2$  is High. When  $\overline{CE}$  is High,  $\overline{CE2}$  is High and  $CE2$  is Low.
  - (2) : All bytes WRITE can be initiated by  $\overline{GW}$  Low or  $\overline{GW}$  High and  $\overline{BWE}$ ,  $\overline{BW1}$  -  $\overline{BW4}$  Low.
  - (3) :  $\overline{BWE}$  is low when any one or more Byte Write Enable ( $\overline{BW1}$ ,  $\overline{BW2}$ ,  $\overline{BW3}$  and  $\overline{BW4}$ ) are low in this diagram.



NOTE

- (1) :  $\overline{CE2}$  and  $CE2$  have the same timing as  $\overline{CE}$ . In this timing, When  $\overline{CE}$  Low,  $\overline{CE2}$  is Low and  $CE2$  is High. When  $\overline{CE}$  is High,  $\overline{CE2}$  is High and  $CE2$  is Low.
- (2) :  $\overline{GW}$  is High in this diagram.



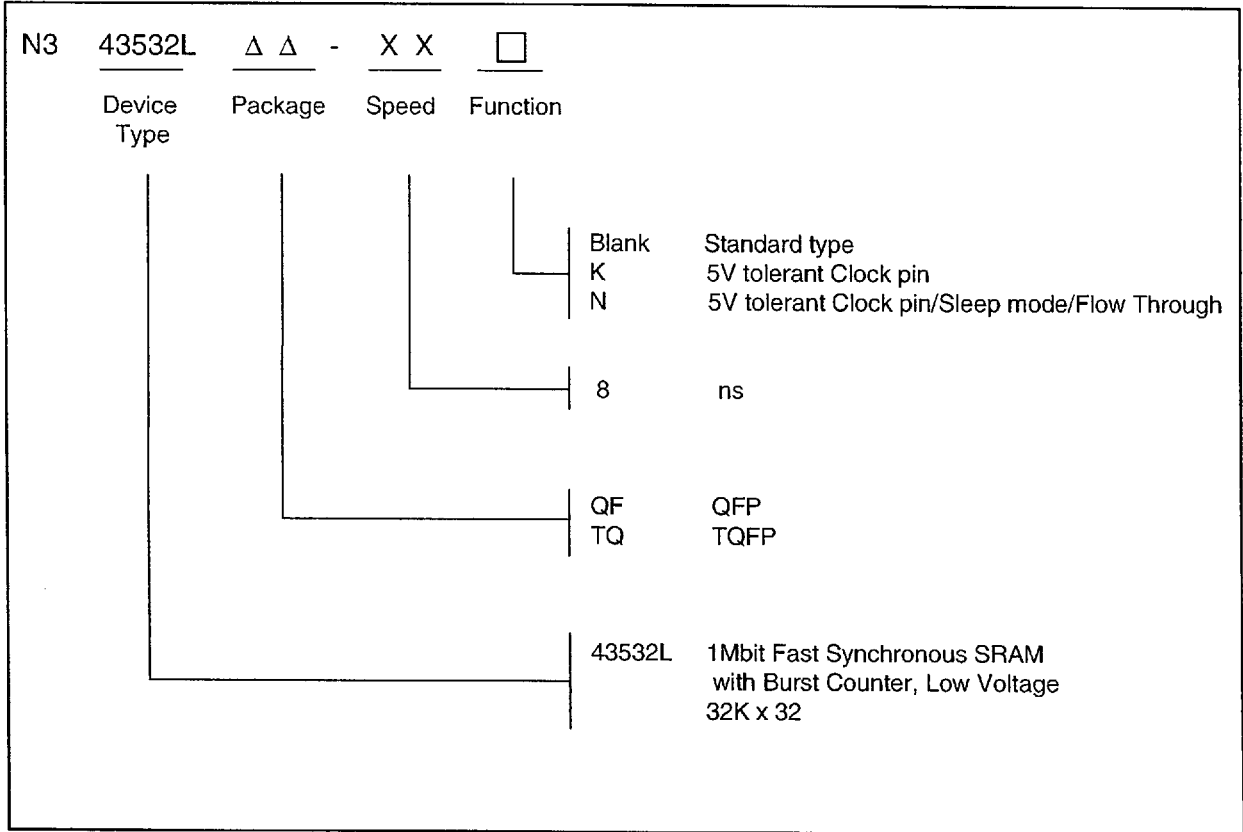
NOTE

- (1) : -N Version only.
- (2) : Data retention is guaranteed when  $\overline{ZZ}$  is asserted and clock remains active.
- (3) :  $\overline{AC}$  and  $\overline{AP}$  must be asserted for a least 60.0ns after leaving  $\overline{ZZ}$  state.
- (4) : Do not assert  $\overline{ZZ}$  during a write operation.
- (5) :  $\overline{AC}$  and  $\overline{AP}$  must be High at rising edge of CLK when the transition of  $\overline{ZZ}$  from High to Low or Low to High occurs



**N343532L**  
-K, -N

■ Ordering informations



PART NO.	Access Time (ns)	Clock Frequency (MHz)	Operating Current (mA)	Package
N343532LQF-8	8	66	250	100Pin QFP
N342532LTQ-8	8	66	250	100Pin TQFP
N343532LQF-8K	8	66	250	100Pin QFP
N342532LTQ-8K	8	66	250	100Pin TQFP
N343532LQF-8N	8	66	185	100Pin QFP
N342532LTQ-8N	8	66	185	100Pin TQFP

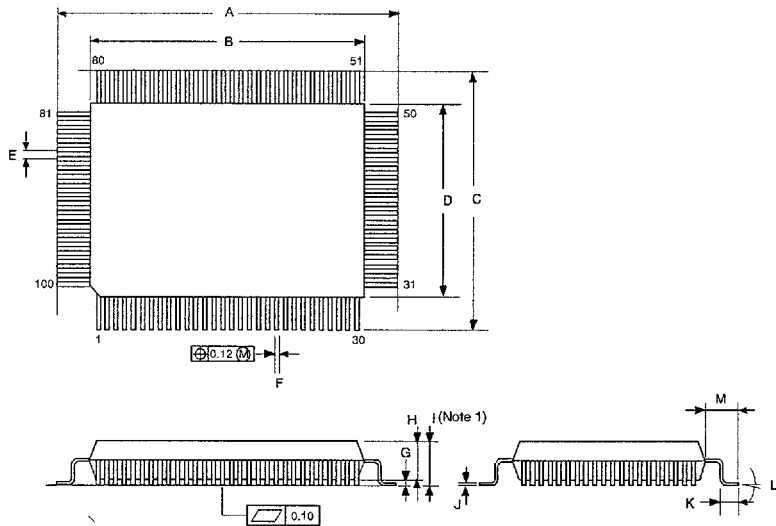


N343532L  
-K, -N

■ Package Information

100pin QFP

ITEM	MILLIMETERS	INCHES
A	23.20 ± 0.25	0.913 ± 0.010
B	20.0 ± 0.10	0.787 ± 0.004
C	17.20 ± 0.25	0.677 ± 0.010
D	14.0 ± 0.10	0.551 ± 0.004
E	0.65 ± 0.2008	0.026 ± 0.003
F	.030 +0.06 - 0.10	0.012 +0.002 - 0.004
G	0.40 +0.10 - 0.15	0.016 +0.004 - 0.006
H	2.70 +0.20 - 0.15	0.106 +0.008 - 0.006
I	3.40 [Max.]	0.134 [Max.]
J	0.17 +0.06 - 0.04	0.007 +0.0024 - 0.0016
K	0.80 ± 0.15	0.031 ± 0.006
L	0 to 10°	0 to 10°
M	1.60 [Typ.]	0.063 [Typ.]

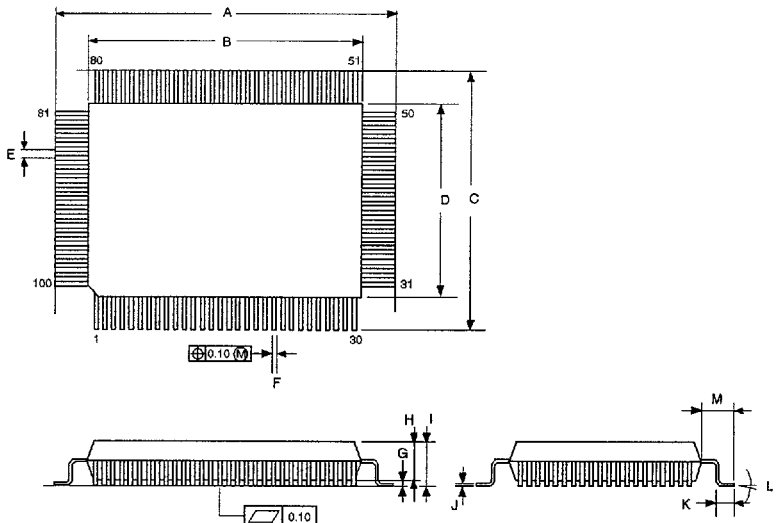


Notes

1. These dimensions include package bend.
2. Burrs on the package side surface are less than 0.20mm.

100pin TQFP

ITEM	MILLIMETERS	INCHES
A	22.00 ± 0.20	0.866 ± 0.008
B	20.0 [Typ.]	0.787 [Typ.]
C	16.00 ± 0.20	0.630 ± 0.008
D	14.0 [Typ.]	0.551 [Typ.]
E	0.65 [Typ.]	0.026 [Typ.]
F	0.30 +0.08 - 0.05	0.012 +0.003 - 0.002
G	0.10 ± 0.05	0.004 ± 0.002
H	1.40 ± 0.05	0.055 ± 0.002
I	1.60 [Max.]	0.063 [Max.]
J	0.17 ± 0.05	0.007 ± 0.002
K	0.50 ± 0.10	0.020 ± 0.004
L	0 to 10°	0 to 10°
M	1.00 [Typ.]	0.039 [Typ.]



Notes

1. These dimensions include package bend.
2. Burrs on the package side surface are less than 0.20mm.