



# STN3PF06

P-channel 60 V - 0.20  $\Omega$  - 2.5 A - SOT-223  
STripFET™ II Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STN3PF06	60 V	< 0.22 $\Omega$	2.5 A

- Extremely dv/dt capability
- 100% avalanche tested
- Application oriented characterization

## Application

- Switching applications

## Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

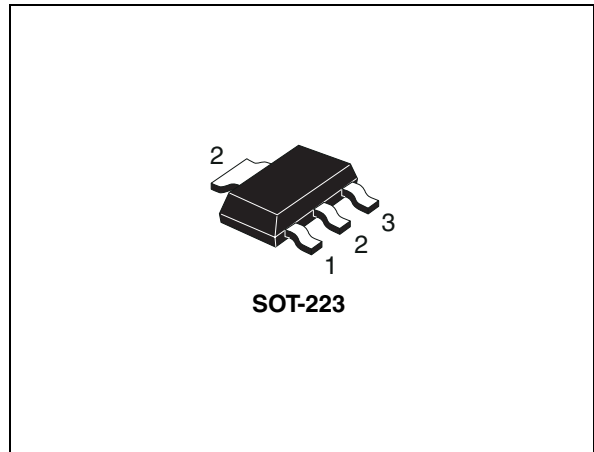


Figure 1. Internal schematic diagram

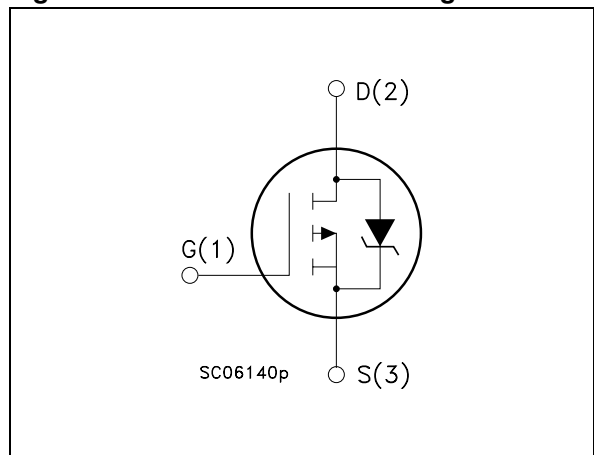


Table 1. Device summary

Order code	Marking	Package	Packaging
STN3PF06	N3PF06	SOT-223	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	10	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2.5	W
	Derating factor	0.02	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	6	V/ns
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-65 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 3\text{A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$	Thermal resistance junction-pcb board max	50	$^\circ\text{C}/\text{W}$
$R_{thj-a}$	Thermal resistance junction-ambient max <sup>(1)</sup>	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	260	$^\circ\text{C}$

1. Surface mounted

*Note:* For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

## 2 Electrical characteristics

(T<sub>CASE</sub>=25 °C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> =125 °C			1 10	μA μA
I <sub>D(on)</sub>	On state drain current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , V <sub>GS</sub> = 10 V	2.5			A
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A		0.20	0.22	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 1.25 A		1.5		S
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		850		pF
C <sub>oss</sub>	Output capacitance			230		pF
C <sub>rss</sub>	Reverse transfer capacitance			75		pF
Q <sub>g</sub>	Total gate charge	I <sub>D</sub> = 12 A, V <sub>DD</sub> = 48 V, V <sub>GS</sub> = 10 V <i>(see Figure 14)</i>		16	21	nC
Q <sub>gs</sub>	Gate-source charge			4		nC
Q <sub>gd</sub>	Gate-drain charge			6		nC

*Note:* For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=30\text{ V}$ , $I_D=6\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 13)		20 40		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=30\text{ V}$ , $I_D=6\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 13)		40 10		ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage rise time Fall time Cross-over time	$V_{clamp}=48\text{ V}$ , $I_D=12\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 13)		10 17 30		ns ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				2.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				10	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=1.5\text{ A}$ , $V_{GS}=0$			1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD}=12\text{ A}$ , $di/dt=100\text{ A}/\mu\text{s}$ $V_{DD}=30\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$		100		ns
$Q_{rr}$	Reverse recovery charge			260		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			5.2		A

1. Pulse width limited by  $T_{jmax}$

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Note:** For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

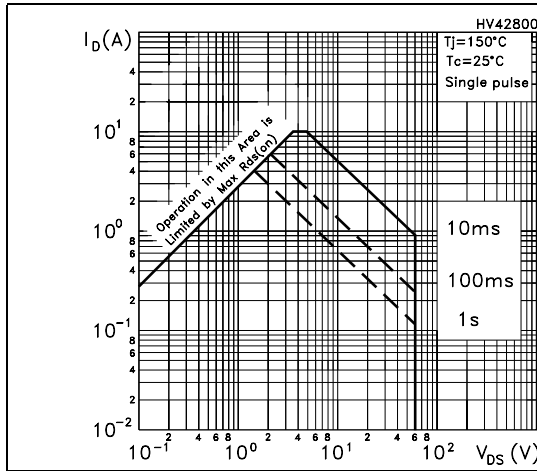


Figure 3. Thermal impedance

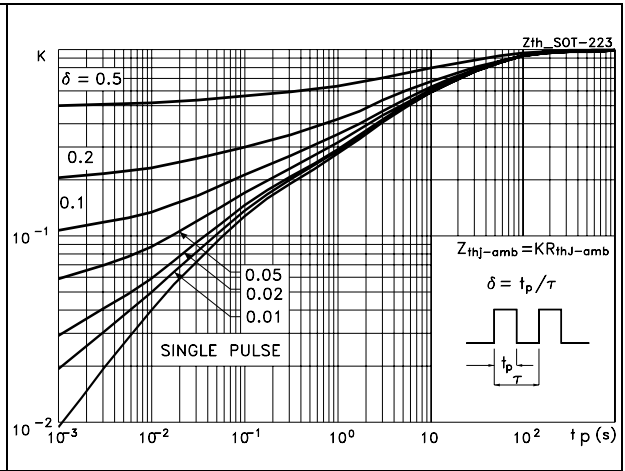


Figure 4. Output characteristics

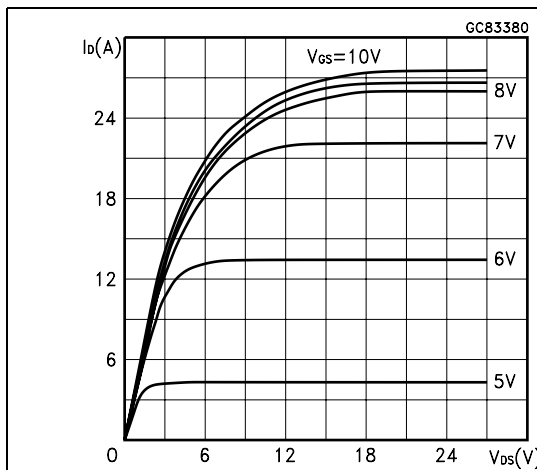


Figure 5. Transfer characteristics

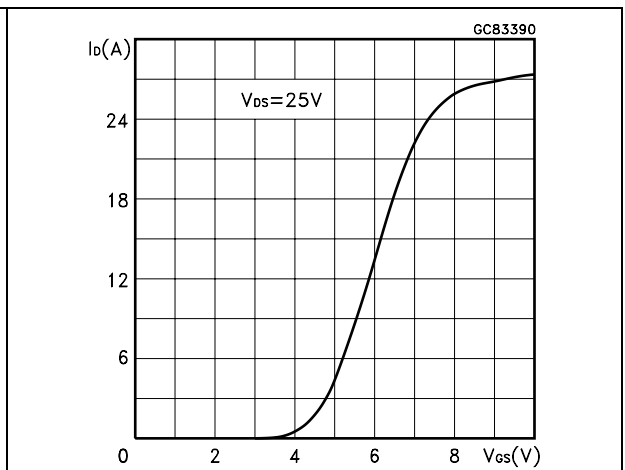


Figure 6. Transconductance

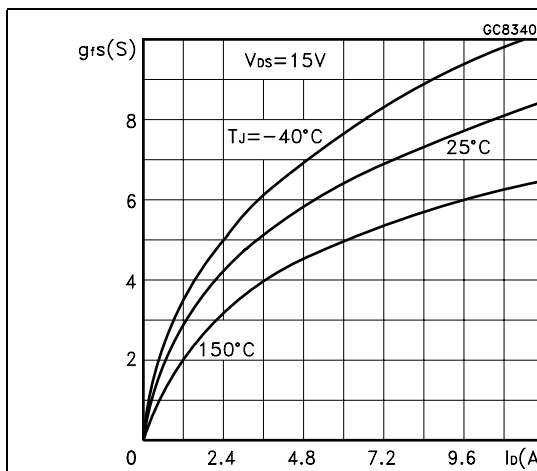


Figure 7. Static drain-source on resistance

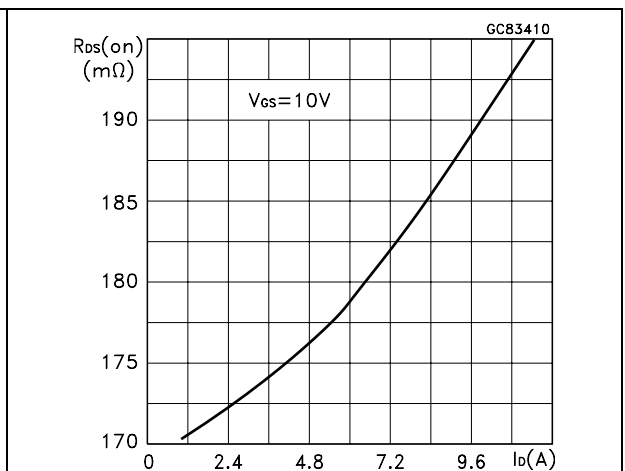


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

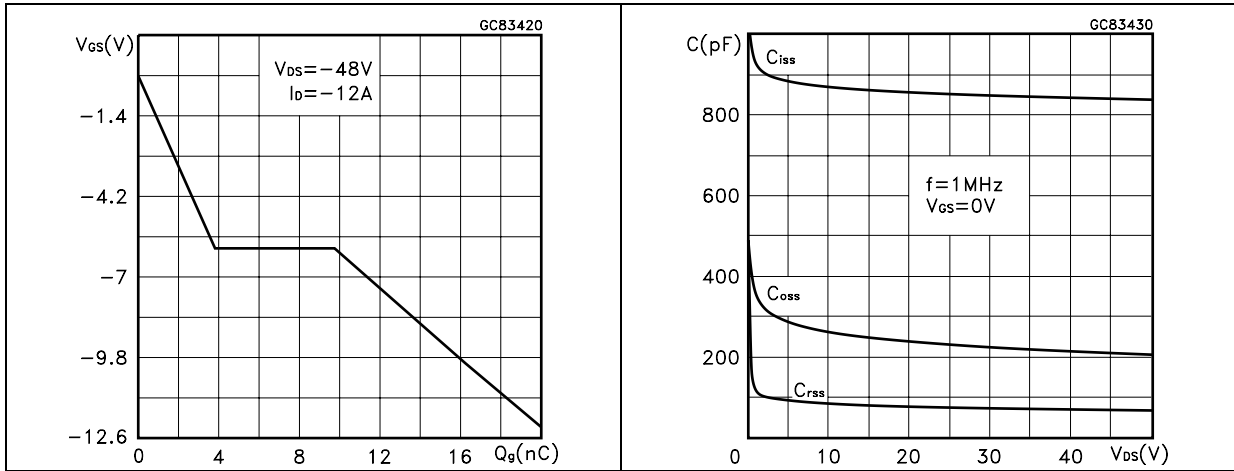


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

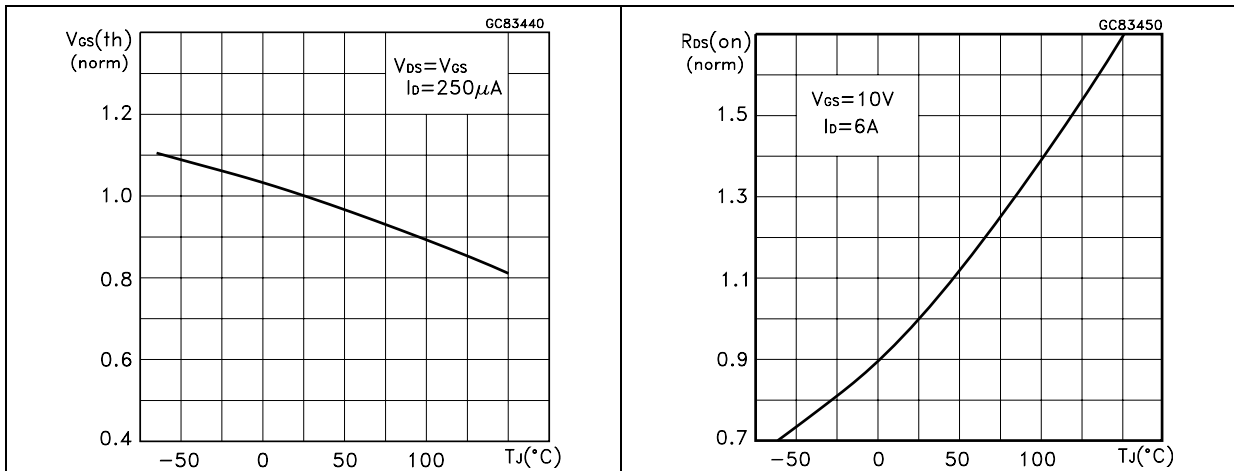
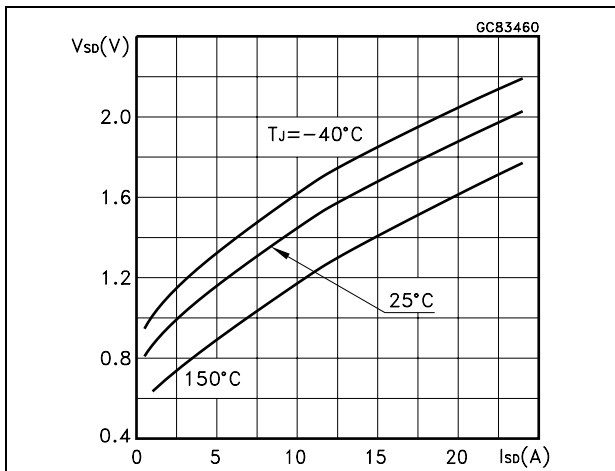


Figure 12. Source-drain diode forward characteristics



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

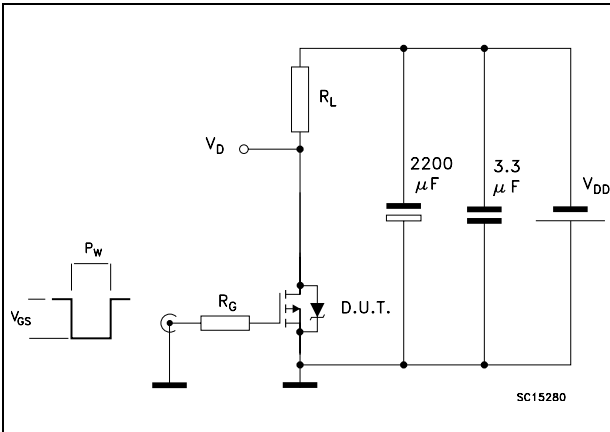


Figure 14. Gate charge test circuit

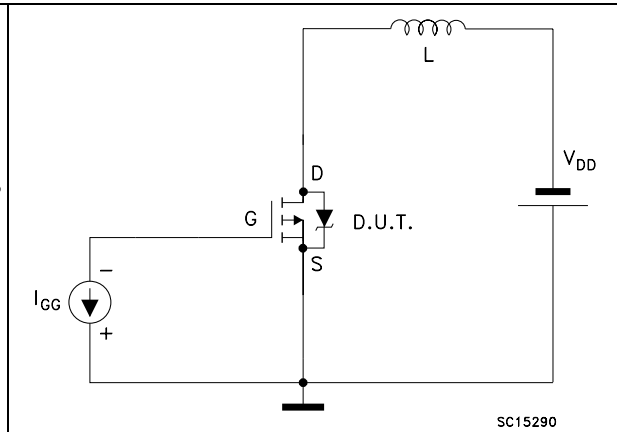
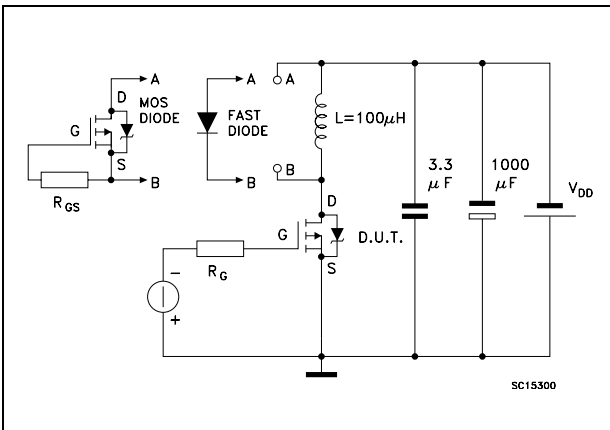


Figure 15. Test circuit for inductive load switching and diode recovery times





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

SOT-223 MECHANICAL DATA						
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				

P008B

## 5 Revision history

**Table 8. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
08-May-2007	3	The document has been reformatted
27-Mar-2008	4	Document status promoted from preliminary data to datasheet.

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