N537A090

Data Sheet

2-ch Speech/Dual Tone/LCD Controller

(ViewTalk® Series)

Table of Contents

1. GENERAL DESCRIPTION

The N537A090 series, a member of the *ViewTalk*™ family, is an 8-bit uC base with a speech and dual tone synthesizer and 64SEG x 32COM LCD driver unit, which includes an internal regulator, pump circuit and one page of dedicated LCD RAM to generate a high quality of LCD display. The 537A/Txxx family offers many significant features including wide operation voltage for either 2 or 3 batteries applications, 2 channels of speech and/or wavetable melody or dual tone, 1000~2000 dots LCD driver, large size of working RAM, 2M bits~ 8M bits ROM size, 12 or 16~24 dedicated I/Os, IR carrier, Low Voltage Detector, and so forth. Furthermore, it also provides multiple power modes to minimize power dissipation, and provides Watch Dog Timer, Low Voltage Reset to prevent hanging-up occurring as power unstable or abnormal bouncing.

The N537A090 series is suitable for the applications of ELA, Hand-held Games, remote controllers, watches, clocks and others that incorporate both LCD display and speech or midi.

The part numbers of N537A090 and comparison with old W537A203 is as below table:

Part Number	ROM (KB)	LCD Dots (SEG x COM)	Working RAM (Byte)	LCD RAM (Byte)	I/O	Voice/Melody Channel	Audio Output
N537A090	281	64 x 16	1K	128	12+16[1]	2	PWM
W537A203	249	64 x 16	1K	128*2	16+16[2]	2	DAC/PWM

1 LCD Segment shared IOs

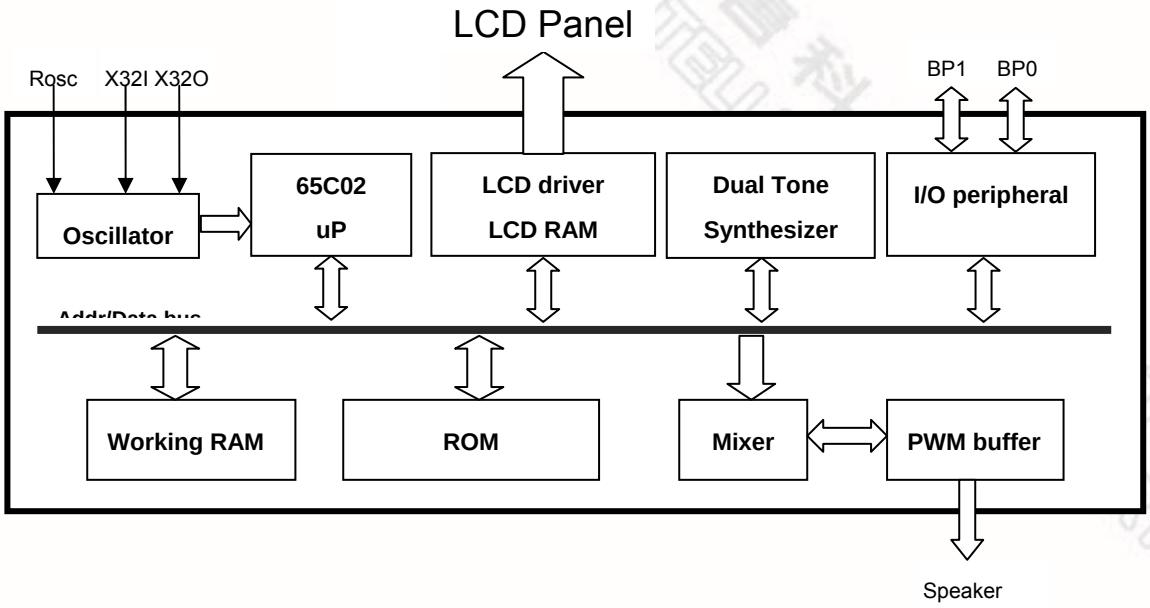
2 LCD Segment shared IOs

2. FEATURES

- **8-bit µP base Speech/Melody synthesizer with 1K dot LCD driver**
- **Wide operating voltage**
  - 4MHz: 2.4V ~ 5.5V
  - 6MHz: 2.9V ~ 5.5V
  - 8MHz: 3.2V ~ 5.5V
- **Provides two configurable system clocks: Main-clock and Sub-clock**
  - The Main-clock is Ring type.
  - The Sub-clock (32.768 KHz) can be selected as X'tal mode or RC type, based on CLKC.6 bit
- **Power management with SLOW, HOLD, and STOP modes**
- **Single ROM architecture to store program, user data/table, speech, timbres, score and pictures**
- **Built-in 1 KB working RAM (W-RAM)**
- **128 bytes LCD RAM (L-RAM)**
- **LCD driver unit**
  - 64 SEG X 16COM, 1/4 or 1/5 bias, 1/8 or 1/16 duty cycle
  - Built-in LCD regulator for stable display quality while speech or melody is playing
  - Built-in drawing operators, such as PUT, INV, AND, OR, XOR, etc., to simplify programming
  - Special registers to simplify block movement
- **Maximum 28 I/O pins and 8 of them can sinking 25mA@4.5V**
  - 12 dedicated I/O pins and 8 I/O pins can sink 25mA@4.5V
  - 16 LCD SEGMENT pins can be used as additional input or output pins
- **2 channels of speech and dual tone melody synthesis**
  - Speech synthesis at programmable playback rates
  - Different channel configurations using speech synthesis:
    - 2-channel speech
    - channel speech + 1-tone melody
    - Dual tone melody
- **Audio output**
  - PWM direct drive: 10-bit resolution, maximum 128 KHz sampling rate @ 8MHz[3] system clock
- Automatic IR-carrier generation for interactive applications
- Low Voltage Detector (LVD) for battery-life management application
- Low Voltage Reset (LVR) (set by mask option)
- Watch Dog Timer (WDT) (set by mask option)

3 8MHz main oscillator clock is used but with 4MHz system clock selection.

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
/RESET	I	IC reset input.
XIN	I	Input pin for the main-oscillator. Connect a resister between XIN and VSS to generate the main clock.
X32IN	I	Input pin for the sub-oscillator (F_S). When the CLKC.6=1, selects RC type, connect RS between X32IN and X32OUT to generate the sub clock. When the CLKC.6=0, selects crystal type, connect a 32-KHz crystal between X32IN and X32OUT.
X32OUT	O	Output pin for the sub-oscillator. Connect a 32-KHz crystal between X32IN and X32OUT.
BP0 [7:0][4]	I/O	Bi-direction port 0. As an input, each pad can be pulled-high or float. As an output, each pad can be an inverter or open-drain type. The configuration is controlled, pin-by-pin, by the associated bits in the BP0D and BP0M registers. Each pin can generate an interrupt when a transition is detected on its respective port. Each pin can detect SEG strobe queuing signals during key-matrix scan. BP0.7 can be used as the IR carrier output.
BP1 [7:4]	I/O	Bi-directional port 1. As an input, each pad can be pulled-high or float. As an output, each pad can be an inverter or open-drain type. The configuration is controlled, pin-by-pin, by the associated bits in the BP1D and BP1M registers. Each pin can generate an interrupt when a transition is detected on its respective port.
PWM+	O	PWM driver positive output.
PWM-	O	PWM driver negative output.
DH1, DH2	I	Connection terminals for the voltage-doubling capacitor used in the LCD driver.
V2	I/O	Voltage regulator output pin. It requires an external capacitor (0.1 uf).[5] If the internal pump is enabled (LCDMC1.5 = 0), the V2 output level is controlled by LCDMC0 [6:3]. If the external reference voltage is selected (LCDMC1.5 = 1), the V2 input voltage should not be more than 1.5 V to prevent chip damage.
V3, V4, V5, V6	O	LCD COM / SEG output driving voltages. Each pin requires an external capacitor. They are produced in terms of

[4] When working at NMOS open drain mode, external pull high voltage can't higher than VDD to avoid leakage current.

[5] 0.1 uF is the default value, but the capacitor value should be larger if the LCD dot size is greater than 0.5 mm * 0.5 mm

PIN NAME	I/O	FUNCTION
		V2.
SEG0 ~ SEG15	O	LCD segment output pins.
SEG16 ~ SEG47	O	LCD segment output pins
SEG48-SEG51, SEG56-SEG59	O/I	LCD segment output pins. These can be used as additional input pins using register LCDIMC, bits 0 and 1.
SEG52 ~ SEG55, SEG60 ~ SEG63	O/O	LCD segment output pins. These can be used as additional output pins using register LCDOMC, bits 0 and 1.
COM0 ~ COM15	O	LCD common output pins. COM15-COM8 could be configured to be floating.
VDD × 2	Power	Positive power supply. Used for oscillator, uP, logic cells and I/O buffers.
VSS × 2	Power	Negative power supply. Used for oscillator, uP, logic cells and I/O buffers.
VDD_SPK	Power	Positive power PWM driver.
VSS1_SPK	Power	Negative power PWM driver.
VSS2_SPK	Power	Negative power PWM / DAC driver.
TEST	I	Test pin, internally pulled low. It is pulled high in TEST mode. Do not connect during normal operation.

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 D.C. CHARATERISTICS

(VDD–VSS = 3.0V, No load, FM = 4 MHz with Ring mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C, STN LCD panel on with dot size 0.5mm*0.5mm; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}	-	2.4	-	5.5	V
Operating Current	I_{OP1}	Dual clock, VDD=3V	-	5	7.5	mA
	I_{OP1}	Sub clock only, VDD=3V	-	40	50	uA
Hold Mode Current (Sub-clock active only)	I_{OP2}	LCD OFF, VDD=3V,		8	10	uA
		LCD ON, VDD=3V,	-	-	70	uA
Standby Current (STOP)	I_{OP3}	LCD OFF, VDD=3V	-	-	1	uA
LCD supply current (No load)	I_{LCD}	LCD ON, All SEG ON, VDD=3V	-	30	40	uA
Input Low Voltage	V_{IL}	All Input Pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All Input Pins	0.7V_{DD}	-	V_{DD}	V
Input Current BP0, BP1, BP2	I_{IN}	VIN = 0V	-5	-	-15	μA
Input Current /RESET	I_{IN1}	VIN = 0V	-15	-	-45	μA
Output Current BP0	I_{OL1}	VDD = 3V, VOUT = 0.4V	8	12	-	mA
	I_{OH1}	VDD = 3V, VOUT = 2.6V	-4	-6	-	mA
	I_{OL1}	VDD = 4.5V,VOUT = 1.0V	-	25	-	mA
	I_{OH1}	VDD = 4.5V,VOUT = 2.6V	-	-12	-	mA
Output Current BP1, BP2	I_{OL2}	VDD = 3V, VOUT = 0.4V	4	8	-	mA
	I_{OH2}	VDD = 3V, VOUT = 2.6V	-4	-6	-	mA
Output Current LCDOP0	I_{OL3}	VDD = 3V, VOUT = 0.4V	-300	-	-	μA

DC Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Current PWM+ / PWM-[6]	I_{OL1}	RLOAD=8 Ohm, Connection: [SPK+]----[R]----[SPK-]	+200	-	-	mA
	I_{OH1}		-200	-	-	mA
DAC full scale current	I_{DAC}	RL = 100Ω	-2.4 -4.0	-3.0 -5.0	-3.6 -6.0	mA
COM/SEG on resister	Ron	IOH=+/- 50uA	-	5	10	KΩ
V2 Pad Output Voltage	V_{RR}	Depended on LCDM4	0.7	-	1.45	V
V2 Pad Output Deviation [7]	V_{D1}	No Load	-	-	± 5	%
V2 Pad Voltage Step	V_{R2}	V2 increased 1 level	-	50	-	mV
V2 input voltage	V_{EXT}	LCDMC1.5 = 1	0.7	-	1.45	V
V6 Pad Output Voltage [4] (LCD's VLCD depends on LCDMC0 register)	V_{LCD}	1/4 Bias & no load	3.9 *V2	-	4 *V2	V
	V_{LCD}	1/5 Bias & no load	4.8 *V2	-	4.95 *V2	V
LVD operating current	I_{LVD}		-	10	20	uA
LVD tolerance of threshold voltage	V_{D2}			-	± 7	%
LVR operating current	I_{LVR}		-	5	10	uA

[6] PWM current deviation will be ±20%.

[7] Deviation is governed by LCD dot size. Larger LCD dots get larger deviations

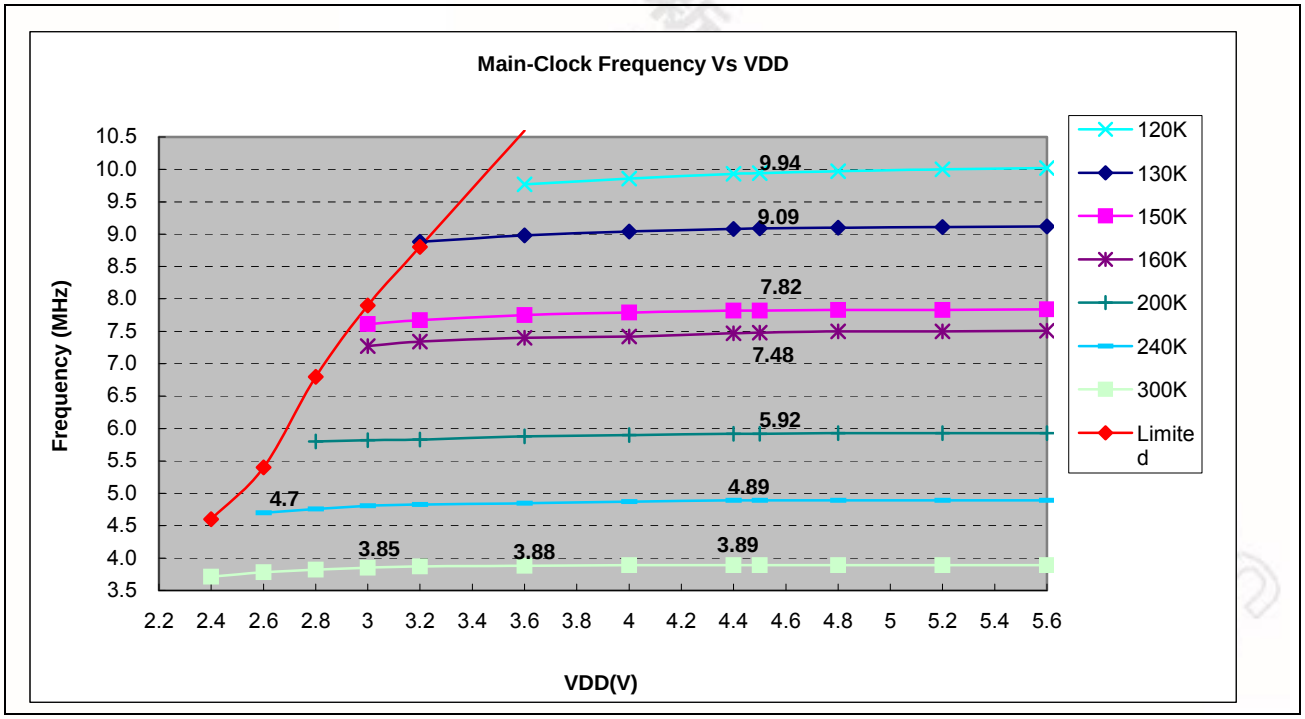
5.3 AC CHARATERISTICS

(VDD–VSS = 3.0V, No load, FM = 4 MHz with Ring mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C, STN LCD on with dot size 0.5mm*0.5mm; unless otherwise specified)

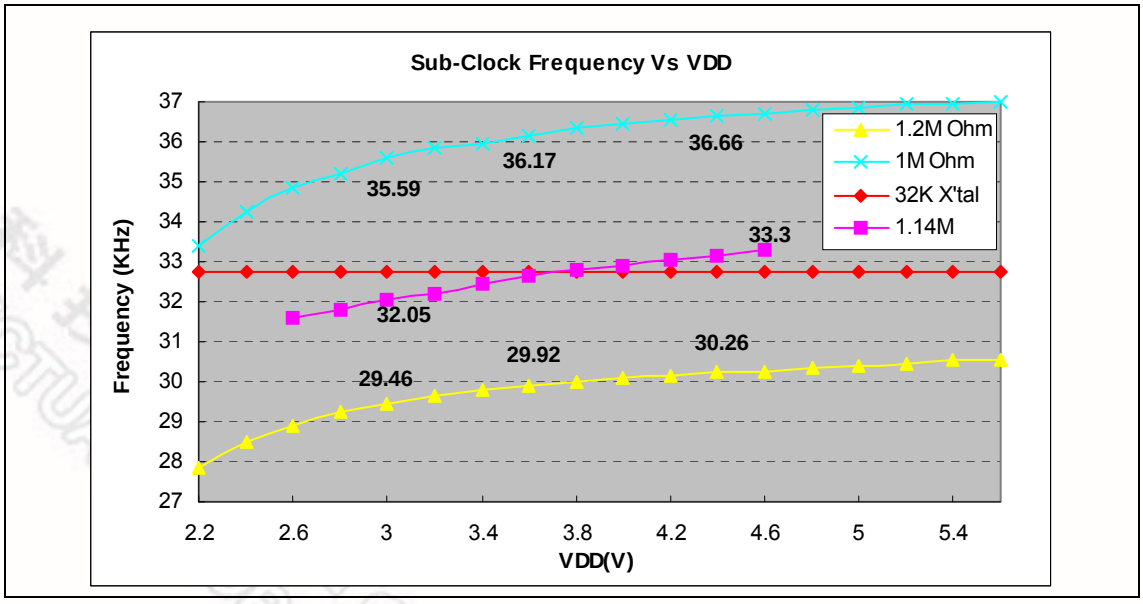
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-clock Frequency	F_{SUB}	Crystal type and X32I and X32O.	-	32768	-	Hz
Main-clock Frequency	F_M	Ring type/Crystal type	-	-	8M	Hz
Chip Operation Frequency	F_{OSC}	CLCK.0=0,F_{SYS}=F_{SUB}	-	32768		Hz
		CLCK.0=1,F_{SYS}= F_{MAIN}	-	-	8M	
Cycle Time	T_{CYC}	F_{SYS} = 4 MHz	250	-	DC	nS
Reset Active Width	T_{RAW}	F_{OSC} = 32.768 KHz	1	-	-	μS
Interrupt Active Width	T_{IAW}	F_{OSC} = 32.768 KHz	1	-	-	μS
Main clock Ring frequency[8]	F_{ROSC}	Rosc =300KΩ	-	4M	-	Hz
		Rosc =200KΩ	-	6M	-	
		Rosc =150KΩ	-	8M	-	
Sub-Clock RC Oscillator	F_{RSUB}	R_{SUB}=1.1MΩ		32		KHz
Sub-Clock Oscillation Stable Time @ Cold Start	F_{STOP}	R_{SUB}=1.1MΩ	0.8	-	1	S
Frequency Deviation of main-clock F_m = 4 MHz	$\frac{\Delta f}{f}$	$\frac{F(3.6V)-F(2.4V)}{F(3.6V)}$	-	3	5	%
Frequency Deviation of main-clock F_m = 6 MHz	$\frac{\Delta f}{f}$	$\frac{F(3.6V)-F(2.4V)}{F(3.6V)}$	-	5	10	%
Frequency Deviation of main-clock F_m =4 ~8MHz	$\frac{\Delta f}{f}$	$\frac{F(5.5V)-F(3.6V)}{F(3.6V)}$	-	3	5	%
Frequency Deviation of F_{RSUB} = 32768Hz	$\frac{\Delta f}{f}$	$\frac{F(3.6V)-F(2.4V)}{F(3.6V)}$	-	5	10	%
Frequency Deviation of F_{RSUB} = 32768Hz	$\frac{\Delta f}{f}$	$\frac{F(5.5V)-F(3.6V)}{F(3.6V)}$	-	3	5	%
Frame frequency	F_{LCD}	LCDMC1=03H (default)	-	64		Hz

[8] The deviation will be +10% while VDD drops from 5.5V to 2.4V based on same resistor

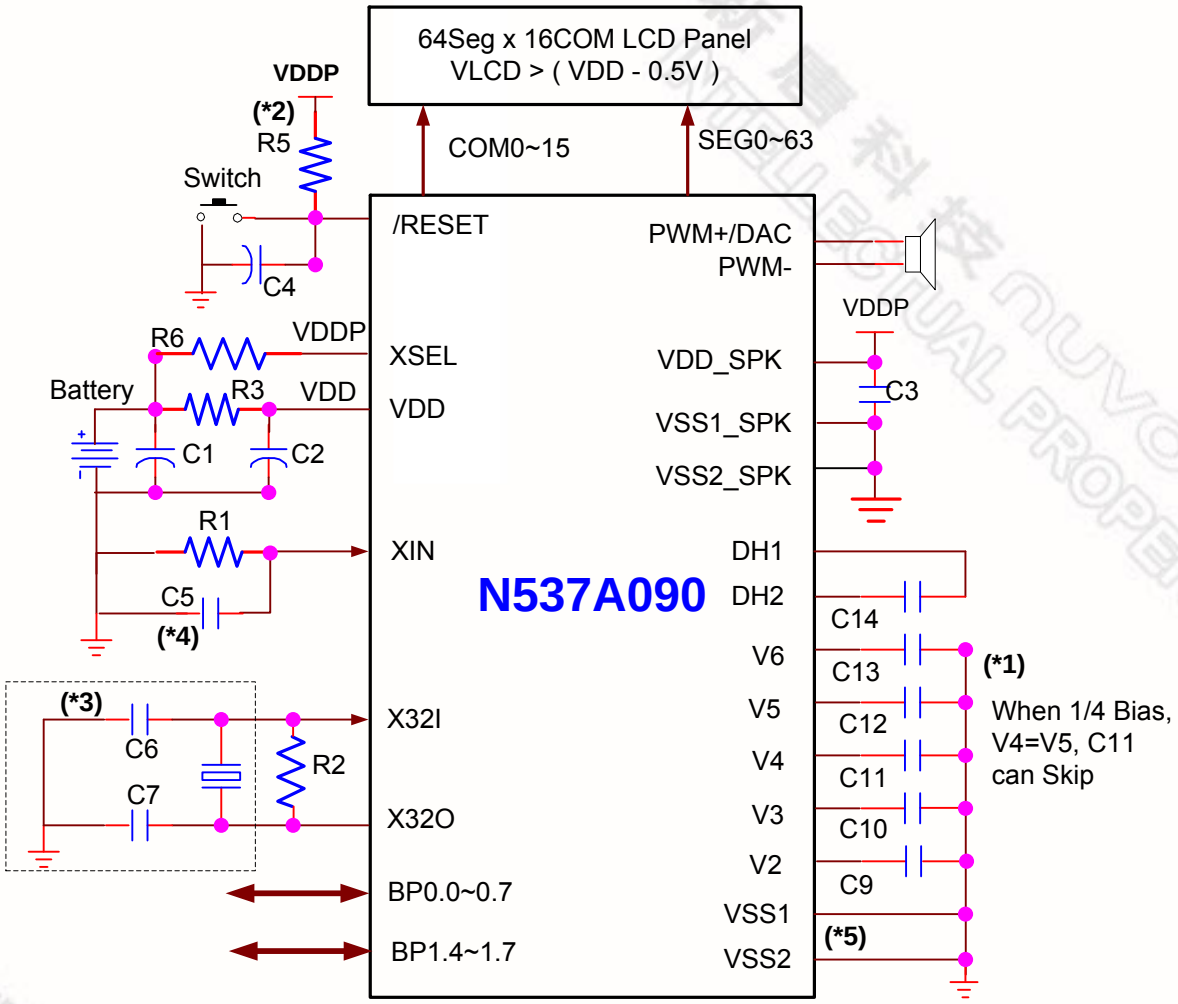
5.4 MAIN-CLOCK OSCILLATION FREQ VS. RESISTOR



5.5 SUB-CLOCK OSCILLATION FREQ VS. RESISTOR



6. TYPICAL APPLICATION CIRCUIT



COMPONENT	C1	C2~C4	C5	C9~C14	R1	R2	R3	R4	R6
Value	4.7uF	0.1uF	100pF	0.1~1uF	300KΩ/4MHz 200KΩ/6MHz 150KΩ/8MHz	1.1 MΩ	1 ~ 10 Ω	470 ~560Ω	1KΩ

Note:

1. C9~C14 depends on LCD panel dot size.
2. Optional R5 equals 100Ω if high noise immunity is needed.
3. For register Sub oscillator selection application.
4. Depending on the mask ROM version (e.g., demo, mass production, …), C5 can be skipped.
5. To be sure chip operation properly, please bond VDD_SPK and VDD together, bond VSS1_SPK, VSS2_SPK and VSS together; and connect VSS as closely as possible to battery ground.
6. Main clock with Ring type, the frequency deviation depends on VDD and the resistor value

7. REVISION HISTORY

Version	Date	Description
A1	Feb. 2, 2012	● Review with Engineering data, remove 10MHz of main freq.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.