

Table of Contents

1.	GENERAL DESCRIPTION.....	2
2.	FEATURES	3
3.	PIN DESCRIPTION.....	5
4.	BLOCK DIAGRAM	6
5.	ELECTRICAL CHARACTERISTICS	7
5.1	Absolute Maximum Ratings	7
5.2	DC Characteristics	7
5.3	AC Characteristics	8
6.	TYPICAL APPLICATION CIRCUITS.....	9
7.	REVISION HISTORY	10

1. GENERAL DESCRIPTION

The N567K081 is a powerful microcontroller (uC) dedicated to speech and melody synthesis applications. With the help of the embedded 8-bit microprocessor & dedicated H/W, the N567K081 can synthesize 6-channel speech & melody simultaneously.

The two channels of synthesized speech can be in different kinds of format, for example ADPCM and MDPCM. The N567K081 can provide 6-channel high-quality wavetable melody, which can emulate the characteristics of musical instruments, such as piano and violin. More colorful melody effects are implemented in N567K081 series, such as modulation, vibrato, and pitch-bending etc. The output of speech/melody channels are mixed together through the on-chip digital mixer to produce colorful effects. With these hardware resources, the N567K081 is very suitable for high-quality and sophisticated scenario applications.

The N567K081 provides 254KB ROM, 24 I/O pins, 384 bytes RAM, IR Tx carrier, Serial Interface Manager (SIM), and S/W libraries to meet requirements from sophisticated applications like interactive toys and educational applications. The N567K081 provides PWM mode audio output to save power during playback and Watch Dog Timer to prevent from code runaway conditions.

Furthermore, the N567K081 enhances system ESD contact immunity, builds in LDO to drive SpiFlash directly, and provides LVD and LVR options. It also has bandgap reference inside to control deviation w.r.t. temperature within +/-3% for voltage references over 0C ~ 70C.

2. FEATURES

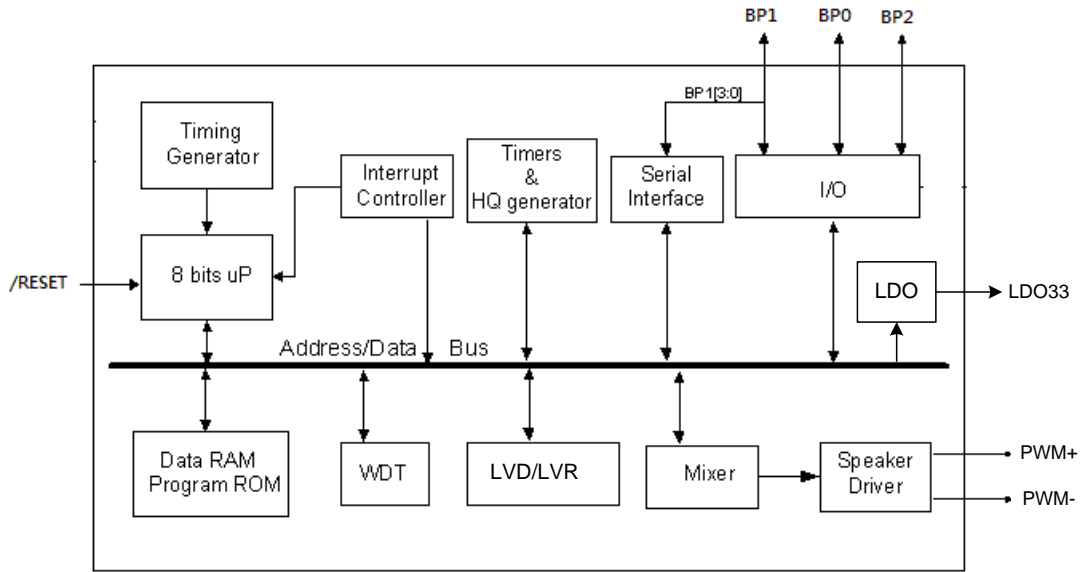
- Wide range of operating voltage:
 - 8 MHz @ 3.0 volt ~ 5.5 volt
 - 6 MHz @ 2.4 volt ~ 5.5 volt
- ROM size: 254KB
- Oscillator
 - Built-in OSC with trim, +/-3%
 - System clock setting via mask option: 4MHz, 6MHz, or 8MHz
- Power management:
 - 4 ~ 8 MHz system clocks, with trim (Ring oscillator).
 - Stop mode for stopping all IC operations
 - ◆ Status changes of the BP0 ~ BP2 pins can wake up the chip
- Provide patented Serial Interface Management (SIM) H/W to access the external memory
 - SpiFlash / SpiROM
 - 65C02 instruction as well as speech/MIDI data could be stored @ external memory
- Provide four levels of LVD options via register control
 - 2.4V, 2.75V, 2.9V, 3.3V @ +/-3% deviation.
- Built-in Low Voltage Reset (LVR) by mask option
 - 2.0V, 2.2V, 2.4V, 2.6V @ +/-5% tolerance
- Built-in bandgap voltage reference to control deviation w.r.t. temperature
 - +/-3% over 0°C ~ 70°C
- Enhance system contact ESD immunity for 8 x I/O pins (BP00 ~ BP03, BP04 ~ BP07) and VDD_BP0, VSS_BP0.
 - No auto-reset @ $\leq 3KV$, with external series resistor
 - No damage, no hang-up @ $\leq 5KV$, with external series resistor
- LDO (3.3V, On/Off control) with overload protection to drive SPI Flash directly
- Built-in TimerG1 for general purpose applications
- Built-in Watch-Dog Timer (WDT)
- Provides up to 24 I/O pins
- Built-in IR carrier generation circuit for simplifying firmware IR application
- Audio output : 1 speaker output, mono effect
 - PWM: direct drive speaker to save power @ 12 bit resolution with Noise Shaping
- F/W speech synthesis:
 - Multiple format parser that supports
 - ◆ New 4-bit MDPCM (NM4), 5-bit MDPCM (MDM), 4-bit MDPCM (MD4), 4-bit ADPCM (APM), 8-bit Log PCM (LP8) algorithms
- Wavetable MIDI synthesis:
 - 6 melody channels that can emulate characteristics of musical instruments
 - Multi-MIDI files simultaneous
 - Multi-MIDI channels dynamic control
 - Various basic MIDI events are supported for colorful melody playback, such as modulation wheel, pitch-bending, pedal, pitch-shift, and vibrato...etc.
- Speech and melody can be played back at the same time

- 2 channels speech + 4 channels wavetable melody
- 1 channel speech + 5 channels wavetable melody
- 6 channels wavetable melody
- Harmonized synchronization among MIDI, Speech, LED, and Motor
- Support **PowerScript™** for developing codes easily
- Full-fledged development system
 - Source-level ICE debugger (Assembly & **PowerScript™** format)
 - **Ultra I/O™** tool for event synchronization mechanism
 - ICE system with USB port
 - User-friendly GUI environment
- Package form: COB.

3. PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
/RESET	In	IC reset input with an internal pull-up resistor, low active.
BP00~BP07	I/O	General input/output pins. When used as output pin, it can be open-drain or CMOS type and it can sink 25mA for high-current applications. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When BP07 is used as output pin, it can be the IR transmission carrier for IR applications. ESD enhanced port, which uses VDD_BP0 and VSS_BP0 accordingly.
BP10~BP17	I/O	General input/output pins. When used as output pin, it can be open-drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When serial interface management (SIM) is enabled, and set memory type as SPI flash, BP10 ~ BP13 are used to be an interface.
BP20~BP27	I/O	General input/output pins. When used as output pin, it can be open-drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode
PWM+	O	PWM driver positive output
PWM-	O	PWM driver negative output
VDD	Power	Positive power supply for uC, peripherals and BP20 ~ BP27, BP14 ~ BP17.
VSS	Power	Negative power supply for uC, peripherals and I/O ports.
VDD_OSC	Power	Positive power supply for oscillator.
VDD_SPK	Power	Positive power supply for speaker driver.
VSS_SPK	Power	Negative power supply for speaker driver.
VDD_BP0	Power	Positive power supply for BP00 ~ BP07.
VSS_BP0	Power	Negative power supply for BP00 ~ BP07.
VDD_SIM	Power	Positive power supply for serial interface Management (SIM) BP10 ~ BP13 For non-SIM application, it should be connect to V _{DD} to keep normal standby current.
LDO33	Power	3.3V regulator output. Connect an external 1uF cap. to VSS.
TEST1~TEST2	-	Internal TEST pins, do not bond or connect.

4. BLOCK DIAGRAM



5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
D.C. Voltage on Any Pin to Ground Potential	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 DC Characteristics

($V_{DD} - V_{SS} = 4.5\text{ V}$, $F_M = 8\text{ MHz}$, $T_a = 25^\circ\text{C}$, No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Operating Voltage	V_{DD}	$F_{SYS} = 6\text{ MHz}$	2.4	-	5.5	V
		$F_{SYS} = 8\text{ MHz}$	3.0	-	5.5	V
Operating Current	I_{OP}	$F_{SYS} = 8\text{ MHz}$, normal operation	-	8	12	mA
Standby Current	I_{SB}	STOP mode	-	1	2	μA
Input Low Voltage	V_{IL}	All input pins	V_{SS}	-	$0.3 V_{DD}$	V
Input High Voltage	V_{IH}	All input pins	$0.7 V_{DD}$	-	V_{DD}	V
Input Current I/O pins	I_{IN1}	$V_{IN} = 0\text{V}$, pulled-high resistor = 500k ohm	-5	-9	-14	μA
Input Current I/O pins	I_{IN2}	$V_{IN} = 0\text{V}$, pulled-high resistor = 150k ohm	-15	-30	-45	μA
Output Current (BP0)	I_{OL}	$V_{DD} = 3\text{V}$, $V_{OUT} = 0.4\text{V}$	8	12	-	mA
	I_{OH}	$V_{DD} = 3\text{V}$, $V_{OUT} = 2.6\text{V}$	-4	-8	-	mA
	I_{OL}	$V_{DD} = 4.5\text{V}$, $V_{OUT} = 1.0\text{V}$	-	35	-	mA
	I_{OH}	$V_{DD} = 4.5\text{V}$, $V_{OUT} = 3.5\text{V}$	-	-20	-	mA
Output Current (BP1, BP2)	I_{OL}	$V_{DD} = 3\text{V}$, $V_{OUT} = 0.4\text{V}$	4	6	-	mA
	I_{OH}	$V_{DD} = 3\text{V}$, $V_{OUT} = 2.6\text{V}$	-4	-8	-	mA
	I_{OL}	$V_{DD} = 4.5\text{V}$, $V_{OUT} = 1.0\text{V}$	-	15	-	mA
	I_{OH}	$V_{DD} = 4.5\text{V}$, $V_{OUT} = 3.5\text{V}$	-	-20	-	mA
Output Current PWM+ / PWM-	I_{OL1}	$R_L = 8\text{ Ohm}$,	+200	-	-	mA
	I_{OH1}	[PWM+]---[R_L]---[PWM-]	-200	-	-	mA
LDO33 Voltage	V_{LDO}	$V_{DD} = 3.6\text{V} \sim 5.5\text{V}$	3.0	3.3	3.6	V
LDO33 Output Current	I_{LDO}	$V_{DD} = 3.6\text{V} \sim 5.5\text{V}$ V_{LDO} drop 10% with 1 μF		30		mA

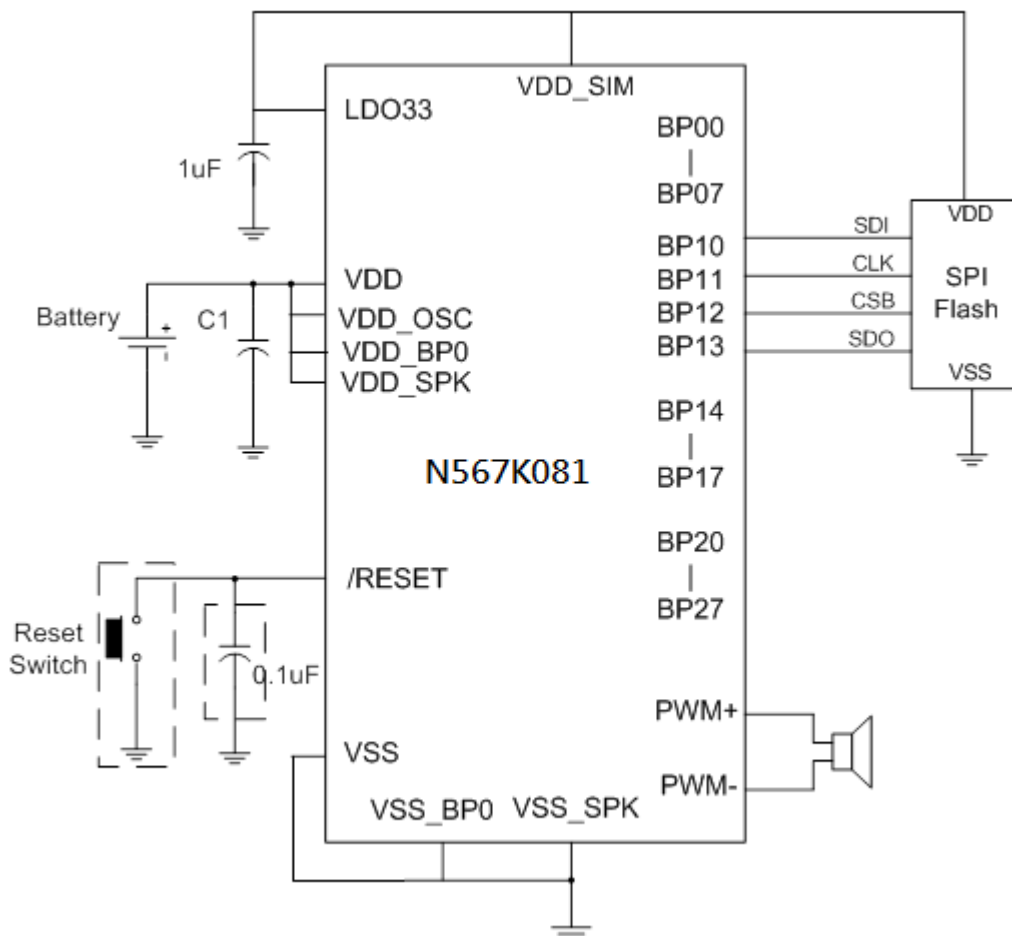
5.3 AC Characteristics

(V_{DD}-V_{SS} = 4.5 V, F_M = 8 MHz, T_a = 25°C; No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Main-Clock	F _M	ROSC built-in, @3.0~5.5V	3973	4096	4218	KHz
		ROSC built-in, @3.0~5.5V	5959	6144	6328	
		ROSC built-in, @3.0~5.5V	7946	8192	8437	
Main-Clock	F _M	ROSC built-in, @2.4~3.6V	3973	4096	4218	KHz
		ROSC built-in, @2.4~3.6V	5959	6144	6328	
Main-Clock Wake-up Stable Time	T _{WSM}	2 ¹³ clock cycle	1		2	mS

6. TYPICAL APPLICATION CIRCUITS

(a) Application Circuit



Notes:

1. Rosc is built in N567K081 internally
2. The C1 value is suggested 4.7uF for audio PWM output
3. The VDD_SIM pad must be connected to VDD for non-SIM application
4. The above application circuits are for reference only. No warranty for mass production

(b) PCB layout guide

1. The IC substrate should be connected to VSS in PCB layout. But VSS_SPK can't connect with IC substrate directly. Both VSS and VSS_SPK tie together in battery negative power.
2. Each VDD, VDD_OSC, VDD_BP0, VDD_SIM and VDD_SPK pad must connect to positive power to support stable voltage for individual function work successfully. (Don't let them floating)

7. REVISION HISTORY

VERSION	DATE	REASONS FOR CHANGE	PAGE
A0.1	June 2014	Preliminary release.	All
A1.0	Oct. 2014	Official version establishment	
A1.1	Nov. 2014	Update ROM size as 254KB	2~3
A1.3	Dec. 2014	Update FEATURES, PIN DESCRIPTION	3~5
		Add LDO33 DC Characteristic	7
A1.4	Jan. 2015	Update the description of ESD immunity	3
		Correct wake-up stable time in AC Characteristic	8
A1.5	Jul. 20.2015	Revise LVD level	3

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