N572F064/F065

Data Sheet

32-BIT MULTI-ALGORITHM VOICE PROCESSOR (NuVoice™)

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1. GENERAL DESCRIPTION

The N572 is the first Cortex™-M0 based processor for voice process applications, running up to 48MHz and equipped with 64KB flash and 8KB SRAM for high performance process of audio and voice algorithms. Integrating rich analog peripherals, like pre-amplifier, ADC, DAC, hardware mixer, and PA, this chip saves a lot of system design effort and cost. An USB device and flash work together to provide updatable content and scenario downloaded from internet via a PC.

To utilize the high performance M0 and high density of SRAM, advanced algorithms are designed, optimized, and tested in N572 chip. These algorithms include watermark, voice changer, NuSound, NuOne, beat detection, and more in developing. In additional to algorithms developed by ourselves, Nuvoton also seeks third parties for more interesting software to enrich the applications on N572. Additionally, the new designed NVIC in M0, the latency of interrupt and response to external events are faster. Multiple algorithms could be run together smoothly and naturally.

The development tools are based on Keil™ MDK using C/C++ for programming language. This is a robust and easy to use environment for development and debug.

Following is table of Part No. of N572F064 and N572F065:

Part No.	N572F065	N572F064
Program	64KB Flash	
SRAM	8KB	
CPU freq	48MHz	
USB	FS/12Mbps	NA

2. FEATURES

- **Core**
  - ARM® Cortex™-M0 core runs up to 48MHz
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 16 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- **Widely operating voltage range from 2.4V to 5.5V**
- **Flash EPROM Memory**
  - 64KB Flash EPROM
  - Support ISP for Flash update
  - 512 bytes page erase for Flash
  - Support 2-wire ICP update from ICE interface
  - Support fast parallel programming mode by external programmer
  - Security Lock preventing content in Flash access from external interface
- **SRAM Memory**
  - 8KB embedded SRAM
- **Clock Control**
  - Flexible selection for different applications

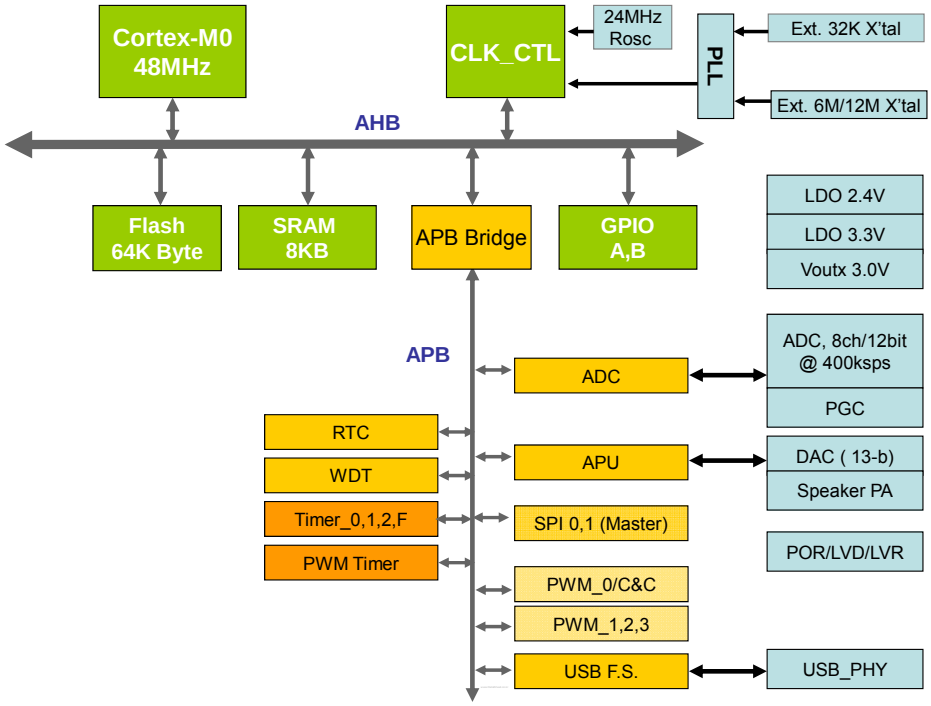
- Support PLL, up to 48MHz, for high performance system operation
- External 12MHz(or 6MHz) crystal input for USB and precise timing operating mode
- External 32KHz crystal input for RTC function and system clock
- Internal 24MHz RC oscillator

- **GPIO**
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- **Timers**
  - 3 sets of the timer with 8-bit pre-scaler and 16-bit timer.
  - Counter auto reload.
  - IR carrier generator
  - One fixed frequency timer
- **Watch Dog Timer**
  - Default ON/OFF by configuration setting
  - Multiple clock sources
  - 8 selectable time out period from 6ms ~ 3.0sec (depends on clock source)
  - Able to wake up power down/sleep
  - Interrupt or reset selectable on watchdog time-out
- **RTC**
  - Support time out interrupt
  - Support wake up function
- **PWM/Capture/Compare Timer**
  - one 16-bit timer and four 16-bit comparators
  - Four clock selectors
  - One 8-bit pre-scaler and one clock divider
  - Two Dead-Zone generators
  - Programmable duty control of output waveform
  - Auto reload mode or one-shot pulse mode
  - Capture and compare function
- **SPI**
  - Two sets of SPI device
  - Master mode up to 24MHz on system runs on 48MHz
  - Support MICROWIRE/SPI master mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines
  - Two 32-bit buffers
- **USB 2.0 Full-Speed Device**
  - One set of USB 2.0 FS Device 12Mbps

- On-chip USB Transceiver
- Provide 1 interrupt source with 4 interrupt events
- Support Control, Bulk In/Out, Interrupt and Isochronous transfers
- Auto suspend function when no bus signaling for 3 ms
- Provide 6 programmable endpoints
- Include 512 Bytes internal SRAM as USB buffer
- Provide remote wakeup capability

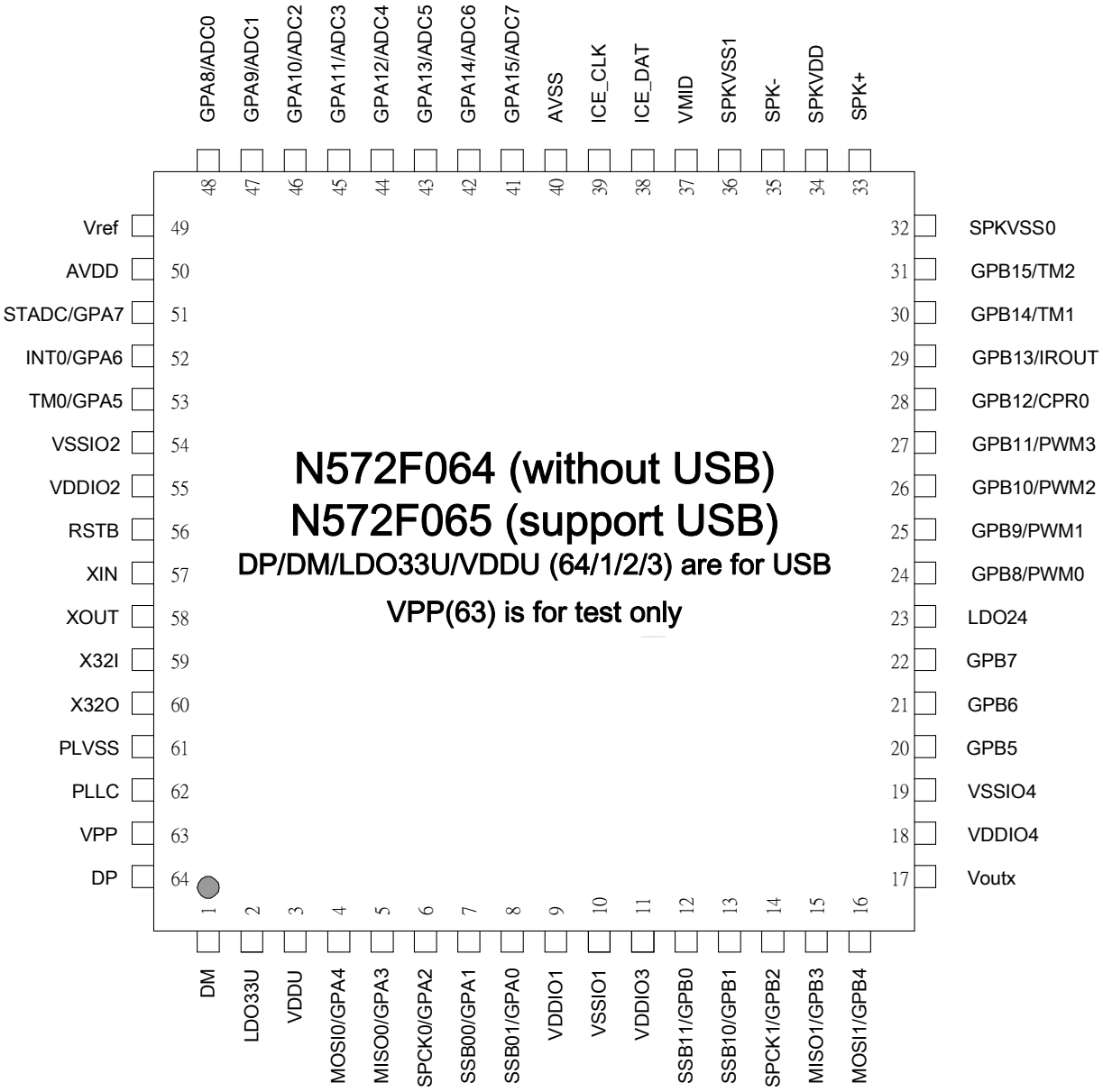
- **ADC**
  - 8-ch 12-bit with 200Ksps
  - Single scan/single cycle scan/continuous scan
  - 8 channels share 8 result registers
  - Programmable channel scan sequence
  - Threshold voltage detection
  - Conversion start by S/W, external pins
  - Programmable gain control for sound record
- **APU**
  - 13-bit DAC
  - H/W mixer with 2 channel PCM input
  - Embedded power amplifier
  - 7-level volume control
- **Voltage detector**
  - with 2 levels: 3.0V/2.7V
- **LDO**
  - Built-in 2.4V LDO for internal core
  - Built-in 3.3V LDO for USB
- **Voltage Output**
  - Built-in power supply Voutx for driving external spi-flash
- **Low Voltage Reset**
- **Operating Temperature: -20℃~85℃**
- **Packages:**
  - All Green package (RoHS)
  - 7mmx7mm LQFP 64-pin

3. FUNCTIONAL BLOCK DIAGRAM



4. PIN CONFIGURATION

4.1 Pin Diagram



Note1: VPP is for embedded flash test, keep it no connection in general application.
Note2: N572F064 does not support USB function, keep (DP/DM/LDO33U/VDDU) no connection.

4.2 Pad Description

NAME	TYPE	DESCRIPTION
1. GPIO		
GPA0 ~ GPA15	I/O	Bidirectional general purpose I/O ports. Most of these pins have alternate function, refer to section 4.3 for detail.
GPB0 ~ GPB15	I/O	Bidirectional general purpose I/O ports. Most of these pins have alternate function, refer to section 4.3 for detail.
2. Oscillator		
X32I	I	32KHz crystal input
X32O	O	32KHz crystal output
XIN	I	6MHz or 12MHz crystal input
XOUT	O	6MHz or 12MHz crystal output
PLVSS	P	PLL ground
PLLC	A	Capacitor connection for built-in PLL1
3. USB		
DP	I/O	USB data pin, DP.
DM	I/O	USB data pin, DM.
LDO33U	P	3.3V LDO output for USB
VDDU	P	USB bus power supply, floating detect input
4. ADC		
VDDA	P	Analog power supply
VSSA	P	Analog ground.
Vref	A	Reference voltage input
5. Speaker Driver		
SPK+/DAC	O	Speaker positive output pin, or current type DAC output.
SPK-	O	Speaker negative output pin.
SPKVDD	P	Analog power supply
SPKVSS1	P	Analog ground.
SPKVSS0	P	Analog ground.

NAME	TYPE	DESCRIPTION
VMID	A	Connect a capacitor to SPKVSS
6. Power		
VDDIO4	P	Power supply for I/O port, and source of LDO for logic circuit.
VSSIO4	P	Ground pin, connect to 0V.
VDDIO2	P	Power supply for I/O port, and source of oscillator.
VSSIO2	P	Ground pin, connect to 0V.
VDDIO1	P	Power supply for I/O port.
VSSIO1	P	Ground pin, connect to 0V.
VDDIO3	P	Power supply for I/O port.
LDO24	P	2.4V LDO output
Voutx	P	3.0V output for driving out
VPP	P	For embedded flash test, keep it no connection in general application.
7. SWD		
ICE_CLK	I	Serial Wired Debugger Clock pin
ICE_DAT	I/O	Serial Wired Debugger Data pin
8. Other		
RSTB	I	Reset input pin, low active. Internal pull-high.

4.3 Alternate Function List of GPIO

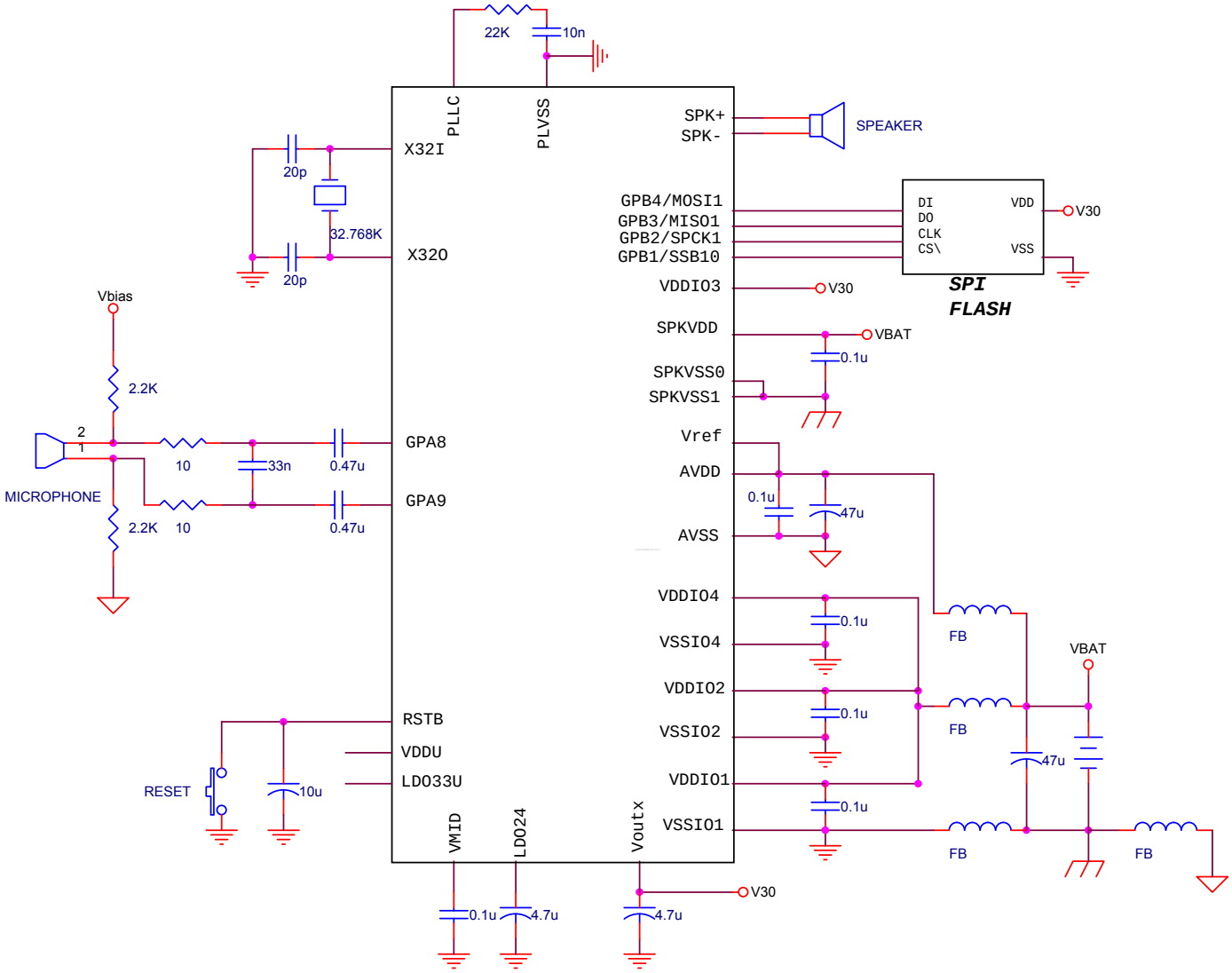
GPIO	POWER	ALTERNATE	I/O OF ALTERNATE	FUNCTION DESCRIPTION
GPA0	VDDIO1	SSB01	O	SPI0 2nd chip select pin
GPA1	VDDIO1	SSB00	O	SPI0 1st chip select pin
GPA2	VDDIO1	SPCK0	O	SPI0 serial clock output
GPA3	VDDIO1	MISO0	I	SPI0 master data input
GPA4	VDDIO1	MOSI0	O	SPI0 master data output
GPA5	VDDIO2	TM0	I	Timer0 counter external input
GPA6	VDDIO2	INT0	I	External interrupt input pin
GPA7	VDDIO2	STADC	I	ADC external trigger input
GPA8	VDDIO2	ADC0	A	ADC analog input 0
GPA9	VDDIO2	ADC1	A	ADC analog input 1
GPA10	VDDIO2	ADC2	A	ADC analog input 2
GPA11	VDDIO2	ADC3	A	ADC analog input 3
GPA12	VDDIO2	ADC4	A	ADC analog input 4
GPA13	VDDIO2	ADC5	A	ADC analog input 5
GPA14	VDDIO2	ADC6	A	ADC analog input 6
GPA15	VDDIO2	ADC7	A	ADC analog input 7
GPB0	VDDIO3	SSB11	O	SPI1 2nd chip select pin
GPB1	VDDIO3	SSB10	O	SPI1 1st chip select pin
GPB2	VDDIO3	SPCK1	O	SPI1 serial clock output
GPB3	VDDIO3	MISO1	I	SPI1 master data input
GPB4	VDDIO3	MOSI1	O	SPI1 master data output
GPB5	VDDIO4	-		
GPB6	VDDIO4	-		
GPB7	VDDIO4	-		
GPB8	VDDIO4	PWM0	O	PWM output pin 0
GPB9	VDDIO4	PWM1	O	PWM output pin 1

GPIO	POWER	ALTERNATE	I/O OF ALTERNATE	FUNCTION DESCRIPTION
GPB10	VDDIO4	PWM2	O	PWM output pin 2
GPB11	VDDIO4	PWM3	O	PWM output pin 3
GPB12	VDDIO4	CPR0	I	Capture input
GPB13	VDDIO4	IROUT	O	IR carrier output
GPB14	VDDIO4	TM1	I	Timer1 counter external input
GPB15	VDDIO4	TM2	I	Timer2 counter external input

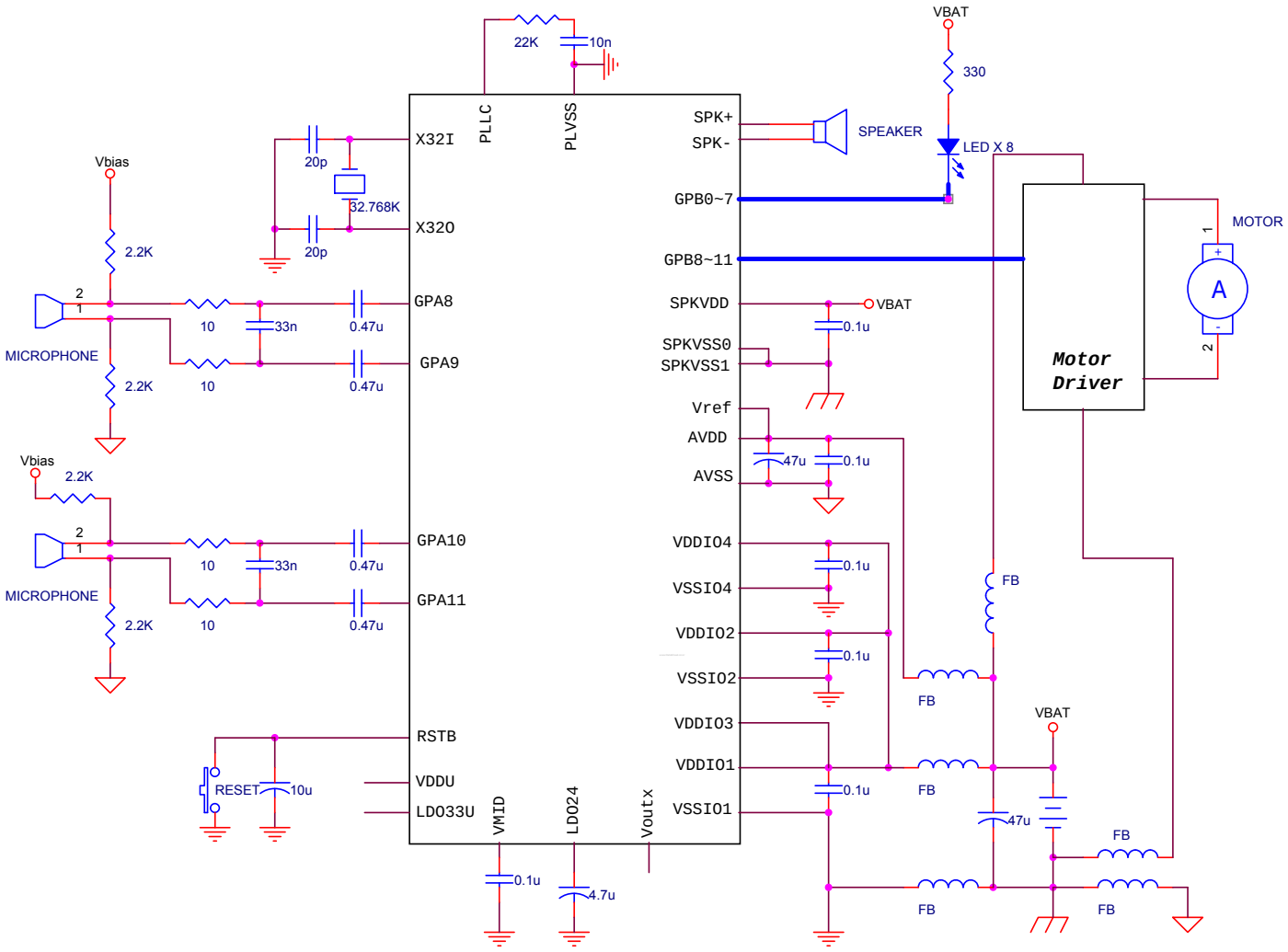
I: Input, O: Output, A: Analog input

5. TYPICAL APPLICATION CIRCUIT

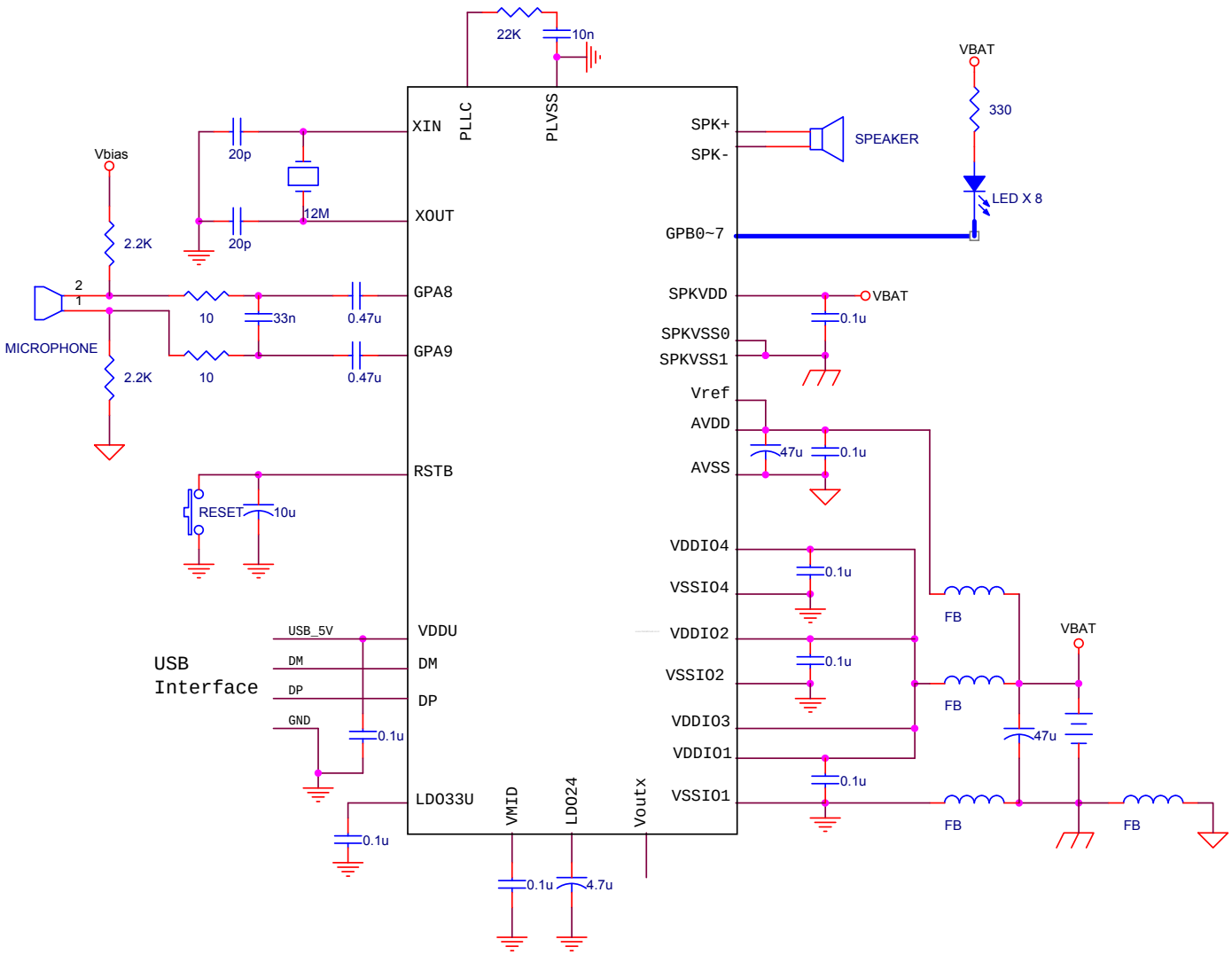
5.1 Recording and Playback



5.2 Dual microphones for sound direction detection and motor control



5.3 USB updateable program and data



6. SOFTWARE AND DEVELOPMENT ENVIRONMENT

The Keil™ MDK 4.0 (or above version) including IDE, compiler, linker, and debugger is for your software development. Debug hardware requires Nu-Link™ and N572 EVB. A Nu-Link driver is required to add views of peripherals and add-ons within MDK's IDE. With software library, you can development and debug in the MDK4.0 environment. Please refer to Programming Guide for details.

7. DC ELECTRICAL CHARACTERISTICS

7.1 DC Electrical Characteristics

PARAMETER	SYM	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.4		5.5	V	
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		V_{DD}	V	
Operating Current at Normal Run Mode	I_{DD1}		50		mA	V_{DD}=5.5V@48MHz, enable all IPs
	I_{DD3}		42		mA	V_{DD}=3V@48MHz, enable all IPs
Operating Current at Idle Mode	I_{IDLE2}		17		mA	V_{DD}=5.5V@48MHz, disable all IPs
	I_{IDLE4}		15		mA	V_{DD}=3V@48MHz, disable all IP
Operating Current at Power-down Mode	I_{PWD1}		10		μA	V_{DD} = 5.5V, No load, disable LVD
	I_{PWD2}		9		μA	V_{DD} = 3.3V, No load, disable LVD
Input Current GPA/GPB	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at RSTB [1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current GPA/GPB	I_{LK}	-0.1	-	+0.1	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Input Low Voltage GPIO (TTL input)	V_{IL1}	-0.3	-	1.0	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.4V
Input High Voltage GPIO (TTL input)	V_{IH1}	2.2	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0V
Source Current GPA/GPB (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90		V_{DD} = 2.7V, V_S = 2.2V
	I_{SR13}	-40	-60	-80		V_{DD} = 2.5V, V_S = 2.0V
Source Current GPA/GPB (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 3.0V
	I_{SR22}	-4	-6	-8		V_{DD} = 2.7V, V_S = 2.2V
	I_{SR23}	-3	-5	-7		V_{DD} = 2.5V, V_S = 2.0V
Sink Current GPA/GPB (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK2}	7	10	13		V_{DD} = 2.7V, V_S = 0.45V
	I_{SK3}	6	9	12		V_{DD} = 2.5V, V_S = 0.45V

Notes: 1. RSTB pin is a Schmitt trigger input.

7.2 AC Electrical Characteristics

7.2.1 Internal 24MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage V_{DD}		2.2	2.4	2.7	V
Center Frequency			24.0		MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD}=2.5V	-0.6		+0.6	%
	-20°C ~+85°C; V_{DD}=2.2V~2.7V	-5		+5	%
Accuracy of Un-calibrated Internal Oscillator Frequency	-20°C ~+85°C; VDD=2.2V~2.7V	-20		+20	%
Operating current	V_{DD}=2.5V		500		uA

7.3 Analog Characteristics

7.3.1 12-bit SAR ADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	±1	-	LSB
Integral nonlinearity error	INL	-	±1	-	LSB
Offset error	EO	-	±1	-	LSB
Gain error (Transfer gain)	EG	-	1	-	-
Monotonic	-	Guaranteed			-
ADC clock frequency	FADC	-	-	5	MHz
Calibration time	TCAL	-	127	-	Clock
Sample time	TS	-	7	-	Clock
Conversion time	TADC	-	25	-	Clock
Sample rate	FS	-	-	200	Ksps
Supply voltage	VDD	-	2.5	-	V
	VDDA	3	-	5.5	V
Supply current (Avg.)	IDD	-	0.5	-	mA
	I_{DDA}	-	1.5	-	mA
Reference voltage	VREFP	-	VDDA	-	V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Reference current (Avg.)	IREFP	-	1	-	mA
Input voltage range	VIN	0	-	VREFP	V
Capacitance	CIN	-	5	-	pF

7.3.2 Voice Recorder

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	VDDA		3	5	5.5	V
Operation Current	IDD			3.5		mA
Programmable Gain (Gain1)	VOL[4:0]	5-bit Control 5'b11111→46dB 5'b00001→16dB 5'b00000→0dB	16		46	dB
Preamp Gain (Gain2)	PAG[1:0]	2-bit Control 2'b00: -6dB 2'b01: 0dB 2'b10: 8dB 2'b11: 14dB	-6		14	dB
Offset Bit	OS[4:0]	5-bit Control	-32		32	mV
THD				50		dB
SNR		Gain1=14db, Gain2=16db VDDA=4.5V Input 100mV		43		dB

7.3.3 2.4V LDO for Internal Core

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage		2.7	5	5.5	V
Output Voltage		-10%	2.4	+10%	V
	Power Down	-10%	2.0	+10%	V

7.3.4 Voutx for External Driving

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage		3.3	5	5.5	V
Output Voltage		-10%	3.0	+10%	V
	Turn off		floating	-	V
I load				30	mA

7.3.5 Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Threshold voltage	Temperature=25°C	1.7	2.0	2.3	V

7.3.6 Voltage Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Detected Voltage	CVDTV=0		2.7		V
	CVDTV=1		3.0		V

7.3.7 Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-20	25	85	°C
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.3.8 Power Amplifier and DAC

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	SPKVDD	2.4	4.5	5.5	V
Temperature		0	25	70	°C
Output Power	SPKVDD=4.5V, 27°C, 8Ω BTL load, 0dB gain		250		mW
Total Harmonic Distortion	SPKVDD=4.5V, 27°C, 8Ω BTL load, 0dB gain, 250mW		0.5		%
Power Amplifier Gain		-18		0	dB
DAC output current	DACGN=0	2.4	3	3.6	mA
	DACGN=1	4.0	5.0	6.0	
DAC operation Current	SPKVDD=4.5V		5.5		mA
DAC Quiescent Current	SPKVDD=4.5V		100		μA
Power Amplifier Quiescent Current	DAC fine-tuned, SPKVDD=4.5V, 27°C		11		mA
Power Down Current	DAC fine-tuned, SPKVDD=4.5V, 27°C		1		μA
Operation Current	SPKVDD=4.5V, 27°C, 250mW		180		mA

7.3.9 PLL

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	VDD		2.2	2.4	2.7	V
Temperature			-20	25	85	°C
Input Low Voltage	VIL	VDD=2.4V	VSS	--	0.2*VDD	V
Input High Voltage	VIH	VDD=2.4V	0.8*VDD	--	VDD	V
Input Clock Frequency	Fin1		--	32.768	--	KHz
	Fin2		--	6 or 12	--	MHz
Output Clock Frequency	Fout		--	48	--	MHz
Jitter	--	25°C, TT, 2.4V	--		1	nS
Duty Cycle	--	Fout=48MHz	40	50	60	%
Operating Current	Iop	25°C, TT, 2.4V		8		mA
Lock Time		32768Hz to 48MHz		5		mS

7.3.10 USB PHY

7.3.10.1 USB DC Electrical Characteristics

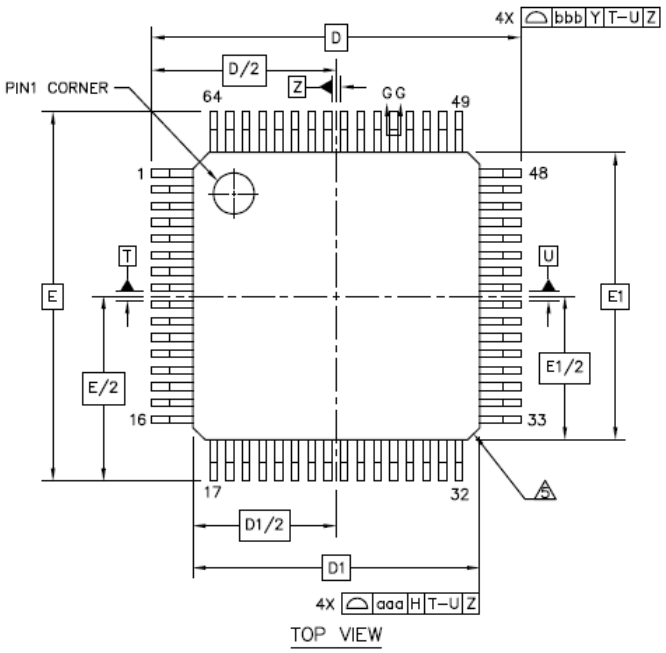
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input high (driven)	V_{IH}		2.0			V
Input low	V_{IL}				0.8	V
Differential input sensitivity	V_{DI}	|DP-DM|	0.2			V
Differential common-mode range	V_{CM}	Include V_{DI} range	0.8		2.5	V
Single-ended receiver threshold	V_{SE}		0.8		2.0	V
Receiver hysteresis	V_{RH}			200		mV
Output low (driven)	V_{OL}		0		0.3	V
Output high (driven)	V_{OH}		2.8		3.6	V
Output signal cross voltage	V_{CRS}		1.3		2.0	V
Pull-up resistor	R_{PU}		1.425		1.575	KΩ
Pull-down resistor	R_{PD}		14.25		15.75	KΩ

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Termination Voltage for upstream port pull up (R_{PU})	V_{TRM}		3.0		3.6	V
Driver output resistance	Z_{DRV}	Steady state drive*		10		Ω
Transceiver capacitance	C_{IN}	Pin to GND			20	pF

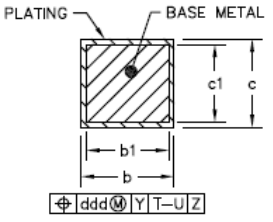
*Driver output resistance doesn't include series resistor resistance.

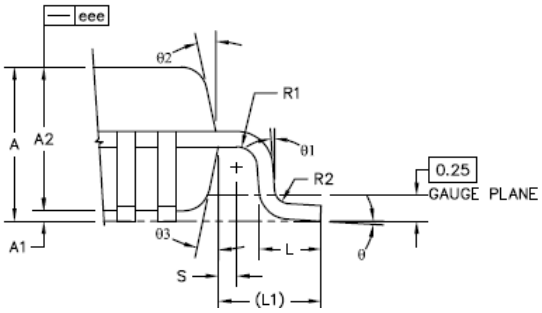
8. PACKAGE INFORMATION

64L LQFP(7x7x1.4mm footprint 2.0mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





9. ORDERING INFORMATION

PART NUMBER	PACKAGE	SPECIAL FEATURE	PB FREE + HALOGEN FREE (GREEN)	RELEASE DATE
N572F064	NA (Die Form)	Without USB	Yes	Available
N572F064G	LQFP 64pin 7mmx7mm	Without USB	Yes	Available
N572F065	NA (Die Form)	With USB	Yes	Available
N572F065G	LQFP 64pin 7mmx7mm	With USB	Yes	Available

10. REVISION HISTORY

Version	Date	Description
A7	Jan 2012	● Add description for VPP & USB related pins/pads (4). ● Add Voutx I load information (7.3.4). ● Add package information (8).
A6	Aug 2011	● Fix the output value of Voutx in Analog Characteristics (7.3.4). ● Sync ADC performance to 200K sps (2 & 7.3.1). ● Change LDO30E to Voutx (4.1) and revise AP circuits (5). ● Update importance notice.
A5	Dec 2010	● Fix the typo of LDO 3.3V, add Voutx in Block Diagram
A4	Oct 2010	● Adjust the part no.
A3	Aug 2010	● Remove Preliminary, add security lock, add part no.
A2	Jun 2010	● Add DC/AC/Analog characteristics
A1	May 2010	● With algorithms and partial DC characteristics
A0	Apr 2010	● Preliminary draft

Important Notice

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All Insecure Usage shall be made at customer’s risk, and in the event that third parties lay claims to Nuvoton as a result of customer’s Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.