NuVoice®

N575C145

Datasheet

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1 GENERAL DESCRIPTION

The N575C145 is a system-on-chip product optimized for low power, audio record and playback with an embedded ARM® Cortex™-M0 32-bit microcontroller core.

The N575C145 embeds a Cortex™-M0 core running up to 50 MHz with 145 KBytes of non-volatile flash memory and 12K Bytes of embedded SRAM. It contains advance algorithm to implement high quality voice recognition application. The N575C145 also comes equipped with a variety of peripheral devices, such as Timers, Watchdog Timer (WDT), Real-time Clock (RTC), Peripheral Direct Memory Access (PDMA), a variety of serial interfaces (UART, SPI/SSP, I^2C, I^2S), PWM modulators, GPIO, Analog Comparator, Low Voltage Detector and Brown-out detector.

The N575C145 comes equipped with a rich set of power saving modes including a Deep Power Down (DPD) mode drawing less than 1μA. A micro-power 16 KHz oscillator can periodically wake up the device from deep power down to check for other events. A Standby Power Down (SPD) mode can maintain a real time clock function at less than 10 μA.

For audio functionality the N575C145 includes a Sigma-Delta ADC with 92 dB SNR performance coupled with a Programmable Gain Amplifier (PGA) capable of a maximum gain of 61 dB to enable direct connection of a microphone. Audio output is provided by a Differential Class D amplifier (DPWM) that can deliver 1W[1] of power to an 8Ω speaker.

The N575C145 provides eight analog enabled general purpose I/O (GPIO) pads. These pads can be configured to connect to an analog comparator, can be configured as analog current sources or can be routed to the SDADC for analog conversion. They can also be used as a relaxation oscillator to perform capacitive touch sensing.

The N575C145 built-in flagship high-performance embedded voice recognition solution specially optimized for interactive toys. Based on phoneme acoustic models, it enables developers to create applications of speaker-independent (SI) voice recognition capability without requiring costly data collection process for specific commands. Small footprint and compact algorithm design, without compromise in recognition accuracy, allow running on resource-limited platforms

[1] We suggest implementing thermal protection by utilizing the Temperature Alarm; for details please refer to Temperature Alarm in Design Guide or TRM.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz.
  - One 24-bit System tick timer for operating system support.
  - Supports a variety of low power sleep and power down modes.
  - Single-cycle 32-bit hardware multiplier.
  - NVIC (Nested Vector Interrupt Controller) for 32 interrupt inputs, each with 4-levels of priority.
  - Serial Wire Debug (SWD) support with 2 watchpoints/4 breakpoints.
- Power Management
  - Wide operating voltage range from 2.4V to 5.5V.
  - Power management Unit (PMU) providing four levels of power control.
  - Deep Power Down (DPD) mode with sub micro-amp leakage (<1μA).
  - Wakeup from Deep Power Down via dedicated WAKEUP pad or timed operation from internal low power 16 KHz oscillator.
  - Standby mode with limited RAM retention and RTC operation (<10μA).
  - Wakeup from Standby can be from any GPIO interrupt, RTC, WDT or BOD.
  - Sleep mode with minimal dynamic power consumption.
  - 3V LDO for operation of external 3V devices such as serial flash.
- Flash EPROM Memory
  - 145K Bytes Flash EPROM for program code and data storage.
  - 4K Bytes of flash can be configured as boot sector for ISP loader.
  - Support In-system program (ISP) and In-circuit program (ICP) application code update
  - 1K Bytes page erase for flash
  - Configurable boundary to delineate code and data flash.
  - Support 2 wire In-circuit Programming (ICP) update from SWD ICE interface
- SRAM Memory
  - 12K Bytes embedded SRAM.
- Clock Control
  - Built-in high speed and low speed oscillators providing flexible selection for different applications. No external components necessary.
  - Built-in high speed oscillator is trimmable with range of 16 ~ 49 MHz. Factory trimmed within 1% to settings of 49.152 MHz and 32.768 MHz. User trimmable with built-in frequency measurement block (OSCFM) using reference clock of 32 KHz crystal or external reference source.
  - Ultra-low power (<1μA) 16 KHz oscillator for watchdog and wakeup from power-down or sleep operation.
  - External 32 KHz crystal input for RTC function and low power system operation.
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable.
  - I/O pad can be configured as interrupt source with edge/level setting.
- Audio Analog to Digital converter
  - Sigma-Delta ADC with configurable decimation filter and 16-bit output.
  - 92 dB Signal-to-Noise (SNR) performance.

- Programmable gain amplifier with 32 steps from -12 to 35.25 dB in 0.75 dB steps.
- Boost gain stage of 26 dB, giving maximum total gain of 61 dB.
- Input selectable from dedicated MIC inputs or analog enabled GPIO.
- Programmable Bi-quad filter to support multiple sample rates from 8 ~ 32 KHz.
- DMA support for minimal CPU intervention.

- Differential Audio PWM Output (DPWM)
  - Direct connection of speaker
  - 1W drive capability into 8Ω load
  - Configurable up-sampling to support sample rates from 8 ~ 32 KHz
  - DMA support for minimal CPU intervention.
- Timers
  - Two timers with 8-bit pre-scalar and 24-bit resolution.
  - Counter auto reload.
- Watch Dog Timer
  - Multiple clock sources
  - 8 selectable time out period from micro seconds to seconds (depending on clock source)
  - WDT can wake up power down/sleep.
  - Interrupt or reset selectable on watchdog time-out.
- RTC
  - Real Time Clock counter (second, minute, hour) and calendar counter (day, month, year)
  - Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Time tick and alarm interrupts.
  - Device wake up function.
  - Supports software compensation of crystal frequency by compensation register (FCR)
- PWM/Capture
  - Built-in up to two 16-bit PWM generators provide two PWM outputs or one complementary paired PWM outputs.
  - The PWM generator equipped with a clock source selector, a clock divider, an 8-bit pre-scalar and Dead-Zone generator for complementary paired PWM.
  - PWM interrupt synchronous to PWM period.
  - 16-bit digital Capture timers (shared with PWM timers) provide rising/falling capture inputs.
  - Support Capture interrupt
- UART
  - UART ports with flow control (TX, RX, CTS and RTS)
  - 8-Byte FIFO.
  - Support IrDA (SIR) and LIN function
  - Programmable baud-rate generator up to 1/16 of system clock.
- SPI
  - Master up to 20 Mbps / Slave up to 10 Mbps.
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - 2 slave/device select lines when used in master mode.
  - Hardware CRC calculation module available for CRC calculation of data stream.
  - DMA support for burst transfers.
- I^2C

  - Master/Slave up to 1M bit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
  - Programmable clock allowing versatile rate control.
  - I^2C-bus controller supports multiple address recognition.
- I^2S
  - Interface with external audio CODEC.
  - Operate as either master or slave.
  - Capable of handling 8, 16, 24 and 32-bit word sizes
  - Mono and stereo audio data supported
  - I^2S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports DMA requests, for transmit and receive
- Brown-out detector
  - With 8 levels: 2.1V, 2.2V, 2.4V, 2.5V, 2.625V, 2.8V, 3.0V, and 4.6V
  - Supports time-multiplex operation to minimize power consumption.
  - Supports Brownout Interrupt and Reset option
- Built-in Low Dropout Voltage Regulator (LDO)
  - Capable of delivering 30mA load current.
  - Configurable for output voltage of 1.8V, 2.4V, 3.0V and 3.3V
  - Eight GPIO (GPIOA<7:0>) operate from LDO voltage domain allowing direct interface to, for example, 3V SPI Flash.
  - Can be bypassed and voltage domain supplied directly from system power.
- Additional Features
  - Over temperature alarm. Can generate interrupt if device exceeds safe operating temperature.
  - Temperature proportional voltage source which can be routed to ADC for temperature measurements.
  - Digital Microphone interface.
- Support Voice Recognition algorithm
- Operating Temperature: -20°C ~ 85°C

3 PAD DESCRIPTION

Pad No. Chip	Pad Name	Type	Alt CFG	Description
1	WAKEUP	**I**		Pull low to wake part from deep power down
2	PB.7	**A/I/O**	0	General purpose input/output, analog capable; Port B, bit 7
	I^2S_SDO	**O**	1	Serial Data Output for I^2S interface
	CMP7	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
3	PB.6	**A/I/O**	0	General purpose input/output, analog capable; Port B, bit 6
	I^2S_SDI	**I**	1	Serial Data Input for I^2S interface
	CMP6	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_MOSI1	**O**	3	Master Out, Slave In channel 1 for SPI interface
4	PB.5	**A/I/O**	0	General purpose input/output, analog capable; Port B, bit 5
	PWM1B	**O**	1	PWM channel 1 complementary output
	CMP5	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_MISO1	**I**	3	Master In, Slave Out channel 1 for SPI interface
5	PB.4	**A/I/O**	0	General purpose input/output, analog capable; Port B, bit 4
	PWM0B	**O**	1	PWM channel 0 complementary output
	CMP4	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_MOSI0	**O**	3	Master Out, Slave In channel 0 for SPI interface
6	PB.3	**A/I/O**	0	General purpose input/output, analog capable; Port B, bit 3
	I^2C_SDA	**I/O**	1	Serial Data, I^2C interface
	CMP3	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_MISO0	**I**	3	Master In, Slave Out channel 0 for SPI interface

Pad No. Chip	Pad Name	Type	Alt CFG	Description
7	PB.2	**A/I/O**	0	General purpose input/output, analog capable; Port B, bit 2
	I^2C_SCL	**I/O**	1	Serial Clock, I^2C interface
	CMP2	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_SCLK	**I/O**	3	Serial Clock for SPI interface
8	PB.1	**A/I/O**	0	General purpose input/output, analog capable; Port B, bit 1. Triggers external interrupt 1 (EINT1/IRQ3)
	MCLK	**O**	1	Master clock output for synchronizing external device
	CMP1	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_SSB1	**O**	3	Slave Select Bar 1 for SPI interface
9	PB.0	**A/I/O**	0	General purpose input/output, analog capable; Port B, bit 0. Triggers external interrupt 0 (EINT0/IRQ2)
	SPI_SSB1	**O**	3	Slave Select Bar 1 for SPI interface
	CMP0	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_SSB0	**I/O**	3	Slave Select Bar 0 for SPI interface
10 11	Reserved			Remain unconnected
12	VCCDPST	**P**		Digital Supply for Chip, Connect to VCCD
13	VCCD	**P**		Main Digital Supply for Chip. Supplies all IO except analog, Speaker Driver and PA<7:0>
14	VREG	**P**		Logic regulator output for decoupling. A 1µF capacitor returning to VSSD must be placed on it..
15	PA.15	**I/O**	0	General purpose input/output; Port A, bit 15
	TM1	**I**	1	External input to Timer 1
	SDIN	**I**	2	Sigma-Delta bit stream input for digital MIC mode
16	PA.9	**I/O**	0	General purpose input/output; Port A, bit 9
	UART_RX	**I**	1	Receive channel of UART
	I^2S_BCLK	**I/O**	2	Bit Clock for I^2S interface
17	PA.8	**I/O**	0	General purpose input/output; Port A, bit 8

Pad No. Chip	Pad Name	Type	Alt CFG	Description
	UART_TX	**O**	1	Transmit channel of UART
	I^2S_FS	**I/O**	2	Frame Sync Clock for I^2S interface
18	VCCSPK	**P**		Power Supply for PWM Speaker Driver, Connect with pad 25 (VCCSPK) externally.
19 20	SPK+ SPK+	**O**		Positive Speaker Driver Output, double-bond.
21 22	VSSSPK VSSSPK	**P**		Ground for PWM Speaker Driver, double-bond.
23 24	SPK- SPK-	**O**		Negative Speaker Driver Output, double-bond
25	VCCSPK	**P**		Power Supply for PWM Speaker Driver, Connect with pad 18 (VCCSPK) externally.
26	RESETN	**I**		External reset input. Pull low to reset device to initial state. Has internal weak pull-up.
27	ICE_DAT	**I/O**		Serial Wire Debug port data. Has internal weak pull-up.
28	ICE_CLK	**I**		Serial Wire Debug port clock. Has internal weak pull-up.
29	VSSD			Digital Ground.
30	VSSDPST	**P**		Digital Ground, Connect to VSSD.
31	PA.7	**I/O**	0	General purpose input/output; Port A, bit 7
	I^2S_SDO	**O**	1	Serial Data Out for I^2S interface
32	PA.6	**I/O**	0	General purpose input/output; Port A, bit 6
	I^2S_SDI	**I**	1	Serial Data In for I^2S interface
33	PA.5	**I/O**	0	General purpose input/output; Port A, bit 5
	I^2S_BCLK	**I/O**	1	Bit Clock for I^2S interface
34 35	Reserved			Remain unconnected
36	PA.4	**I/O**	0	General purpose input/output; Port A, bit 4
	I^2S_FS	**I/O**	1	Frame Sync Clock for I^2S interface
37	PA.3	**I/O**	0	General purpose input/output; Port A, bit 3
	SPI_MISO0	**I**	1	Master In, Slave Out channel 0 for SPI interface

Pad No. Chip	Pad Name	Type	Alt CFG	Description
	I^2C_SDA	**I/O**	2	Serial Data, I^2C interface
38	PA.2	**I/O**	0	General purpose input/output; Port A, bit 2
	SPI_SSB0	**I/O**	1	Slave Select Bar 0 for SPI interface
39	VDLDO	**P**		LDO Regulator Output. If used, a 1µF capacitor must be placed to ground. If not used then tie to VCCD.
40	PA.1	**I/O**	0	General purpose input/output; Port A, bit 1
	SPI_SCLK	**I/O**	1	Serial Clock for SPI interface
	I^2C_SCL	**I/O**	2	Serial Clock, I^2C interface
41	PA.0	**I/O**	0	General purpose input/output; Port A, bit 0
	SPI_MOSI0	**O**	1	Master Out, Slave In channel 0 for SPI interface
	MCLK	**O**	2	Master clock output.
42	VCCLDO	**P**		Power Supply for LDO, should be connected to VCCD
43	PA.14	**I/O**	0	General purpose input/output; Port A, bit 14
	SDCLK	**O**	1	Clock output for digital microphone mode.
	SDCLKN	**O**	2	Inverse Clock output for digital microphone mode.
44	PA.13	**I/O**	0	General purpose input/output; Port A, bit 13
	PWM1	**O**	1	PWM1 Output.
	SPKM	**O**	2	Equivalent to SPK-.
	I^2S_BCLK	**I/O**	3	Bit Clock for I^2S interface
45	PA.12	**I/O**	0	General purpose input/output; Port A, bit 12
	PWM0	**O**	1	PWM0 Output.
	SPKP	**O**	2	Equivalent to SPK+
	I^2S_FS	**I/O**	3	Frame Sync Clock for I^2S interface
46	XO32K	**O**		32.768 KHz Crystal Oscillator Output
47	XI32K	**I**		32.768 KHz Crystal Oscillator Input. Max Voltage 1.8V
48	VSSA	**AP**		Ground for analog circuitry.
49	VMID	**O**		Mid rail reference. Connect 4.7µF to VSSA.
50	MIC+	**AI**		Positive microphone input.

Pad No. Chip	Pad Name	Type	Alt CFG	Description
51	MIC-	**AI**		Negative microphone input.
52	MICBIAS	**AO**		Microphone bias output.
53	VCCA	**AP**		Analog power supply.
54	PA.11	**I/O**	0	General purpose input/output; Port A, bit 11
	I^2C_SCL	**I/O**	1	Serial Clock, I^2C interface
	I^2S_SDO	**O**	2	Serial Data Out I^2S interface
	UART_CTSN	**I**	3	UART Clear to Send Input.
55	PA.10	**I/O**	0	General purpose input/output; Port A, bit 10
	I^2C_SDA	**I/O**	1	Serial Data, I^2C interface
	I^2S_SDI	**I**	2	Serial Data In I^2S interface
	UART_RTSN	**O**	3	UART Request to Send Output.

Note:

- Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power; AP=Analog Power
- There are some aliases of GPIO, for example, PA.5 could be PA5, GPA5 or GPIOA5.

4 BLOCK DIAGRAM

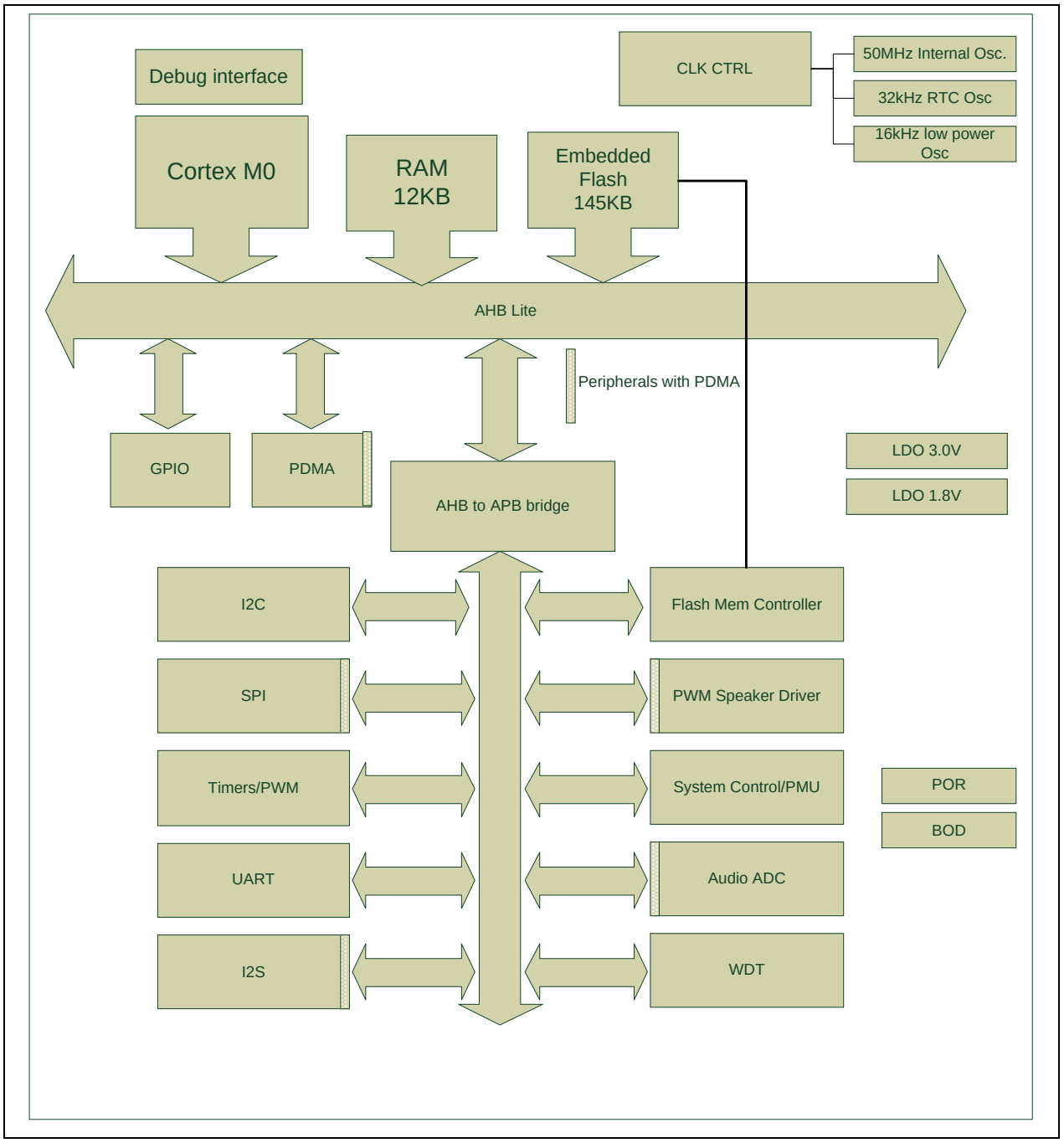
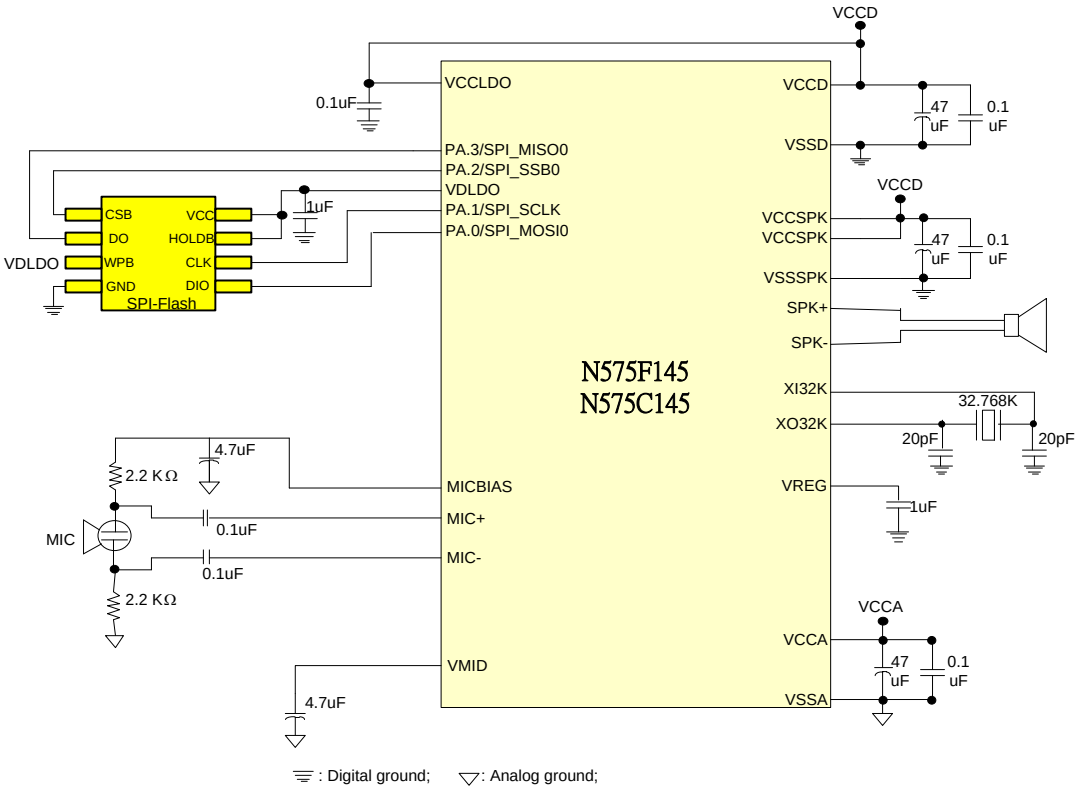


Figure 4-1 N575C145 Block Diagram

5 APPLICATION DIAGRAM



6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
DC Power Supply	VDD–VSS	-0.3	+6.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency			50	MHz
Operating Temperature	TA	-20	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}			120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O			35	mA
Maximum Current sourced by a I/O			35	mA
Maximum Current sunk by total I/O			100	mA
Maximum Current sourced by total I/O			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

6.2 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, F_{OSC} = 49.152 MHz unless otherwise specified.)

Parameter	Sym.	Specification				Test Conditions
		Min	Typ.	Max	Unit	
Operation voltage	V_{DD}	2.4		5.5	V	V_{DD} =2.4V ~ 5.5V
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 49.152 MHz	I_{DD1}		24.8		mA	V_{DD}= 5.5V, Enable all IP.
	I_{DD2}		19.7		mA	V_{DD}=5.5V, disable all IP
	I_{DD3}		23.6		mA	V_{DD} = 3V, enable all IP
	I_{DD4}		18.3		mA	V_{DD} = 3V, disable all IP
Operating Current Normal Run Mode @ 32.768 MHz	I_{DD5}		18.8		mA	V_{DD} = 5.5V, Enable all IP.
	I_{DD6}		15.0		mA	V_{DD} = 5.5V, Disable all IP.
	I_{DD7}		17.6		mA	V_{DD} = 3V, Enable all IP.
	I_{DD8}		13.8		mA	V_{DD} = 3V, Disable all IP.

Operating Current Normal Run Mode @ 12.288 MHz	I_{DD9}		12.5		mA	V_{DD} = 5.5V enable all IP
	I_{DD10}		10.3		mA	V_{DD} = 5.5V, disable all IP
	I_{DD11}		11.4		mA	V_{DD} = 3V enable all IP
	I_{DD12}		9		mA	V_{DD} = 3V, disable all IP
Operating Current Normal Run Mode @ 4.9152 MHz	I_{DD13}		9.7		mA	V_{DD} = 5.5V, Enable all IP.
	I_{DD14}		8.1		mA	V_{DD} = 5.5V, Disable all IP.
	I_{DD15}		8.7		mA	V_{DD} = 3V, Enable all IP.
	I_{DD16}		7.0		mA	V_{DD} = 3V, Disable all IP.
Operating Current Sleep Mode	I_{IDLE1}		10		mA	V_{DD}= 5.5V
	I_{IDLE1}		9		mA	V_{DD}= 3.3V
Operating Current Deep Sleep Mode	I_{IDLE1}		10		mA	V_{DD}=5.5V
	I_{IDLE1}		8		mA	V_{DD}= 3.3V
Standby Power down mode(SPD)	I_{IDLE1}		3		µA	V_{DD}=3.3V 32K running with RTC
	I_{IDLE1}		1		µA	V_{DD}= 3.3V 16K running
Operating Current Deep Power down mode(DPD)	I_{IDLE1}		500		nA	V_{DD}=3.3V Wakeup with16K
	I_{IDLE1}				nA	V_{DD}= 3.3V wakeup with WAKEUP pad

Input Current PA, PB (Quasi-bidirectional mode)	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at RESETN [1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PB (Quasi-bidirectional mode)	I_{TL}	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage PA, PB (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	V	
Input High Voltage X32I[*2]	V_{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), RESETN	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input), RESETN	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage of PA~PB(Schmitt input)	V_{HY}		0.2V_{DD}		V	

Source Current PA, PB (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brownout voltage with BOV_VL [2:0] =000b	$V_{BO2.1}$		2.15		V	
Brownout voltage with BOV_VL [2:0] =001b	$V_{BO2.2}$		2.25		V	
Brownout voltage with BOV_VL [2:0] =010b	$V_{BO2.4}$		2.45		V	
Brownout voltage with BOV_VL [2:0] =011b	$V_{BO2.5}$		2.55		V	
Brownout voltage with BOV_VL [2:0] =100b	$V_{BO2.7}$		2.7		V	
Brownout voltage with BOV_VL [2:0] =101b	$V_{BO2.8}$		2.8		V	
Brownout voltage with BOV_VL [2:0] =110b	$V_{BO3.0}$		3.0		V	
Brownout voltage with BOV_VL [2:0] =111b	$V_{BO4.5}$		4.55		V	

Notes:

1. RESETN is a Schmitt trigger input.
2. Crystal Input is a CMOS input.

6.3 AC Electrical Characteristics

6.3.1 External 32 KHz XTAL Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Input clock frequency	External crystal	-	32.768	-	KHz
Temperature	-	-20	-	85	℃
V_{DD}	-	2.4	-	5.5	V

6.3.2 Internal 49.152 MHz Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage[1]	-	2.4	-	5.5	V
Center Frequency	-	-	49.152		MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-1	-	1	%
	-20°C~+85°C; V_{DD}=2.5V~5.5V	-4	-	4	%

6.3.3 Internal 16 KHz Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage[1]	-	2.4	-	5.5	V
Center Frequency	-	-	16	-	KHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-10	-	10	%
	-20°C~+85°C; V_{DD}=2.5V~5.5V	-20	-	20	%

Notes:

1. Internal operation voltage comes from LDO.

6.3.4 Reset Characteristics

(VDD-VSS=5V, TA = 25°C, F_{OSC} = 49.152 MHz unless otherwise specified.)

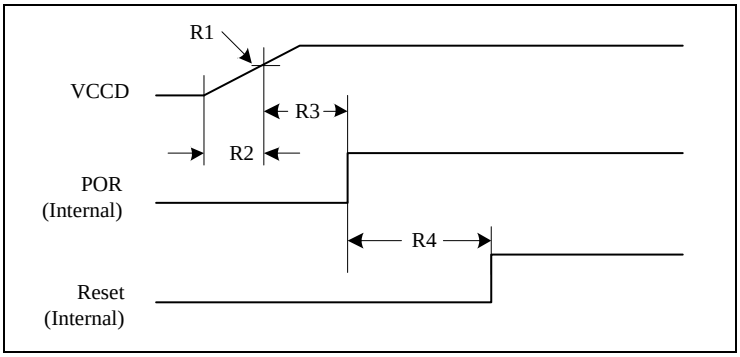
Parameter No.	Parameter	Parameter Name	Min	Typ	Max	Unit
R1	V_{TH}	Reset threshold	1	1.7	2	V
R2	$T_{VDDRISE}$	Supply voltage (VDD) rise time (0V-V_{TH}), power on reset	-	-	100	ms
R3	T_{POR}	Power-On Reset timeout	-	-	12	µs
R4	T_{IRPOR}	Internal reset timeout after POR	-	-	45	µs

R5	T_{MIN}	Minimum RESETN pulse width	100	-	-	ns
R6	T_{IRHWR}	Internal reset timeout after hardware reset (RESETN)	-	-	20	µs
R7	T_{IRSWR}	Internal reset timeout after software-initiated system reset	-	-	2	µs
R8	T_{IRWDR}	Internal reset timeout after watchdog reset	-	-	3 *[2]	µs

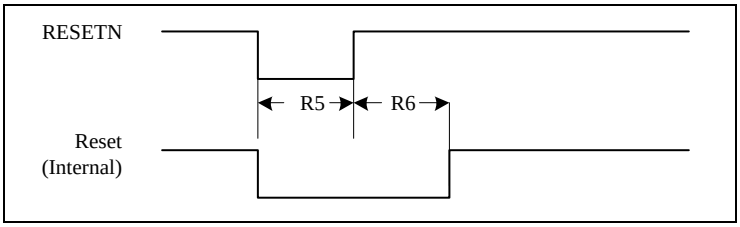
Notes:

2. It will be 6500us when use OSC_16K as the WDT clock.

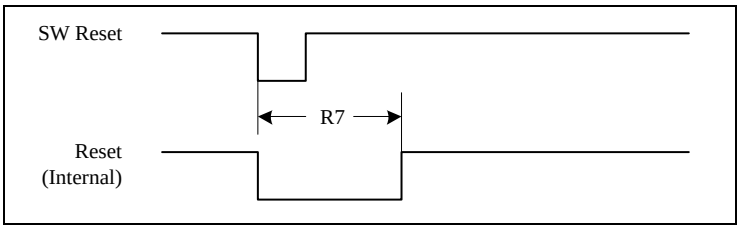
6.3.4.1 Power-On Reset Timing



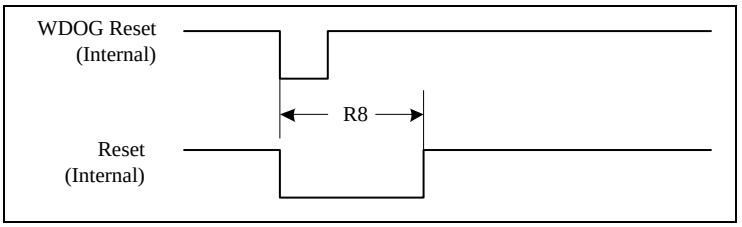
6.3.4.2 External Reset Timing (RESETN)



6.3.4.3 Software Reset Timing



6.3.4.4 Watchdog Reset Timing



7 ORDERING INFORMATION

Die form: N575C145 (Blank)

Die form: N575C145xxxx (Pre-code)

8 REVISION HISTORY

Version	Date	Substantial Changes	Page
A1	Sep. 2015	Initial Release	All

Important Notice

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.