N584HP300

Data Sheet

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1. General Description

N584HP300 (OTP) is a 4-bit microcontroller-based speech synthesizer with PWM mode output to drive the speaker directly. The synthesizer contains one voice-channel and/or dual tone melody. It has ***Ultra I/O***^{TM} to simplify the procedure of defining the output pattern, besides, it also includes 4-level Low Voltage Detection function. The N584HP300 built-in OTP to cover following ROM version bodies:

N584H	H009	H010	H019	H020	H029	H030	H039	H040
ROM (Kbit)	300	300	620	620	940	940	1260	1260
*Duration	12”	12”	24”	24”	37”	37”	49”	49”
I/O pins	4	8	4	8	4	8	4	8

N584H	H060	H070	H120	H170	H210	H260	H300
ROM (Kbit)	1740	1900	3340	4460	5740	7020	7980
*Duration	68”	73”	131”	175”	225”	275”	312
I/O pins	8	8	16	16	16	16	16

Note1: The duration time is based on 4-bit NM4 at 6 KHz sampling rate

2. Features

- Operating Voltage and CPU Frequency:
  - 1.8 ~ 5.5V (Fcpu = 4 MHz)
  - 2.0 ~ 5.5V (Fcpu = 8 MHz)
- Speech synthesis
  - 1-channel voice
  - Dual Tone Melody w/ 8 octaves
  - 4-bit NM4
- Build in internal oscillator (TRIM)
- Build in PWM Direct Drive circuit
- Programmable sample rate
- Provides power management to save current consumption
  - 4 / 8 MHz system clock, with Ring type oscillator
  - STOP mode for stopping entire device’s operation
- Provides 16 I/O
- High sink current capability

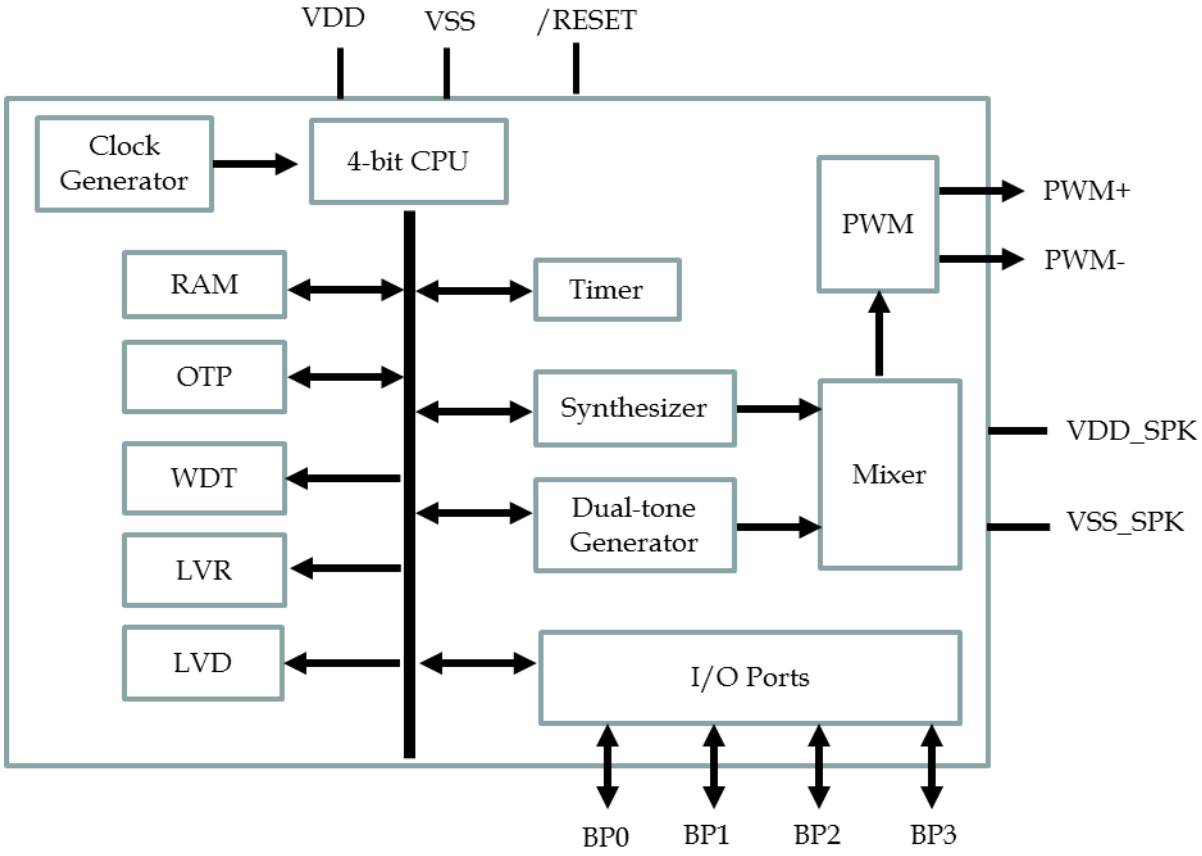
- Support capture timer to implement up to 8 capture sensor key
- Provides 224*4 bits RAM
- Provides 64K*10 of program data
- Provides IR carrier generator (38 KHz or 56 KHz)
- Provides Watch Dog Timer (WDT)
- Provides Low Voltage Reset (LVR: 1.7V, 1.9V)
- Provides Low Voltage Detection (LVD: 2.2V, 2.4V, 3.0V, 3.3V)
- Shared ROM for voice and program storage
- Supports ***PowerScript***^{TM} for developing codes easily
- Full-fledged development system
  - Source-level ICE debugger (***PowerScript***^{TM} format)
  - Event synchronization mechanism
  - User-friendly GUI environment
  - It has ***Ultra I/O***^{TM} to simplify the defined output pattern

3. Pad Description

Pad Name	I/O	Function
BP00 ~ BP03	I/O	Bi-directional I/O port0, defined as input or output. As input, it can be set as pull-high, pull-low or floating. As output, it is defined as CMOS. BP03 can also be defined as IR carrier output.
BP10 ~ BP13	I/O	Bi-directional I/O port1, defined as input or output. As input, it can be set as pull-high, pull-low or floating. As output, it is defined as CMOS.
BP20 ~ BP23	I/O	Bi-directional I/O port2, defined as input or output. As input, it can be set as pull-high, pull-low or floating. As output, it is defined as CMOS.
BP30 ~ BP33	I/O	Bi-directional I/O port3, defined as input or output. As input, it can be set as pull-high, pull-low or floating. As output, it is defined as CMOS.
VDD, VDD_IO	-	Power supply
VSS, VSS_IO	-	Ground
V33O	-	3.3V regulator output
VPP	-	Positive high voltage 7.5V input during OTP memory writer mode. NC for normal operation mode
PWM+	O	PWM drive positive output
PWM-	O	PWM drive negative output
VDD_SPK	-	Power supply for PWM drive
VSS_SPK	-	Ground for PWM drive
TEST	-	Test pin
/RESET	I	Chip reset input with Schmitt trigger, internal pull-high

Note: As program OTP, the BP01 ~ BP03, VDD, VSS, V33O, /RESET and VPP pin will be used.

4. Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Item	Symbol	Conditions	Rated Value	Unit
Power Supply	VDD – VSS	-	-0.3 ~ +7.0	V
Input Voltage	VIN	All Inputs	VSS-0.3 ~ VDD+0.3	V
Storage Temp.	TSTG	-	-55 ~ +150	°C
Operating Temp.	TOPR	-	0 ~ +70	°C

NOTE:
Operating the device under conditions beyond those indicated above may cause permanent damage or affect device reliability.

5.2 DC Parameters

(VDD−VSS = 4.5V, VDD_SPK-VSS_SPK=4.5V, TA = 25°C; no load, unless otherwise specified)

Parameter	Sym	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}	Fcpu = 4 MHz Fcpu = 8 MHz	1.8 2.0		5.5 5.5	V
Operating current	I_{OP}	Fcpu=8 MHz, VDD=4.5V		5.0		mA
		Fcpu=8 MHz, VDD=3.0V		3.0		
Standby current	I_{SB}	VDD=4.5V		3	10	μA
		VDD=3.0V		3	10	
Output high current (BP0, BP1,BP2,BP3)	I_{OH}	VDD=3.0V,Vout=2.6V	-5	-6		mA
		VDD=4.5V,Vout=2.6V		-30		
Output low current (BP0, BP1,BP2,BP3)	I_{OL}	VDD=3.0V,Vout=0.4V	8	12		mA
		VDD=4.5V,Vout=1.0V		34		
PWM driver current	Ipw	Rl=8Ω, connect to PWM+ and PWM-	200			mA
Pull-high resistor (BP0, BP1,BP2,BP3)	R_{PL}	VDD=4.5V		150K 1M		Ω
LVD Voltage	V_{LVD}	LVD_SEL[1:0] = 11	3.14	3.3	3.47	V
		LVD_SEL[1:0] = 10	2.85	3.0	3.15	V
		LVD_SEL[1:0] = 01	2.28	2.4	2.52	V
		LVD_SEL[1:0] = 00	2.09	2.2	2.31	V

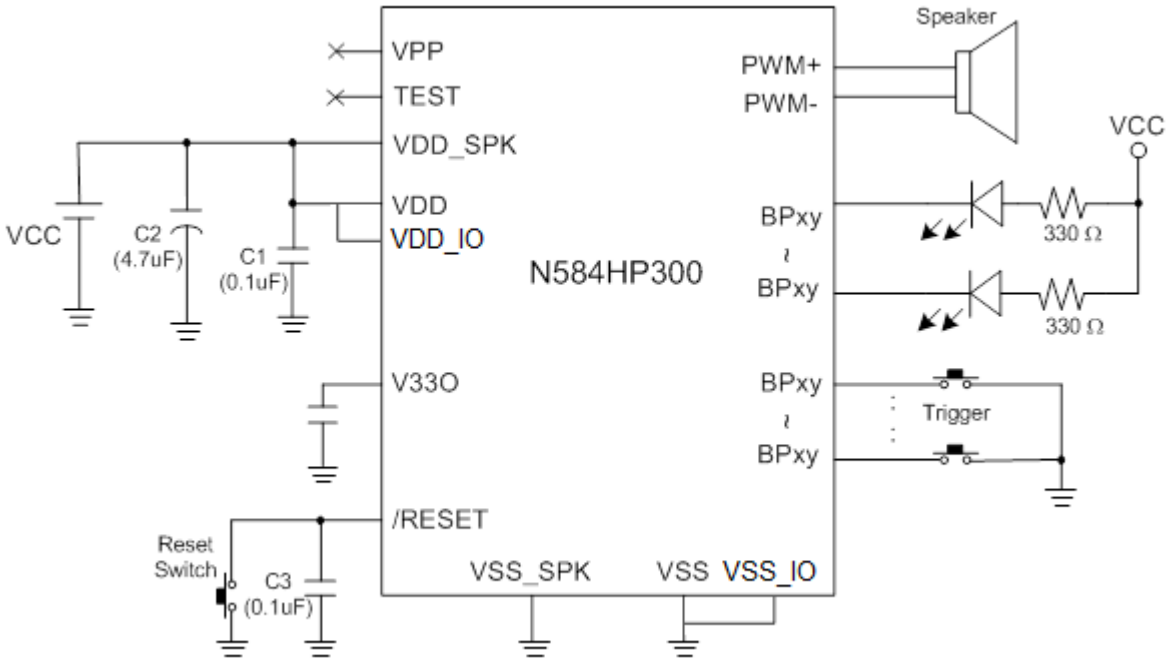
5.3 AC Parameters

(VDD−VSS = 4.5V, TA = 25° C; unless otherwise specified)

Parameter	Sym	Conditions	Min	Typ	Max	Unit
Main-clock Frequency	Fosc	8 MHz	7.95	8.19	8.44	MHz
Frequency Deviation	$\frac{\Delta F}{F}$	Fosc=8MHz, VDD=2.2 ~ 5.5V $\frac{Fosc(\max) - Fosc(\min)}{Fosc(\min)}$		3	5	%

6. Typical Application Circuit

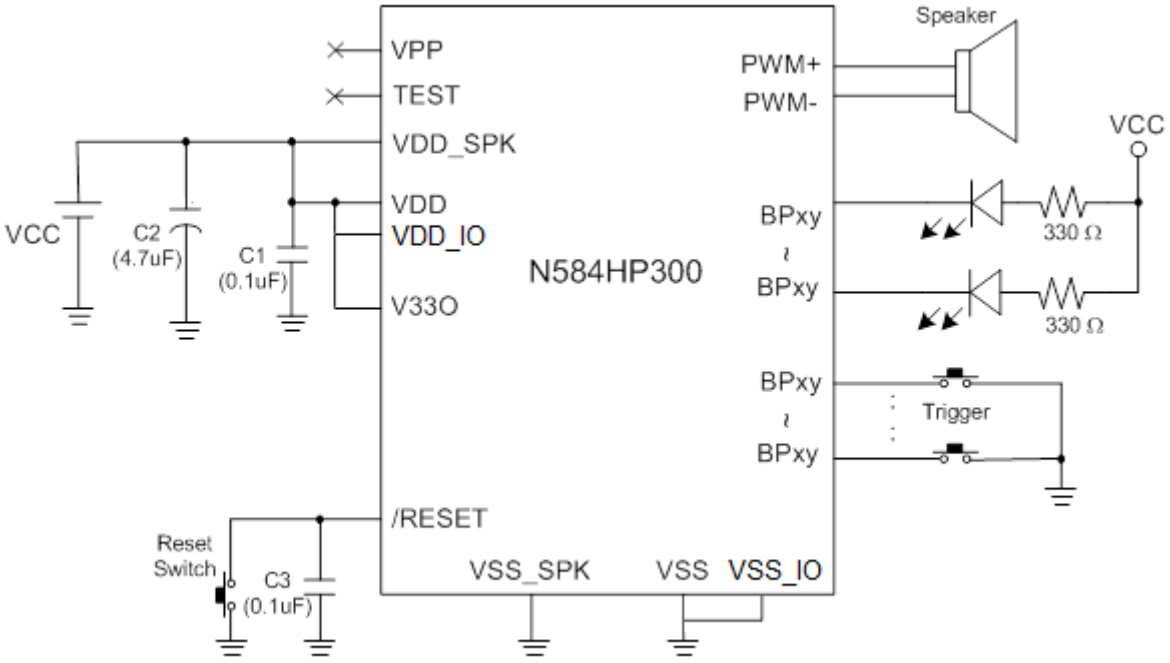
3-battery Application



Notes:

1. In PCB layout, VSS_SPK should be connected to VSS; and VDD_SPK should be connected to VDD
2. The C1 capacitor 0.1uF is recommended to prevent the IC from hang-up as battery power bouncing. For power line layout in extended length, suggest C1 to be 1uF
3. The C2 capacitor 4.7uF shunts between VDD and GND is to stabilize power noise
4. The C3 capacitor 0.1uF shunts between /Reset and GND is for power reset stability
5. The V33O capacitor value is 0.1uF. It is for regulator power stability on 3-battery applications
6. BPxy means I/O pins. X: 0 ~ 3; Y: 0 ~ 3

2-battery Application



Notes:

1. In PCB layout, VSS_SPK should be connected to VSS; and VDD_SPK should be connected to VDD
2. The C1 capacitor 0.1uF is recommended to prevent the IC from hang-up as battery power bouncing. As power line is long, suggest C1 to be 1uF
3. The C2 capacitor 4.7uF shunts between VDD and GND is to stabilize power noise
4. The C3 capacitor 0.1uF shunts between /Reset and GND is for power reset stability
5. BPxy means I/O pins. X: 0 ~ 3; Y: 0 ~ 3

7. Revision History

Version	Date	Substantial Changes	Page
A1.0	Sep. 2015	Initial Release	
A2.0	Jul. 2016	Revise application circuits	8, 9