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64Kb Low Power Serial SRAMs

8K × 8 bit Organization

Overview

The AMI Semiconductor serial SRAM family includes several integrated memory devices including this 64K serially accessed Static Random Access Memory, internally organized as 8K words by 8 bits. The devices are designed and fabricated using AMI's advanced CMOS technology to provide both high-speed performance and low power. The devices operate with a single chip select ($\overline{CS}$) input and use a simple Serial Peripheral Interface (SPI) serial bus. A single data in and data out line is used along with a clock to access data within the devices. The N64S08xxHDA devices include a $\overline{HOLD}$ pin that allows communication to the device to be paused. While paused, input transitions will be ignored. The devices can operate over a wide temperature range of -40°C to +85°C and can be available in several standard package offerings.

Features

- **Power Supply Options**
  1.8V to 3.6V
- **Very low standby current**
  As low as 200nA
- **Very low operating current**
  As low as 500uA
- **Simple memory control**
  Single chip select ($\overline{CS}$)
  Serial input (SI) and serial output (SO)
- **Flexible operating modes**
  Word read and write
  Page mode (32 word page)
  Burst mode (full array)
- **Organization**
  8K x 8 bit
- **Self timed write cycles**
- **Built-in write protection ($\overline{CS}$ high)**
- **$\overline{HOLD}$ pin for pausing communication**
- **High reliability**
  Unlimited write cycles
- **RoHS Compliant Packages**
  Green SOIC and TSSOP

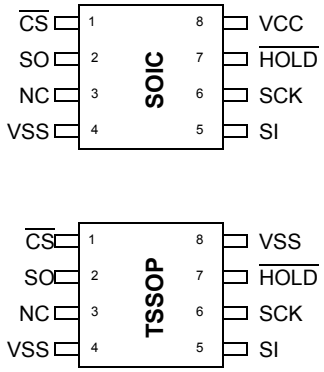
Device Options

Part Number	Density	Power Supply (V)	Speed (MHz)	Feature	Typical Standby Current	Read/Write Operating Current
N64S0818HDA	64Kb	1.8	20	$\overline{HOLD}$	200nA	500 uA @ 1Mhz
N64S0830HDA		3.0	25		1uA	

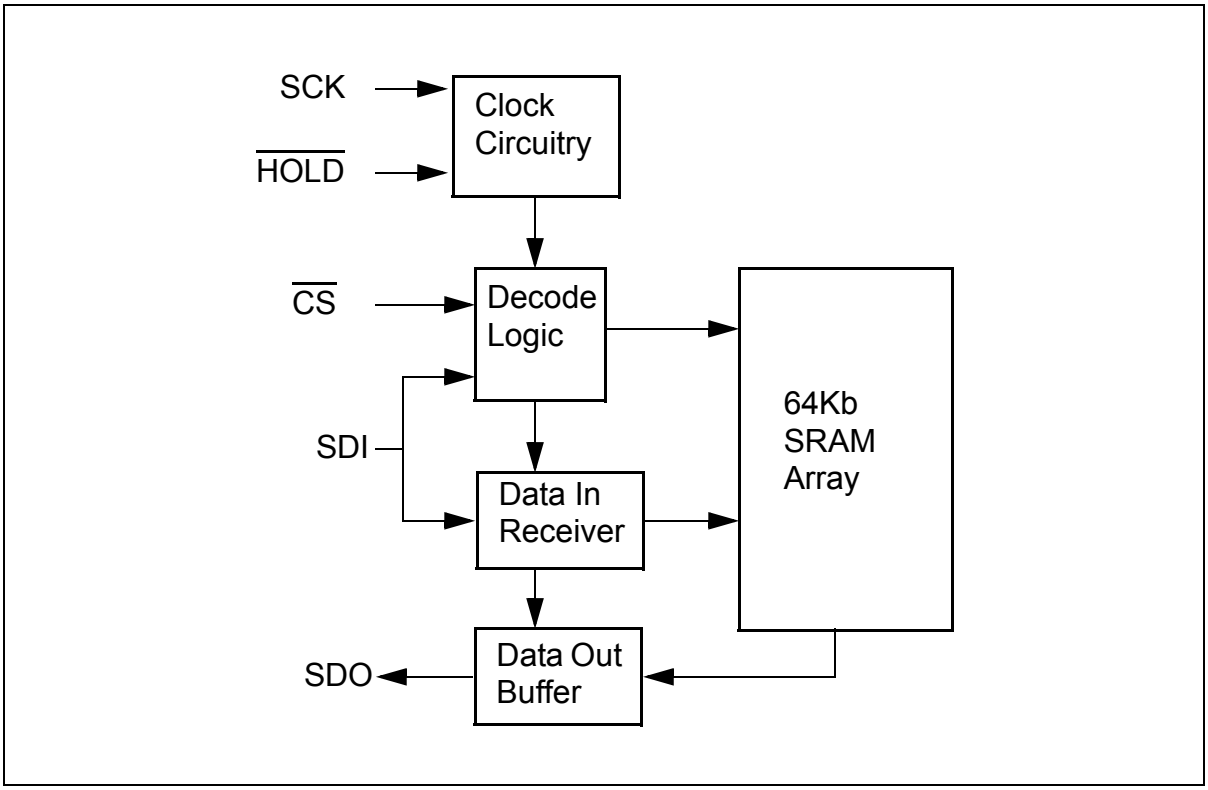
Pin Names

Pin Name	Pin Function
$\overline{CS}$	Chip Select Input
SCK	Serial Clock Input
SI	Serial Data Input
SO	Serial Data Output
$\overline{HOLD}$	Hold Input
NC	No Connect
V_{CC}	Power
V_{SS}	Ground

Package Configurations



Functional Block Diagram



Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min.	Typ[1]	Max	Unit
Supply Voltage	V_{CC}	1.8V Device	1.7		1.95	V
Supply Voltage	V_{CC}	3V Device	2.3		3.6	V
Input High Voltage	V_{IH}		0.7 x V_{CC}		V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3		0.3 x V_{CC}	V
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	V_{CC}–0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.2	V
Input Leakage Current	I_{LI}	$\overline{CS}$ = V_{CC}, V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{CC}, V_{OUT} = 0 to V_{CC}			0.5	µA
Read/Write Operating Current	I_{CC1}	F = 1MHz, I_{OUT} = 0			500	µA
	I_{CC2}	F = 10MHz, I_{OUT} = 0			4	mA
	I_{CC3}	F = 20/25MHz, I_{OUT} = 0			8/10	mA
Standby Current	I_{SB}	1.8V Device $\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		200	500	nA
		3V Device $\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	3	µA

1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and are not 100% tested.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		7	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		7	pF

1. These parameters are verified in device characterization and are not 100% tested

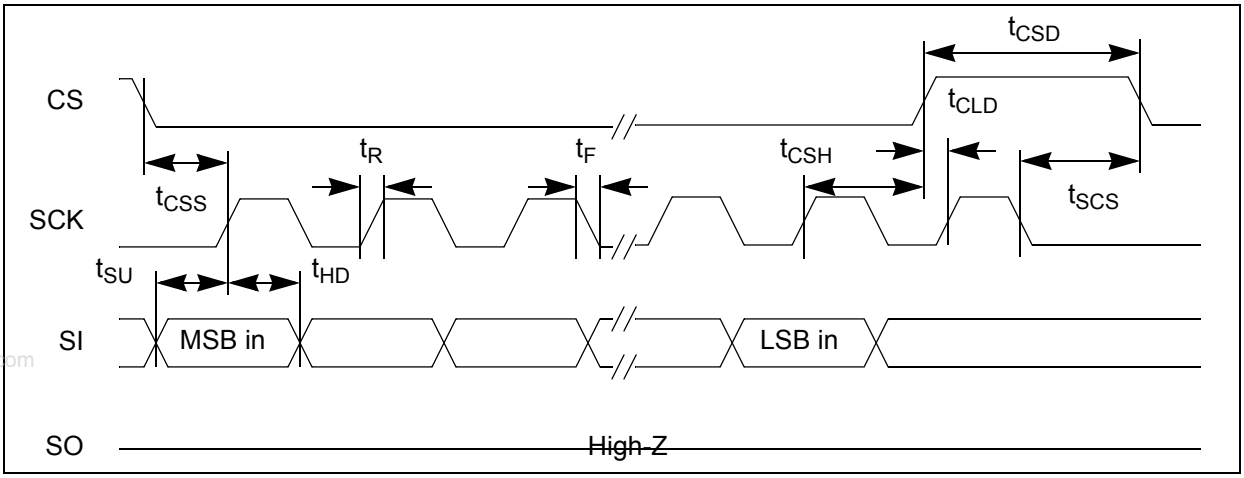
Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 100pF
Operating Temperature	-40 to +85 ^{o}C

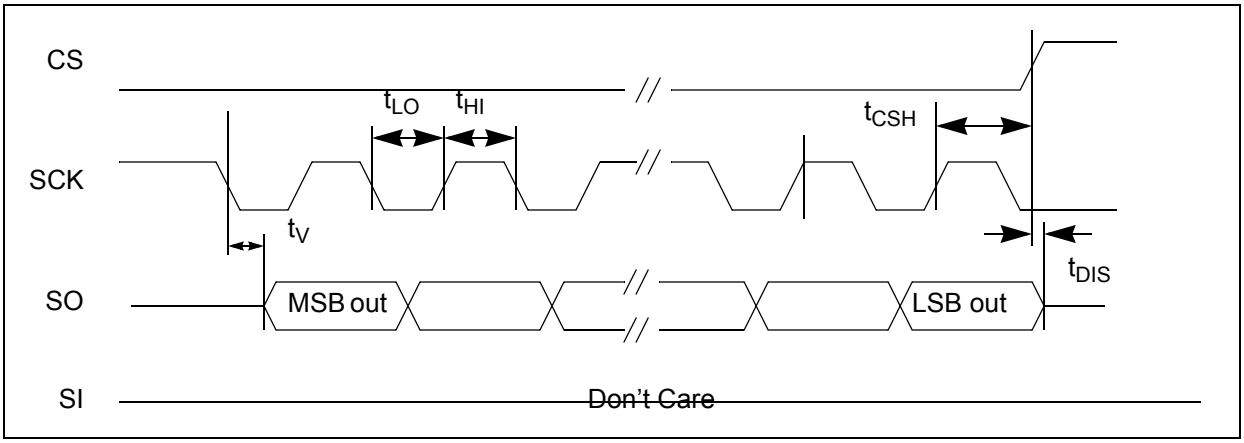
Timing

Item	Symbol	1.8V Device		3V Device		Units
		Min.	Max.	Min.	Max.	
Clock Frequency	f_{CLK}		20		25	MHz
Clock Rise Time	t_R		2		2	us
Clock Fall Time	t_F		2		2	us
Clock High Time	t_{HI}	25		20		ns
Clock Low Time	t_{LO}	25		20		ns
Clock Delay Time	t_{CLD}	25		20		ns
$\overline{CS}$ Setup Time	t_{CSS}	25		20		ns
$\overline{CS}$ Hold Time	t_{CSH}	50		40		ns
$\overline{CS}$ Disable Time	t_{CSD}	25		20		ns
SCK to $\overline{CS}$	t_{SCS}	5		5		ns
Data Setup Time	t_{SU}	10		10		ns
Data Hold Time	t_{HD}	10		10		ns
Output Valid From Clock Low	t_V		25		20	ns
Output Hold Time	t_{HO}	0		0		ns
Output Disable Time	t_{DIS}		20		15	ns
$\overline{HOLD}$ Setup Time	t_{HS}	10		10		ns
$\overline{HOLD}$ Hold Time	t_{HH}	10		10		ns
$\overline{HOLD}$ Low to Output High-Z	t_{HZ}	10		10		ns
$\overline{HOLD}$ High to Output Valid	t_{HV}		50		40	ns

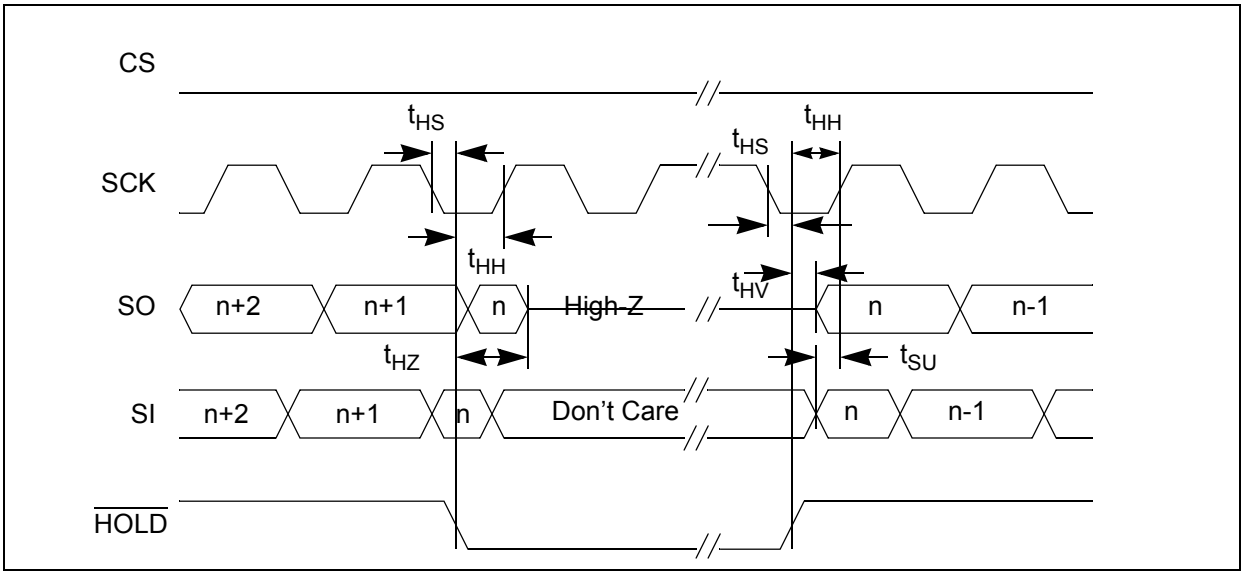
Serial Input Timing



Serial Output Timing



Hold Timing



Control Signal Descriptions

Signal	Name	I/O	Description
$\overline{CS}$	Chip Select	I	A low level selects the device and a high level puts the device in standby mode. If $\overline{CS}$ is brought high during a program cycle, the cycle will complete and then the device will enter standby mode. When $\overline{CS}$ is high, SO is in high-Z. $\overline{CS}$ must be driven low after power-up prior to any sequence being started.
SCK	Serial Clock	I	Synchronizes all activities between the memory and controller. All incoming addresses, data and instructions are latched on the rising edge of SCK. Data out is updated on SO after the falling edge of SCK.
SI	Serial Data In	I	Receives instructions, addresses and data on the rising edge of SCK.
SO	Serial Data Out	O	Data is transferred out after the falling edge of SCK.
$\overline{HOLD}$	Hold	I	A high level is required for normal operation. Once the device is selected and a serial sequence is started, this input may be taken low to pause serial communication without resetting the serial sequence. The pin must be brought low while SCK is low for immediate use. If SCK is not low, the Hold function will not be invoked until the next SCK high to low transition. The device must remain selected during this sequence. SO is high-Z during the Hold time and SI and SCK are inputs are ignored. To resume operations, $\overline{HOLD}$ must be pulled high while the SCK pin is low. Lowering the $\overline{HOLD}$ input at any time will take to SO output to High-Z.

Functional Operation

Basic Operation

The 64Kb serial SRAM is designed to interface directly with a standard Serial Peripheral Interface (SPI) common on many standard micro-controllers. It may also interface with other non-SPI ports by programming discrete I/O lines to operate the device.

The serial SRAM contains an 8-bit instruction register and is accessed via the SI pin. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation. Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared, the user can assert the $\overline{HOLD}$ input and place the device into a Hold mode. After releasing the $\overline{HOLD}$ pin, the operation will resume from the point where it was held.

The following table contains the possible instructions and formats. All instructions, addresses and data are transferred MSB first and LSB last.

Instruction Set

Instruction	Instruction Format	Description
READ	0000 0011	Read data from memory starting at selected address
WRITE	0000 0010	Write data to memory starting at selected address
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register

READ Operations

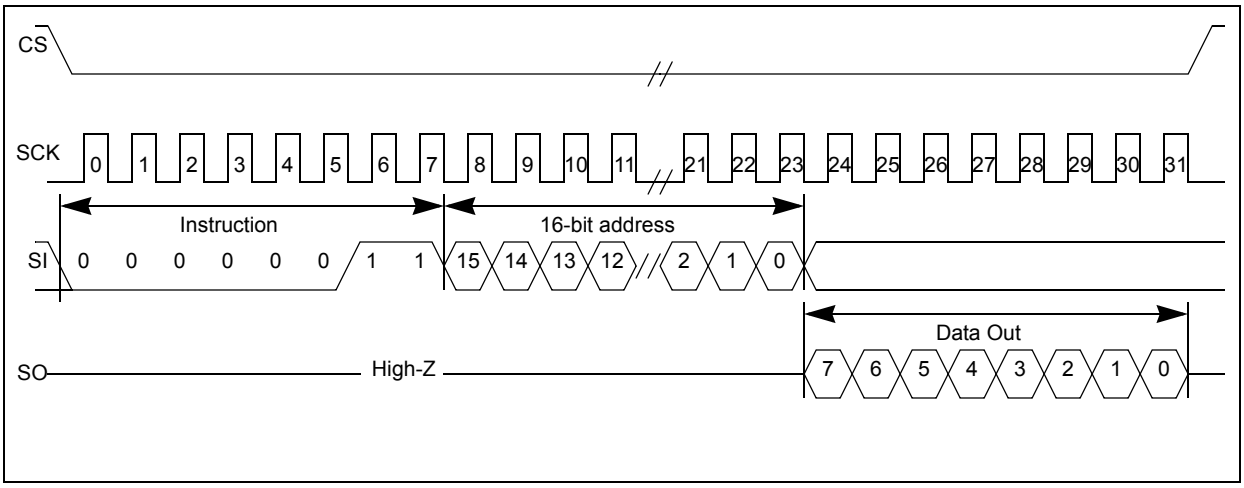
The serial SRAM READ is selected by enabling $\overline{CS}$ low. First, the 8-bit READ instruction is transmitted to the device followed by the 16-bit address with the 3 MSBs being don't care. After the READ instruction and addresses are sent, the data stored at that address in memory is shifted out on the SO pin after the output valid time from the clock edge.

If operating in page mode, after the initial word of data is shifted out, the data stored at the next memory location on the page can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each word of data is read out. This can be continued for the entire page length of 32 words long. At the end of the page, the addresses pointer will be wrapped to the 0 word address within the page and the operation can be continuously looped over the 32 words of the same page.

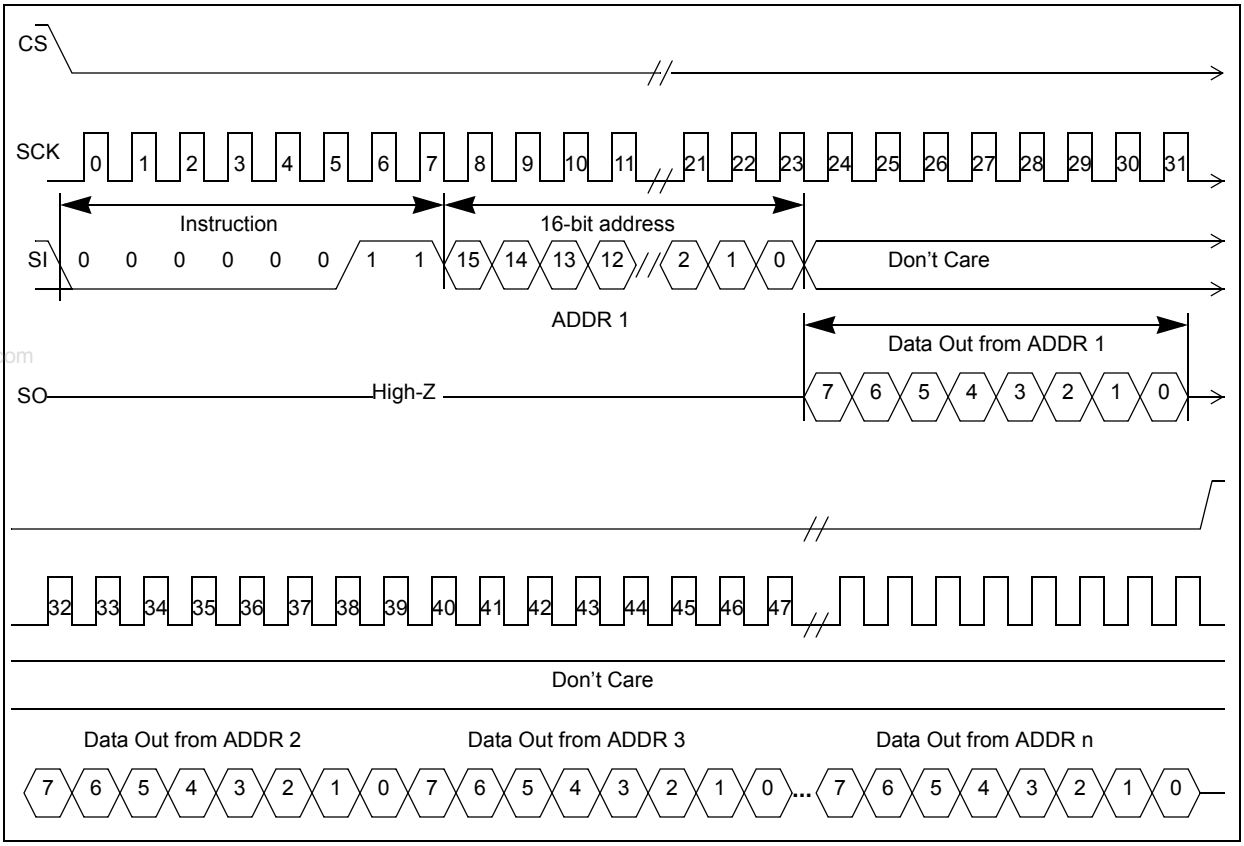
If operating in burst mode, after the initial word of data is shifted out, the data stored at the next memory location can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each word of data is read out. This can be continued for the entire array and when the highest address is reached (1FFFh), the address counter wraps to the address 0000h. This allows the burst read cycle to be continued indefinitely.

All READ operations are terminated by pulling $\overline{CS}$ high.

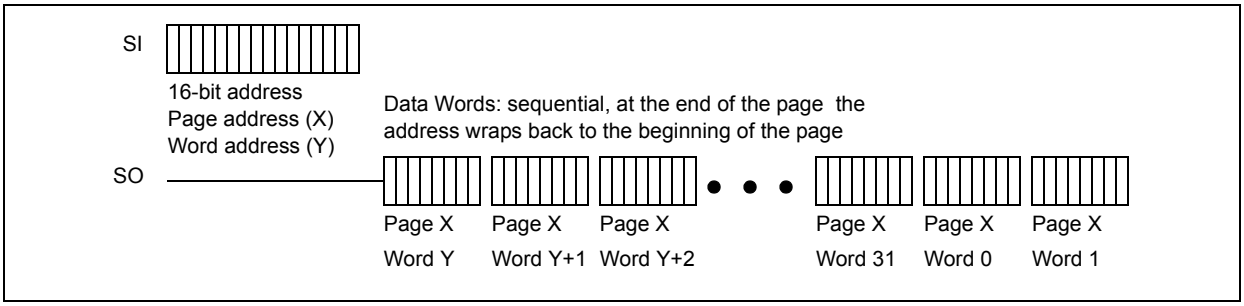
Word READ Sequence



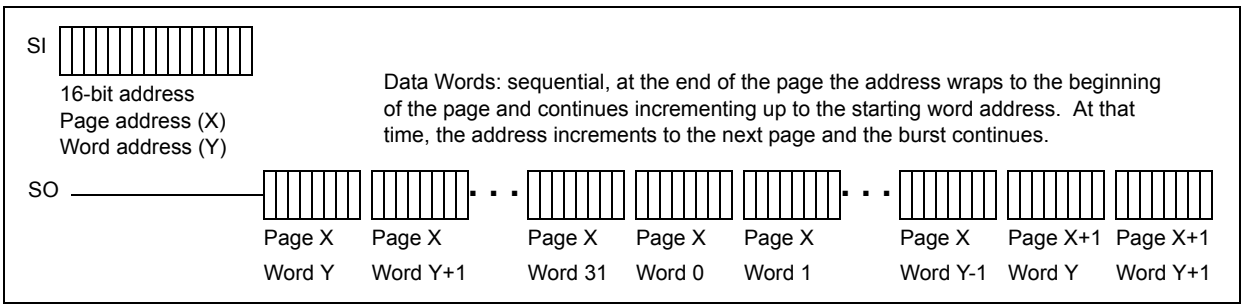
Page and Burst READ Sequence



Page READ Sequence



Burst READ Sequence



WRITE Operations

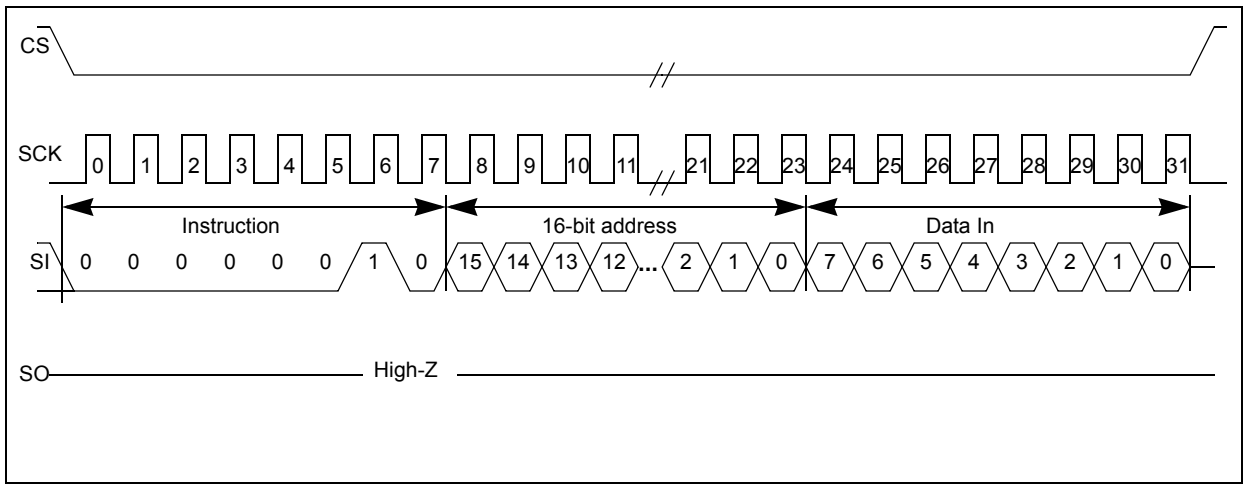
The serial SRAM WRITE is selected by enabling $\overline{CS}$ low. First, the 8-bit WRITE instruction is transmitted to the device followed by the 16-bit address with the 3 MSBs being don't care. After the WRITE instruction and addresses are sent, the data to be stored in memory is shifted in on the SI pin.

If operating in page mode, after the initial word of data is shifted in, additional data words can be written as long as the address requested is sequential on the same page. Simply write the data on SI pin and continue to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each word of data is written in. This can be continued for the entire page length of 32 words long. At the end of the page, the addresses pointer will be wrapped to the 0 word address within the page and the operation can be continuously looped over the 32 words of the same page. The new data will replace data already stored in the memory locations.

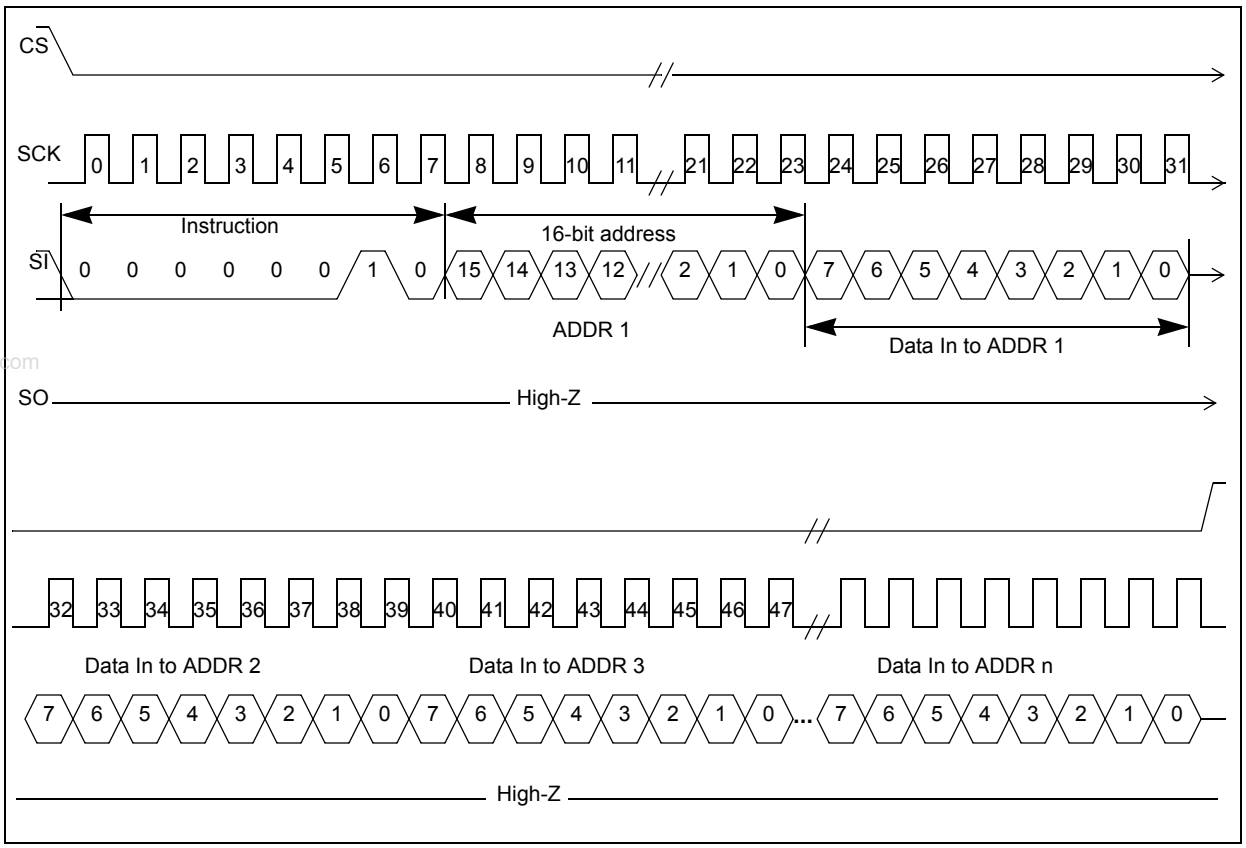
If operating in burst mode, after the initial word of data is shifted in, additional data words can be written to the next sequential memory locations by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each word of data is read out. This can be continued for the entire array and when the highest address is reached (1FFFh), the address counter wraps to the address 0000h. This allows the burst write cycle to be continued indefinitely. Again, the new data will replace data already stored in the memory locations.

All WRITE operations are terminated by pulling $\overline{CS}$ high.

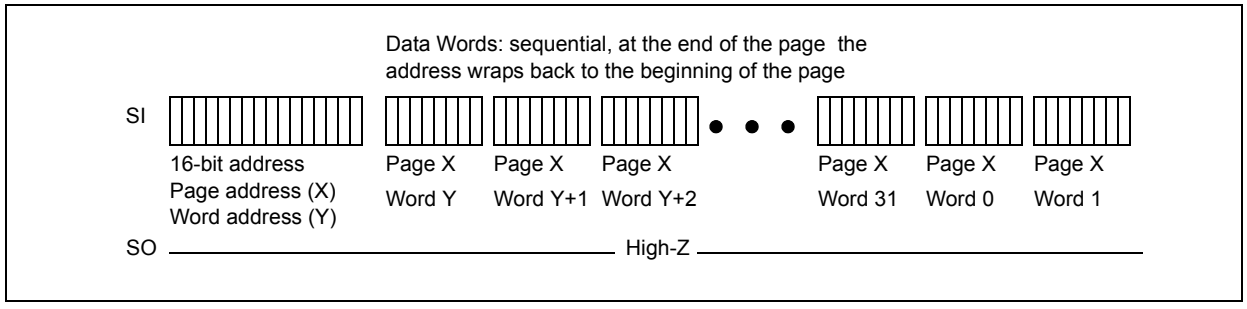
Word WRITE Sequence



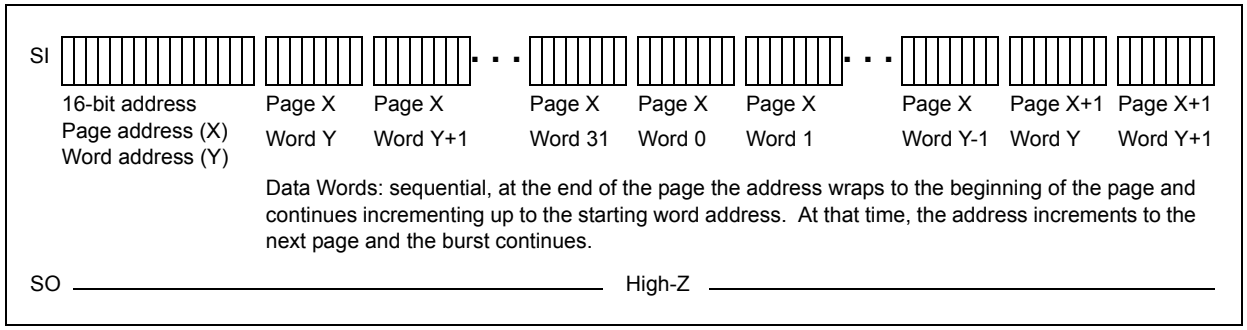
Page and Burst WRITE Sequence



Page WRITE Sequence



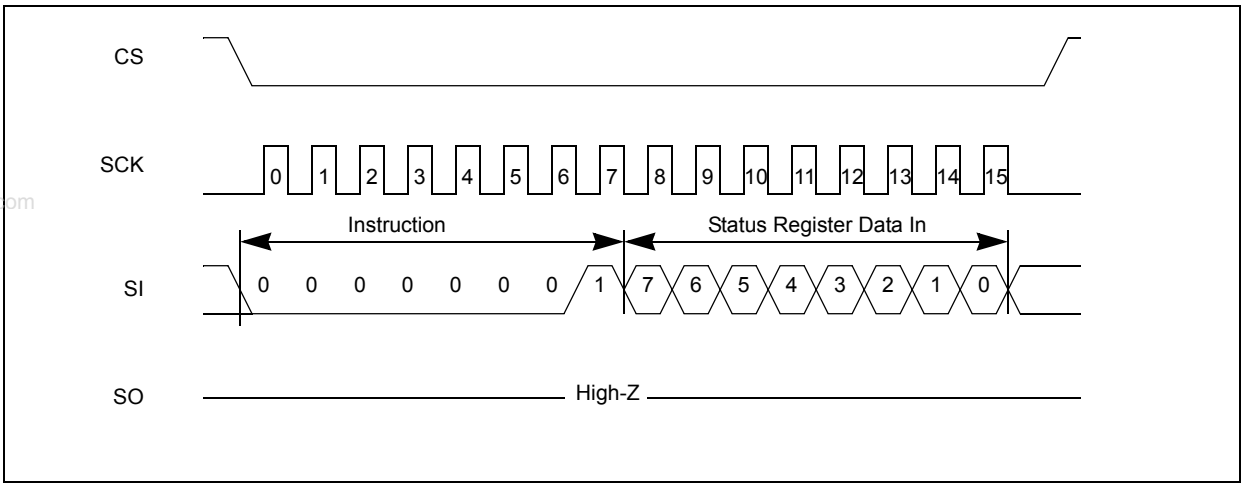
Burst WRITE Sequence



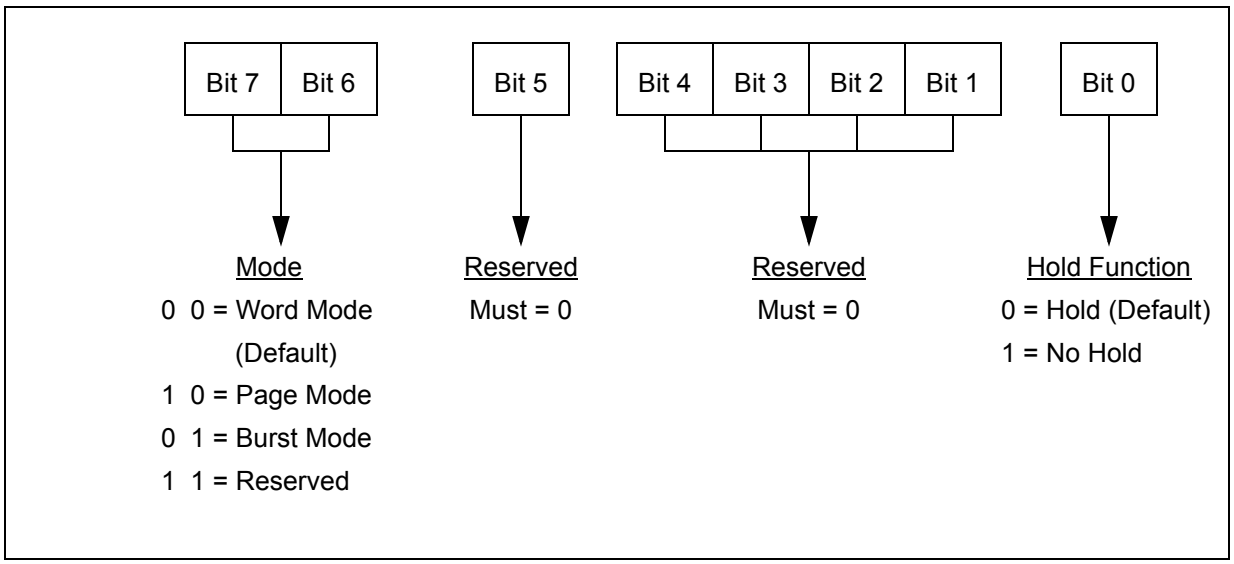
WRITE Status Register Instruction (WRSR)

This instruction provides the ability to write the status register and select among several operating modes. Several of the register bits must be set to a low '0' if any of the other bits are written. The timing sequence to write to the status register is shown below, followed by the organization of the status register.

WRITE Status Register Sequence



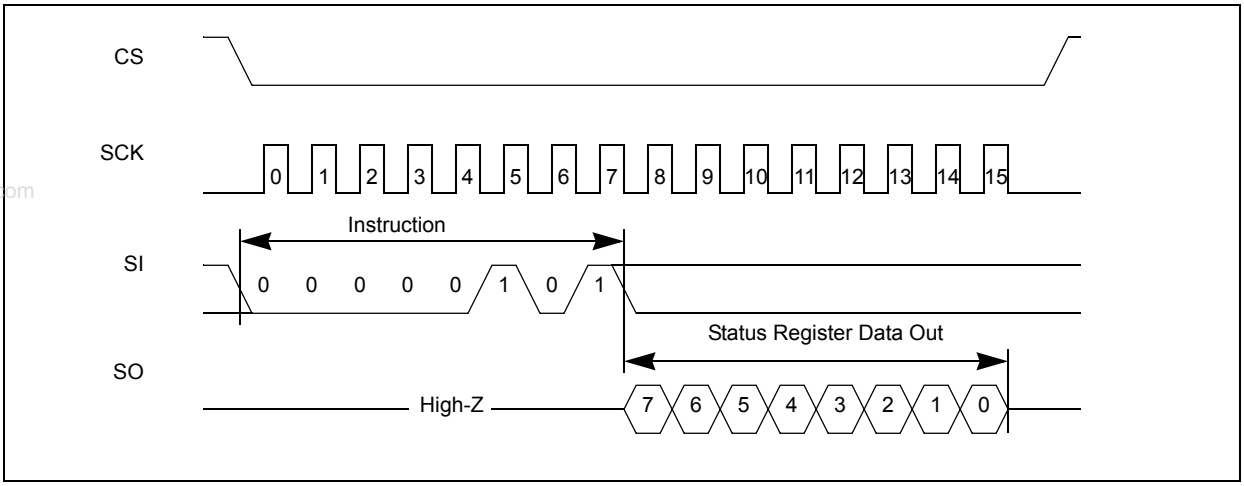
Status Register



READ Status Register Instruction (RDSR)

This instruction provides the ability to read the Status register. The register may be read at any time by performing the following timing sequence.

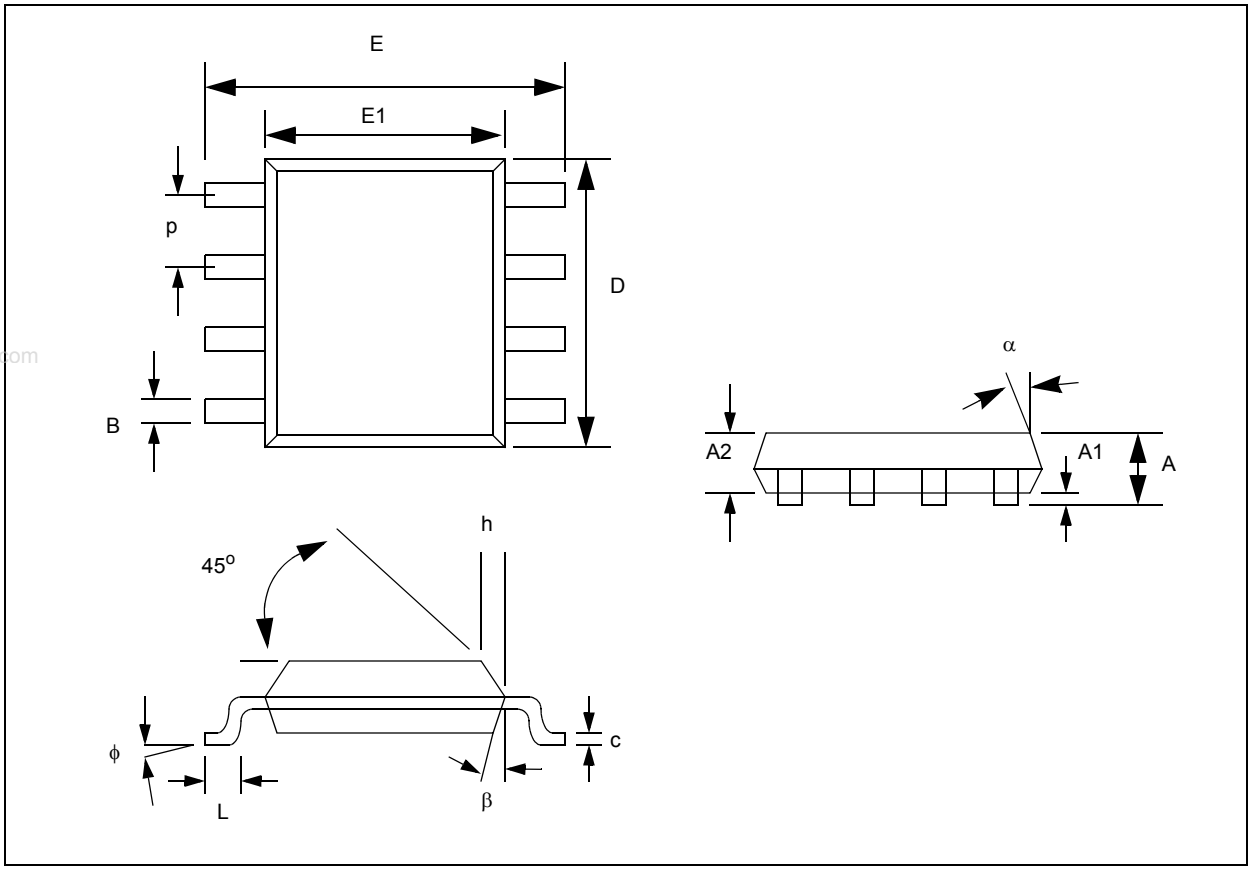
READ Status Register Instruction (RDSR)



Power-Up State

The serial SRAM enters a know state at power-up time. The device is in low-power standby state with $\overline{CS}$ = 1. A low level on $\overline{CS}$ is required to enter a active state.

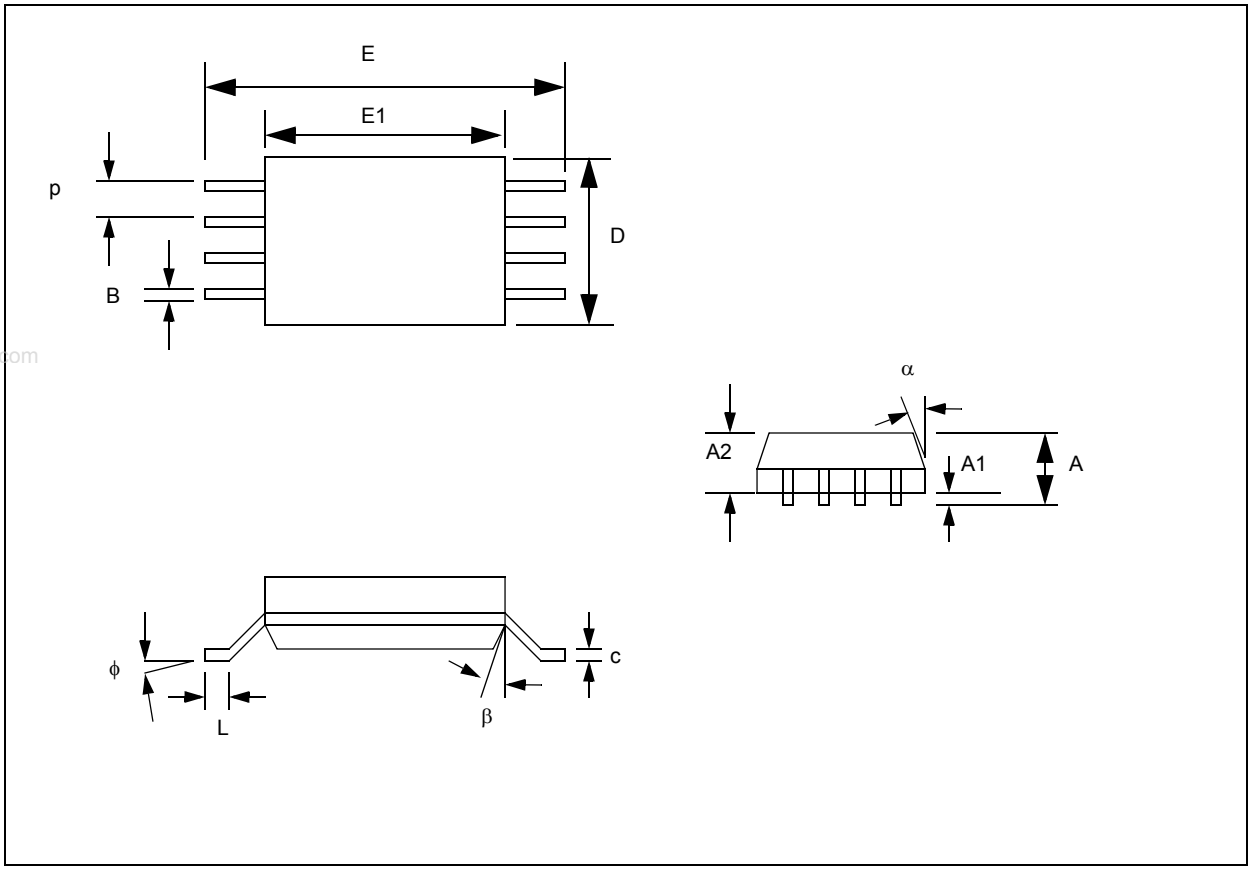
8-Lead Plastic Small Outline, 150mil SOIC



Parameter	Sym	Min	Nom	Max
Pin Pitch	p		1.27	
Overall height	A	1.35	1.55	1.75
Molded Package Thickness	A2	1.32	1.42	1.55
Standoff	A1	0.10	0.18	0.25
Overall Width	E	5.79	6.02	6.20
Molded Package Width	E1	3.71	3.91	3.99
Overall Length	D	4.80	4.90	5.00
Chamfer Distance	h	0.25	0.38	0.51
Foot Length	L	0.48	0.62	0.76
Foot Angle	ϕ	0	4	8
Lead Thickness	c	0.20	0.23	0.25
Lead Width	B	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15
Mold Draft Angle Bottom	β	0	12	15

Note:
1. All dimensions in Millimeters
2. Package dimensions exclude mold flash and protusions.

8-Lead Plastic Thin Shrink Small Outline, 4.4 mm TSSOP



Parameter	Sym	Min	Nom	Max
Pin Pitch	p		0.65	
Overall height	A			1.10
Molded Package Thickness	A2	0.85	0.90	0.95
Standoff	A1	0.05	0.10	0.15
Overall Width	E	6.25	6.38	6.50
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8
Lead Thickness	c	0.09	0.15	0.20
Lead Width	B	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10
Mold Draft Angle Bottom	β	0	5	10

Note:
1. All dimensions in Millimeters
2. Package dimensions exclude mold flash and protusions.

Ordering Information

N64S08 XX XX A X- XX I

- **Performance**: 25 = 25MHz; 20 = 20MHz
- **Package**: S2 = Green SOIC (RoHS Compliant); T2 = Green TSSOP (RoHS Compliant)
- **Function**: HD = Hold Function Input
- **Voltage**: 18 = 1.8V; 30 = 3V

Revision History

Revision #	Date	Change Description
A	October 2005	Initial advance release
B	January 2006	Separated density, removed write protection and added page and burst modes
C	January 2006	Changed packages to green type
D	January 2006	Changed TSSOP pinout to match SOIC
E	September 2006	Split x8 and x16 devices Converted to AMI Semiconductor