## DESCRIPTION

The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.

The 8263 employs active output structures to effect minimum delays: the 8264 utilizes bare collector outputs for expansion of input terms.

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus, eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.

## ORDERING CODE (See Section 9 for further Package and Ordering Information)

| PACKAGES | PIN CONF. | COMMERCIAL RANGES $V_{CC}$=5V ± 5%; $T_A$=0°C to +75°C | MILITARY RANGES $V_{CC}$=5V ± 5%; $T_A$=−55°C to +125°C |
|---|---|---|---|
| Plastic DIP | Fig.A<br>Fig.B | N8263N<br>N8264N | |
| Ceramic DIP | Fig.A<br>Fig.B | N8263F<br>N8264F | S8263F<br>S8264F |
| Flatpak | Fig.A<br>Fig.B | | S8263Q<br>S8264Q |

## TRUTH TABLE

| DATA INPUT $A_n$ | $B_n$ | $C_n$ | CHANNEL SELECT $S_0$ | $S_1$ | DATA COMPLEMENT | OUTPUT ENABLE (8264) | DATA OUTPUTS |
|---|---|---|---|---|---|---|---|
| $A_n$ | X | X | H | H | L | H | $A_n$ |
| X | $B_n$ | X | L | H | L | H | $B_n$ |
| X | X | $C_n$ | H | L | L | H | $C_n$ |
| X | X | X | L | L | L | H | 0 |
| $A_n$ | X | X | H | H | H | H | $\overline{A}_n$ |
| X | $B_n$ | X | L | H | H | H | $\overline{B}_n$ |
| X | X | $C_n$ | H | L | H | H | $\overline{C}_n$ |
| X | X | X | L | L | H | H | H |
| X | X | X | X | X | X | L | H |

H = HIGH
L = LOW
X = Don't care

## PIN CONFIGURATIONS

8263

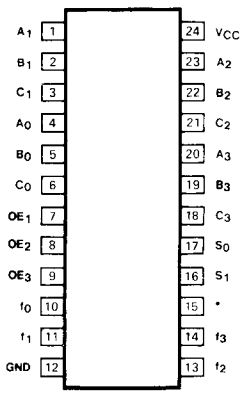



Figure A

8264

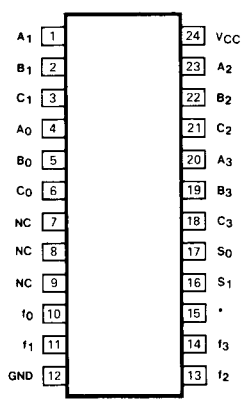
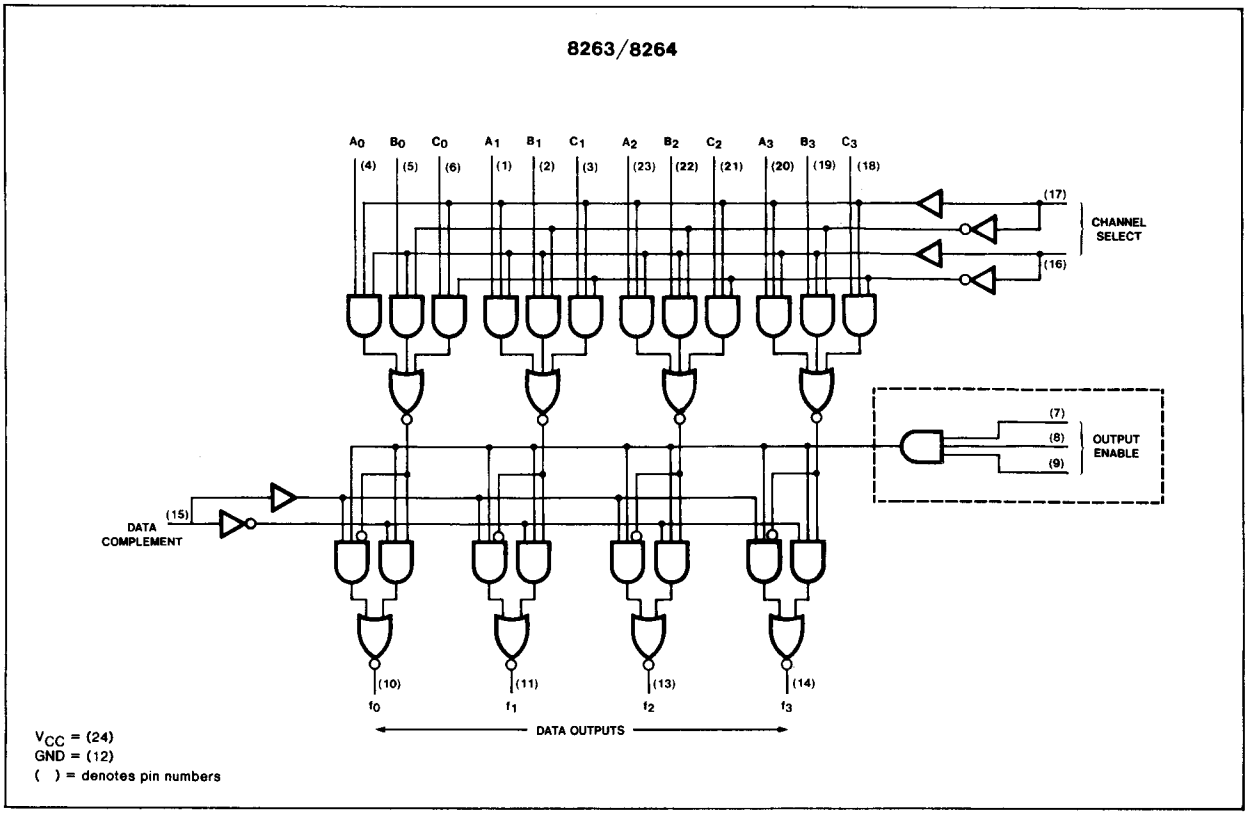



Figure B

*Data complement

## LOGIC DIAGRAM




## DC ELECTRICAL CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | 8263 | | 8264 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $V_{OH}$ | Output HIGH voltage | $V_{CC}$ = 4.75V, $I_{OH}$ = −800μA | 2.6 | | | | V |
| $I_{OH}$ | Output HIGH current | $V_{CC}$ = 4.75V, $V_{OUT}$ = 2.0V | | | | 200 | μA |
| $V_{OL}$ | Output LOW voltage<br>8263<br>8264 | $V_{CC}$ = 4.75V,<br>$I_{OL}$ = 9.6mA<br>$I_{OL}$ = 16.mA | | 0.4 | | 0.4 | V |
| $I_{IL}$ | Input LOW current<br>$A_n$,$B_n$,$C_n$,OE,DC<br>$S_0$,$S_1$ | $V_{CC}$ = 5.25V, $V_{IN}$ = 4.5V | | <br>−1.6<br>−3.2 | | <br>−1.6<br>−3.2 | <br>mA<br>mA |
| $I_{IH}$ | Input HIGH current<br>$A_n$,$B_n$,$C_n$,OE,DC<br>$S_0$,$S_1$ | $V_{CC}$ = 5.25V, $V_{IN}$ = 4.5V | | <br>40<br>80 | | <br>40<br>80 | <br>μA<br>μA |
| $I_{OS}$ | Output short circuit current | $V_{CC}$ = 5V, $V_{OUT}$ = OV | −20 | −70 | | | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = 5.25V | | 80 | | 90.4 | mA |

## AC CHARACTERISTICS: $T_A$ = 25°C (See Section 4 for Waveforms and Conditions)

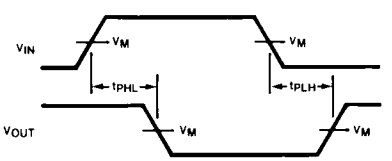
| PARAMETER | | TEST CONDITIONS | 8263 $C_L$ = 18pF $R_1$ = ∞Ω $R_2$ = 150Ω | | 8264 $C_L$ = 30pF $R_1$ = 360Ω $R_2$ = 440Ω | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$A_n$ to $f_n$ | Figures 1 & 2 | | 26<br>26 | | 36<br>36 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$S_0$, $S_1$ to $f_n$ | Figures 1 & 2 | | 36<br>36 | | 36<br>36 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>DC to $f_n$ | Figures 1 & 2 | | 26<br>26 | | 30<br>30 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>OE to $f_n$ | Figure 1 | | | | 30<br>30 | ns<br>ns |

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

## AC WAVEFORMS

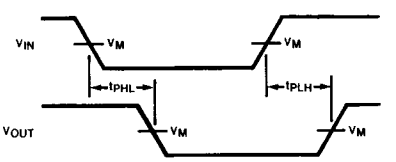
**WAVEFORM FOR INVERTING OUTPUTS**




$V_M$ = 1.5V

**Figure 1**

**WAVEFORM FOR NON-INVERTING OUTPUTS**




$V_M$ = 1.5V

**Figure 2**



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