

Document No.	853-0033
ECN No.	96054
Date of Issue	March 14, 1989
Status	Product Specification
Memory Products	

# 82LS135

## 2K-bit TTL bipolar PROM

### DESCRIPTION

The 82LS135 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82LS135 includes on-chip decoding and two Chip Enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

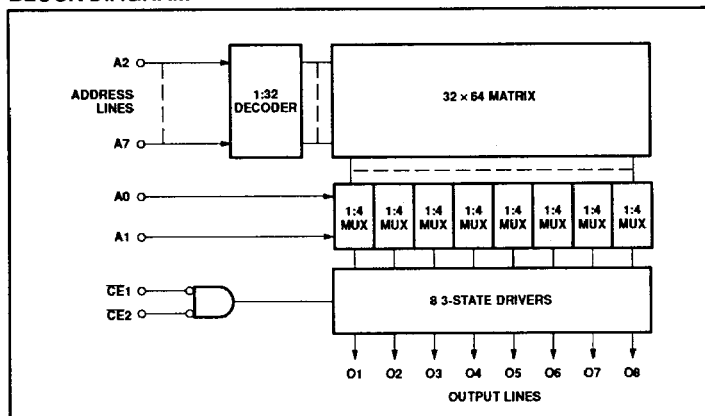
### FEATURES

- Address access time: 100ns max
- Power dissipation: 200 $\mu$ W/bit typ
- Input loading: -100 $\mu$ A max
- Two Chip Enable inputs
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Unprogrammed outputs are Low level
- Outputs: 3-State

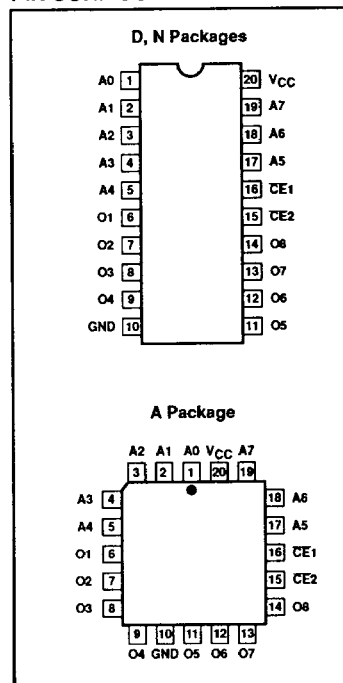
### APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

### BLOCK DIAGRAM



### PIN CONFIGURATIONS



## 2K-bit TTL bipolar PROM (256 × 8)

82LS135

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	N82LS135 N
20-Pin Plastic Small Outline 300mil-wide	N82LS135 D
20-Pin Plastic Leaded Chip Carrier 350mil-square	N82LS135 A

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	+7.0	$V_{DC}$
$V_{IN}$	Input voltage	+5.5	$V_{DC}$
$V_O$	Output voltage Off-State	+5.5	$V_{DC}$
$T_{amb}$	Operating temperature range	0 to +75	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

## DC ELECTRICAL CHARACTERISTICS

0°C ≤  $T_{amb}$  ≤ +75°C, 4.75V ≤  $V_{CC}$  ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1,2</sup>	LIMITS			UNIT
			Min	Typ <sup>3</sup>	Max	
<b>Input voltage</b>						
$V_{IL}$	Low	$I_{IN} = -12mA$	2.0		0.8	V
$V_{IH}$	High					V
$V_{IC}$	Clamp				-1.2	V
<b>Output voltage</b>						
$V_{OL}$	Low	$I_{OUT} = 16mA$	2.4		0.5	V
$V_{OH}$	High	$I_{OUT} = -2mA$ , High stored			V	
<b>Input current</b>						
$I_{IL}$	Low	$V_{IN} = 0.45V$			-100	μA
$I_{IH}$	High	$V_{IN} = 5.5V$			40	μA
<b>Output current</b>						
$I_{OZ}$	Hi-Z state	$CE1, CE2 = High, V_{OUT} = 0.5V$			-40	μA
$I_{OS}$	Short circuit <sup>4</sup>	$CE1, CE2 = High, V_{OUT} = 5.5V$			40	μA
		$CE1, CE2 = Low, V_{OUT} = 0V$ , High stored	-15		-75	mA
<b>Supply current<sup>5</sup></b>						
$I_{CC}$		$V_{CC} = 5.25V$		80	100	mA
<b>Capacitance</b>						
$C_{IN}$	Input	$V_{CC} = 5.0V, CE = High$		5		pF
$C_{OUT}$	Output	$V_{IN} = 2.0V$ $V_{OUT} = 2.0V$		8		pF

## NOTES:

- Positive current is defined as into the terminal referenced.
- All voltages with respect to network ground.
- Typical values are at  $V_{CC} = 5V, T_{amb} = +25°C$ .
- Duration of short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

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## AC ELECTRICAL CHARACTERISTICS

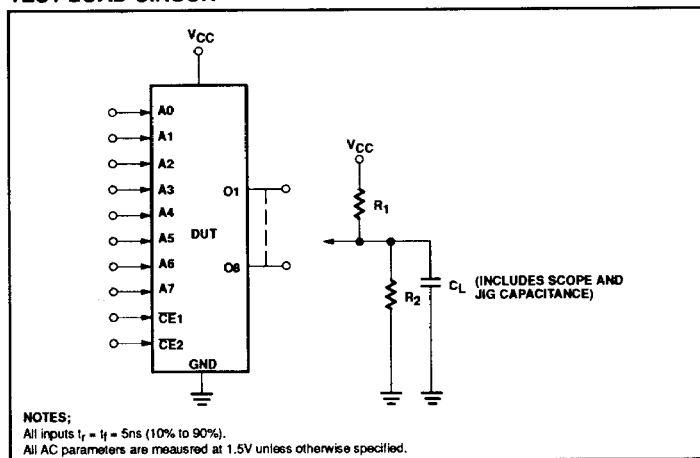
$R_1 = 270\Omega$ ,  $R_2 = 600\Omega$ ,  $C_L = 30\text{pF}$ ,  $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ <sup>1</sup>	Max	
<b>Access time<sup>2</sup></b>							
$t_{AA}$		Output	Address		70	100	ns
$t_{CE}$		Output	Chip Enable		30	50	ns
<b>Disable time<sup>3</sup></b>							
$t_{CD}$		Output	Chip Disable		30	60	ns

**NOTES:**

1. Typical values are at  $V_{\text{CC}} = 5\text{V}$ ,  $T_{\text{amb}} = +25^\circ\text{C}$ .
2. Tested at an address cycle time of  $1\mu\text{s}$ .
3. Measured at a delta of 0.5V from Logic Level with  $R_1 = 750\Omega$ ,  $R_2 = 750\Omega$ ,  $C_L = 5\text{pF}$ .

### TEST LOAD CIRCUIT



### VOLTAGE WAVEFORMS

