intel®

# 809XBH/839XBH/879XBH ADVANCED 16-BIT MICROCONTROLLER WITH 8- OR 16-BIT EXTERNAL BUS

*Automotive*

- **Extended Automotive Temperature Range (−40°C to +125°C Case)**
- **High Performance NMOS Process**
- **8 Kbytes On-Chip ROM/EPROM**
- **232 Byte Register RAM**
- **Register-to-Register Architecture**
- **10-Bit A/D Converter with S/H**
- **Five 8-Bit I/O Ports**
- **20 Interrupt Sources**
- **8-Bit Pulse-Width Modulated Output**
- **Run-Time Programmable EPROM**
- **Full Duplex Serial Port**
- **High-Speed I/O Subsystem**
- **Full Duplex Serial Port**
- **Dedicated Baud Rate Generator**
- **6.25 μs 16 x 16 Multiply**
- **6.25 μs 32/16 Divide**
- **16-Bit Watchdog Timer**
- **Four 16-Bit Software Timers**
- **Two 16-Bit Counters/Timers**
- **Available in 68-Pin PLCC, PFP and CFP; 48-Pin PDIP Package**
  (See Packaging Specifications, Order # 231369)

The 8X9XBH family of 16-bit microcontrollers consists of many members, all of which are designed for high-speed control functions. The 8X9XBH family members produced for the automotive environment, using Intel's HMOS-III process, with 8 Kbytes of ROM (or ROMless) and 232 total bytes of on-chip RAM, 256 bytes of register RAM are described in this datasheet.

The CPU supports bit, byte, and word operations. Thirty-two-bit double words are supported for a subset of the instruction set. With a 12 MHz input frequency the 8X9XBH can do a 16-bit addition in 1.0 μs and a 16 x 16-bit multiply or 32/16 divide in 6.25 μs. Instruction execution times average 1 μs to 2 μs in typical applications.

Four high-speed capture inputs are provided to record the times at which external events occur stored in an eight-level FIFO. Rising, falling, rising and falling, or every eight rising edges can be recorded every 2.25 μs using 12 MHz clock. Interrupts can be programmed for every FIFO entry, or every 6th FIFO entry.

Up to 6 high-speed pulse generator outputs are provided to trigger external events at preset times. The high-speed output unit can simultaneously perform software timer functions, start A/D conversions, or pulse one or more outputs. Up to four 16-bit software timers can be in operation at once.

The on-chip A/D converter includes a Sample and Hold (S/H), and converts up to 8 multiplexed analog input channels to a 10-bit digital result. With a 12 MHz input frequency, each conversion takes as little as 22 μs. A/D conversions can be performed at preprogrammed times, or asynchronously.

Also provided on-chip are: a full duplex, double buffered receive serial port with 3 asynchronous and 1 synchronous modes; a 16-bit watchdog timer, and a 256 state pulse-width modulated output signal.

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**NOTICE:**

This datasheet contains information on products in full production. Specifications within this datasheet are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

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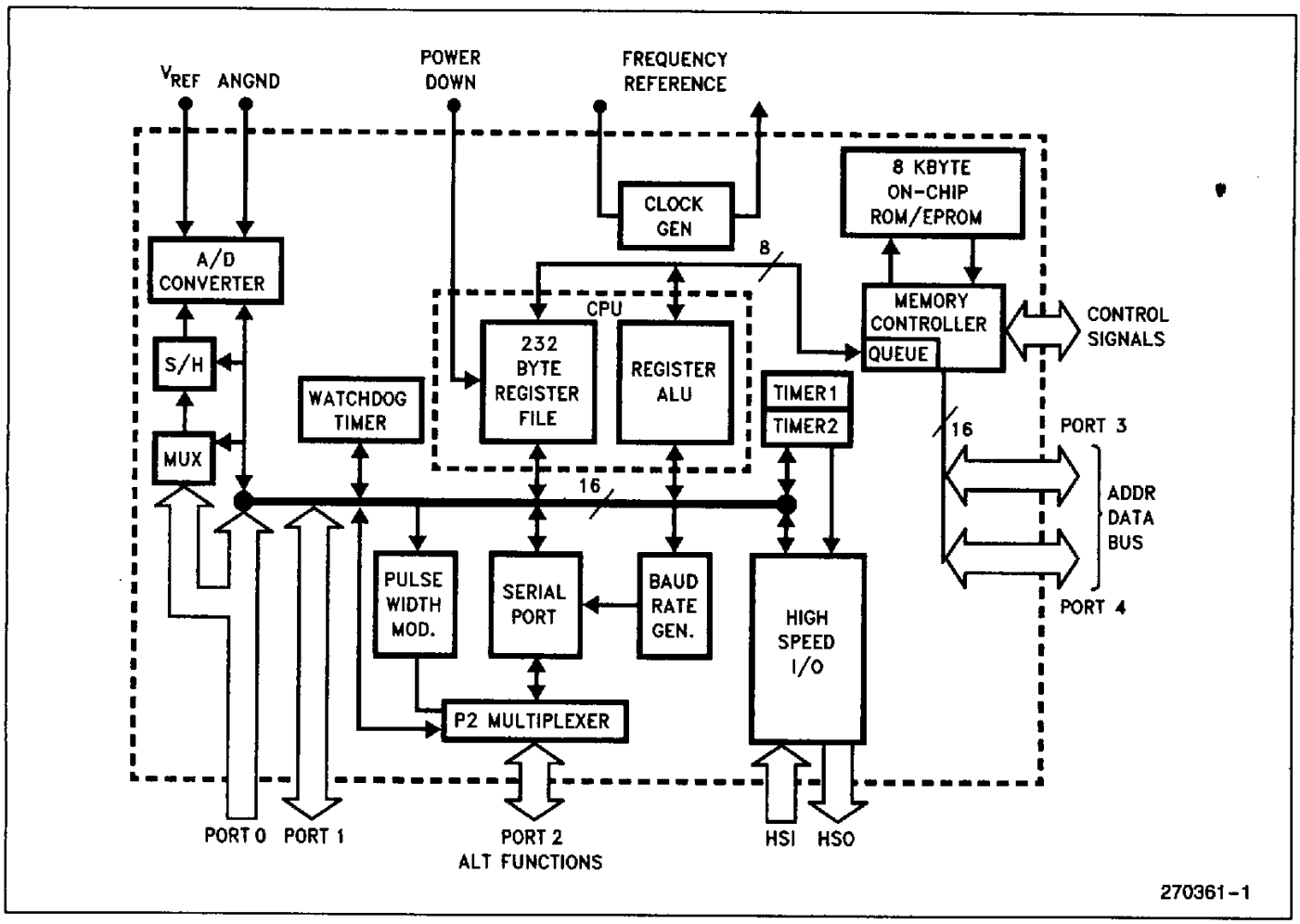


**Figure 1. MCS® 96 Microcontroller Block Diagram**

## PRODUCT/PACKAGING OPTIONS

The 8X9XBH is available in 48 and 68-pin packages, with and without on-chip ROM or EPROM. The 8X9XBH nomenclature is shown in Figure 2. Figures 3, 4 and 6 show the pinouts for all available 68-pin packages: Plastic Leaded Chip Carrier (PLCC), Plastic Flatpack (PFP) and Ceramic Flatpack (CFP). Figure 5 shows the pinout for the 48-pin Plastic Dip Package (PDIP).

The 8X9XBH is also available in three temperature range options: Commercial (0°C to +70°C), Extended (−40°C to +85°C) and Automotive (−40°C to +125°C). Intel's extended and automotive temperature range products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The automotive, extended, and commercial temperature versions of the 8X9XBH product families are available with or without burn-in options as listed in Table 1.

As shown in Figure 2, temperature, burn-in and package options are indentified by a one- or two-letter prefix to the part number. It also illustrates the 8X9XBH family nomenclature for ROM/EPROM/ROMless, with/without A/D, and process.

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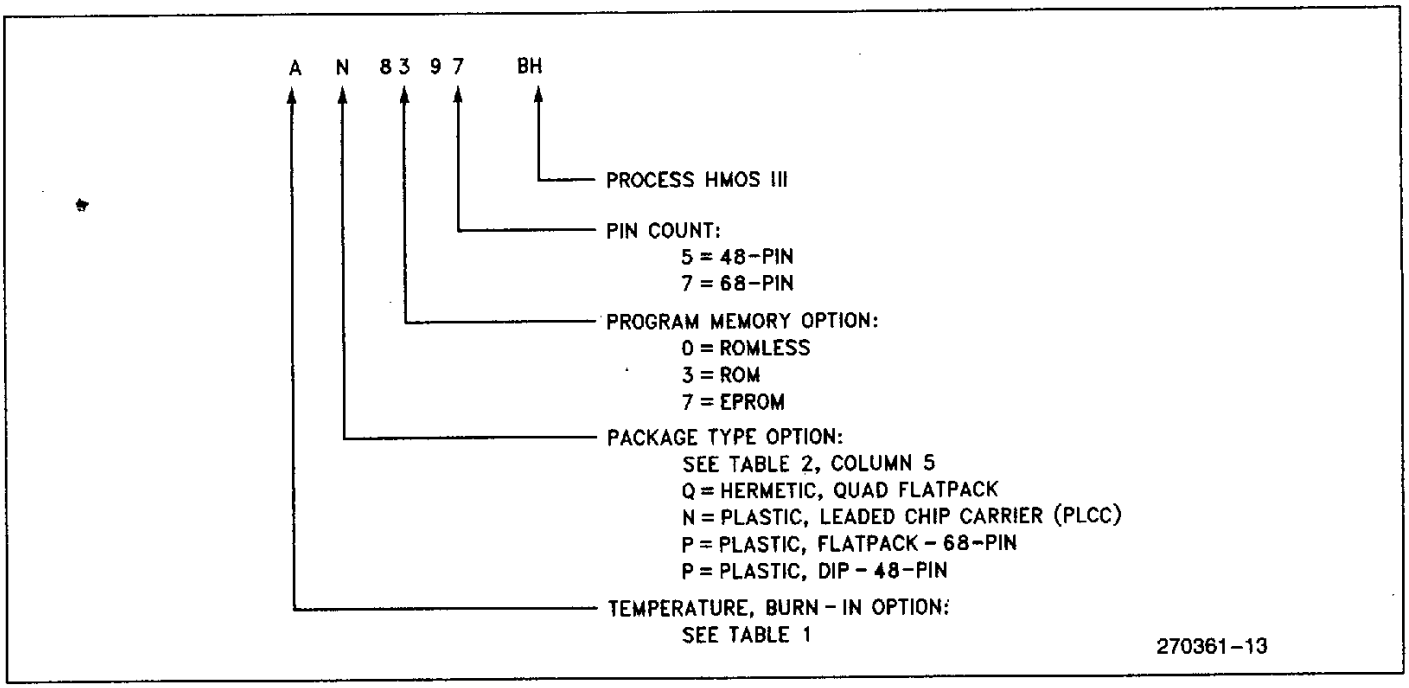



**Figure 2. The 8X9XBH Family Nomenclature**

**Table 1. Temperature — Burn-In Option**

| Temperature Classification | Temperature Designation | Operating Temperature | Burn-In 125°C (Hr) |
|---|---|---|---|
| Commercial | Null | 0°C to +70°C Ambient | 6 |
| Extended | T | −40°C to +85°C Ambient | 6 |
| Automotive | A | −40°C to +125°C Case | 6 |
| | H | −40°C to +125°C Case | 6 |

**NOTES:**
1. Burn-in is dynamic at +125°C, $V_{CC}$ = 7.3V ±0.25V, for 6 hours.
2. Other burn-in durations are also available, but not standard.

**Table 2. The 8X9XBH Family Packages**

| | | |
|---|---|---|
| ROMless | 68-Pin | N8097BH-PLCC |
| | 68-Pin | P8097BH-PFP |
| | 48-Pin | P8095BH-P-DIP |
| ROM (8 Kbytes) | 68-Pin | N8397BH-PLCC |
| | 68-Pin | P8397BH-PFP |
| | 48-Pin | P8395BH-P-DIP |
| EPROM (8 Kbytes) | 68-Pin | Q8797BH-CFP |
| | 48-Pin | C8795BH-DIP |

| PFP/CFP | 48-Pin P-DIP | 68-Pin PLCC | Description | PFP/CFP | 48-Pin P-DIP | 68-Pin PLCC | Description |
|---|---|---|---|---|---|---|---|
| 1 | 41 | 9 | ACH7/P0.7 | 35 | 16 | 43 | READY |
| 2 | 40 | 8 | ACH6/P0.6 | 36 | — | 42 | T2RST/P2.4 |
| 3 | — | 7 | ACH2/P0.2 | 37 | 15 | 41 | $\overline{BHE}/\overline{WRH}$ |
| 4 | — | 6 | ACH0/P0.0 | 38 | 14 | 40 | $\overline{WR}/\overline{WRL}$ |
| 5 | — | 5 | ACH1/P0.1 | 39 | 13 | 39 | PWM/P2.5 |
| 6 | — | 4 | ACH3/P0.3 | 40 | — | 38 | P2.7/T2CAPTURE |
| 7 | — | 3 | NMI | 41 | 12 | 37 | $V_{PP}$ |
| 8 | 39 | 2 | $\overline{EA}$ | 42 | 11 | 36 | $V_{SS}$ |
| 9 | 38 | 1 | $V_{CC}$ | 43 | 10 | 35 | HSO.3 |
| 10 | 37 | 68 | $V_{SS}$ | 44 | 9 | 34 | HSO.2 |
| 11 | 36 | 67 | XTAL1 | 45 | — | 33 | P2.6 |
| 12 | 35 | 66 | XTAL2 | 46 | — | 32 | P1.7 |
| 13 | — | 65 | CLKOUT | 47 | — | 31 | P1.6 |
| 14 | — | 64 | BUSWIDTH | 48 | — | 30 | P1.5 |
| 15 | — | 63 | INST | 49 | 8 | 29 | HSO.1 |
| 16 | 34 | 62 | ALE/$\overline{ADV}$ | 50 | 7 | 28 | HSO.0 |
| 17 | 33 | 61 | $\overline{RD}$ | 51 | 6 | 27 | HSO.5/HSI.3 |
| 18 | 32 | 60 | AD0/P3.0 | 52 | 5 | 26 | HSO.4/HSI.2 |
| 19 | 31 | 59 | AD1/P3.1 | 53 | 4 | 25 | HSI.1 |
| 20 | 30 | 58 | AD2/P3.2 | 54 | 3 | 24 | HSI.0 |
| 21 | 29 | 57 | AD3/P3.3 | 55 | — | 23 | P1.4 |
| 22 | 28 | 56 | AD4/P3.4 | 56 | — | 22 | P1.3 |
| 23 | 27 | 55 | AD5/P3.5 | 57 | — | 21 | P1.2 |
| 24 | 26 | 54 | AD6/P3.6 | 58 | — | 20 | P1.1 |
| 25 | 25 | 53 | AD7/P3.7 | 59 | — | 19 | P1.0 |
| 26 | 24 | 52 | AD8/P4.0 | 60 | 2 | 18 | TXD/P2.0 |
| 27 | 23 | 51 | AD9/P4.1 | 61 | 1 | 17 | RXD/P2.1 |
| 28 | 22 | 50 | AD10/P4.2 | 62 | 48 | 16 | $\overline{RESET}$ |
| 29 | 21 | 49 | AD11/P4.3 | 63 | 47 | 15 | EXTINT/P2.2 |
| 30 | 20 | 48 | AD12/P4.4 | 64 | 46 | 14 | $V_{PD}$ |
| 31 | 19 | 47 | AD13/P4.5 | 65 | 45 | 13 | $V_{REF}$ |
| 32 | 18 | 46 | AD14/P4.6 | 66 | 44 | 12 | ANGND |
| 33 | 17 | 45 | AD15/P4.7 | 67 | 43 | 11 | ACH4/P0.4 |
| 34 | — | 44 | T2CLK/P2.3 | 68 | 42 | 10 | ACH5/P0.5 |

**Figure 3. PFP/CFP, P-DIP and PLCC Functional Pinouts**

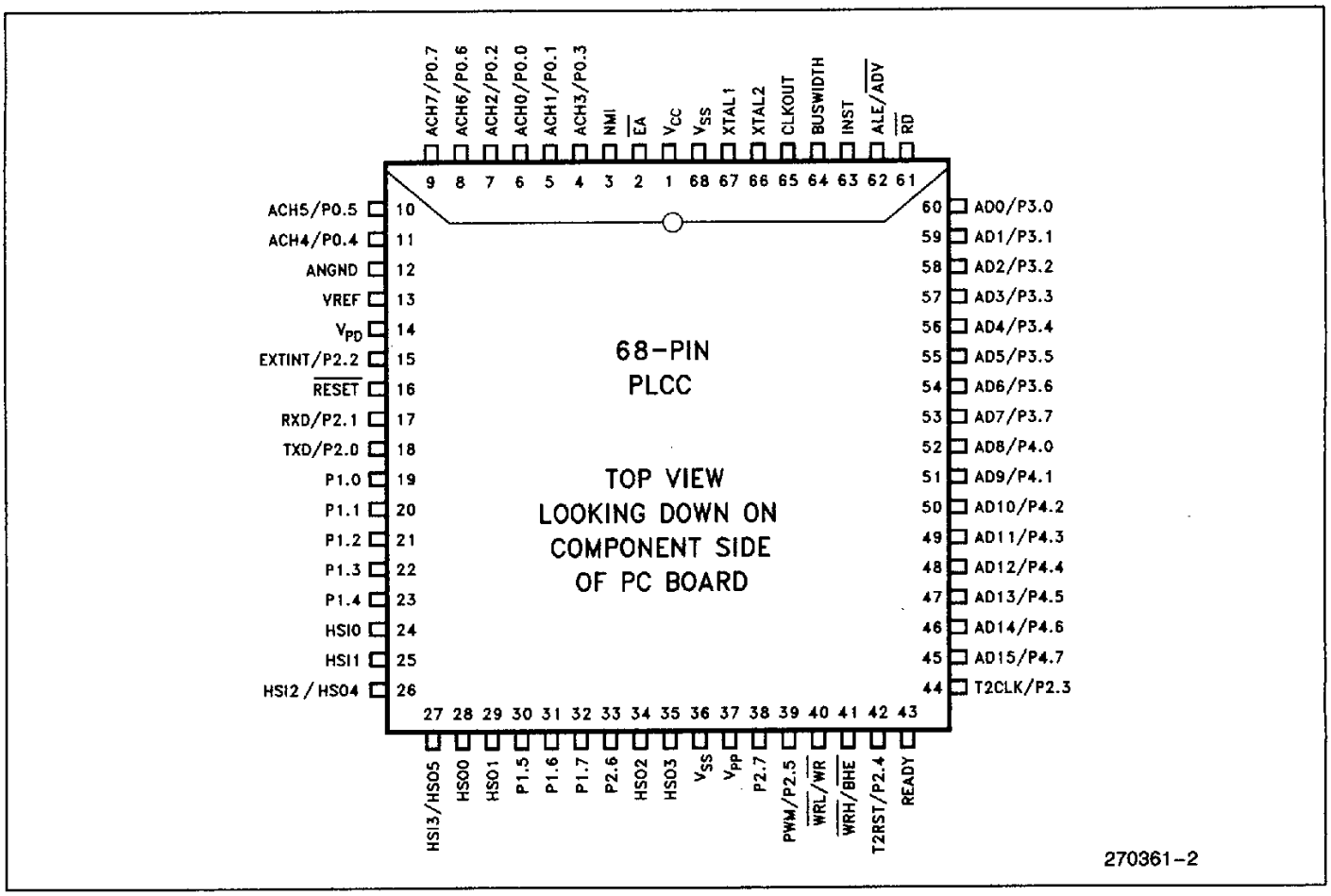



**Figure 4. 68-Pin PLCC Package**

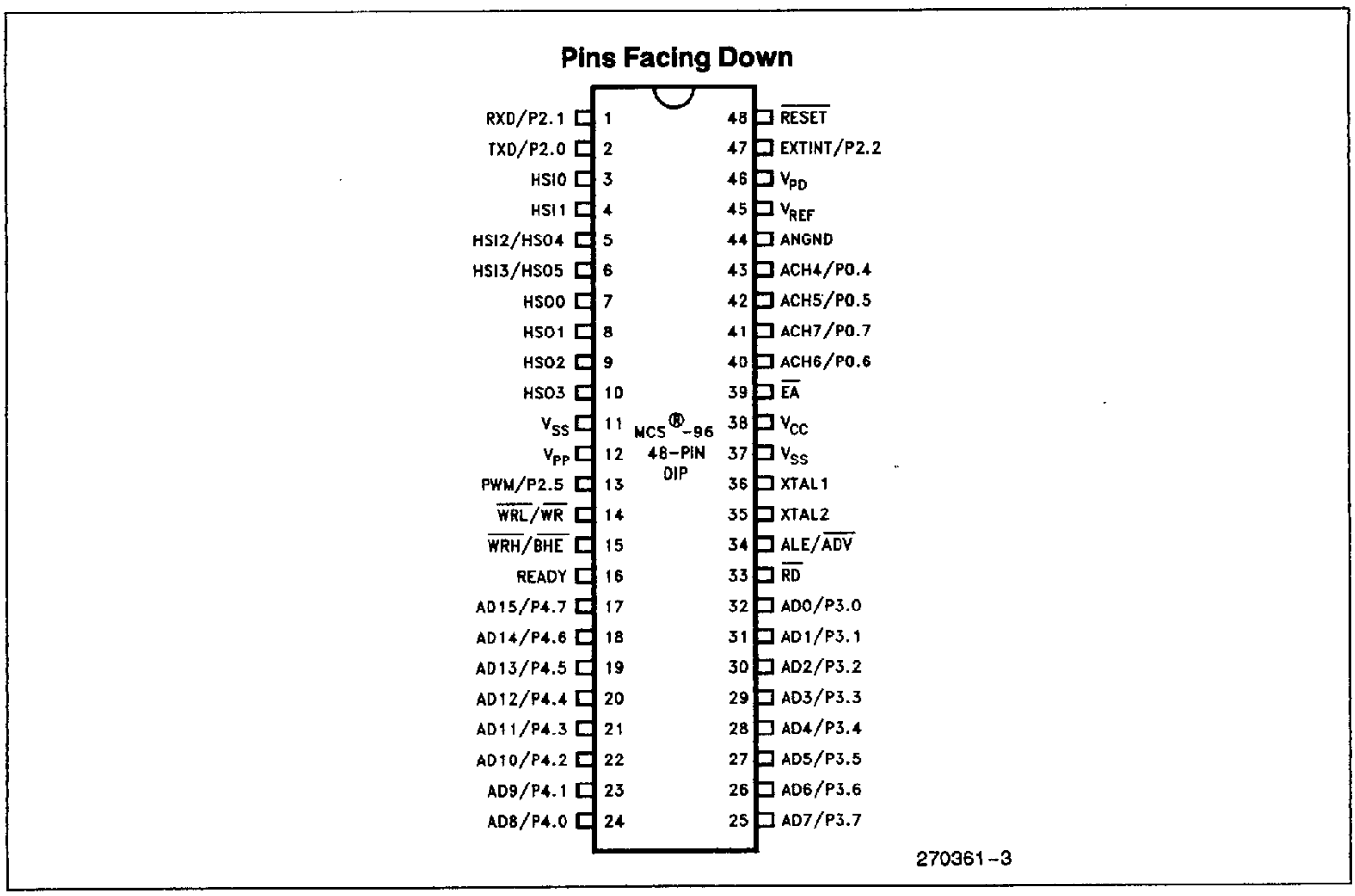



**Figure 5. 48-Pin P-DIP Package**

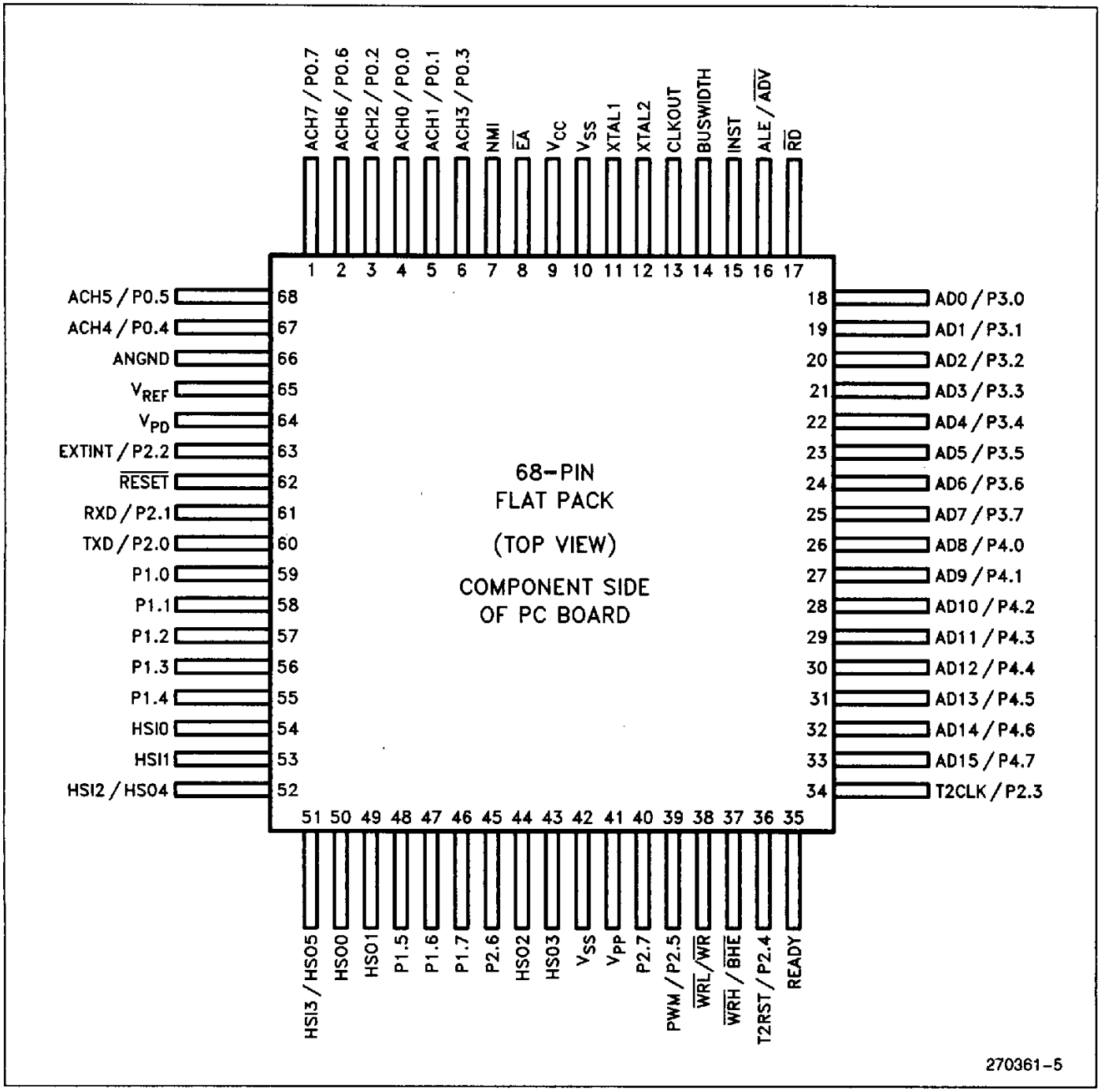



**Figure 6. 68-Pin Package (Flat Pack—Top View)**

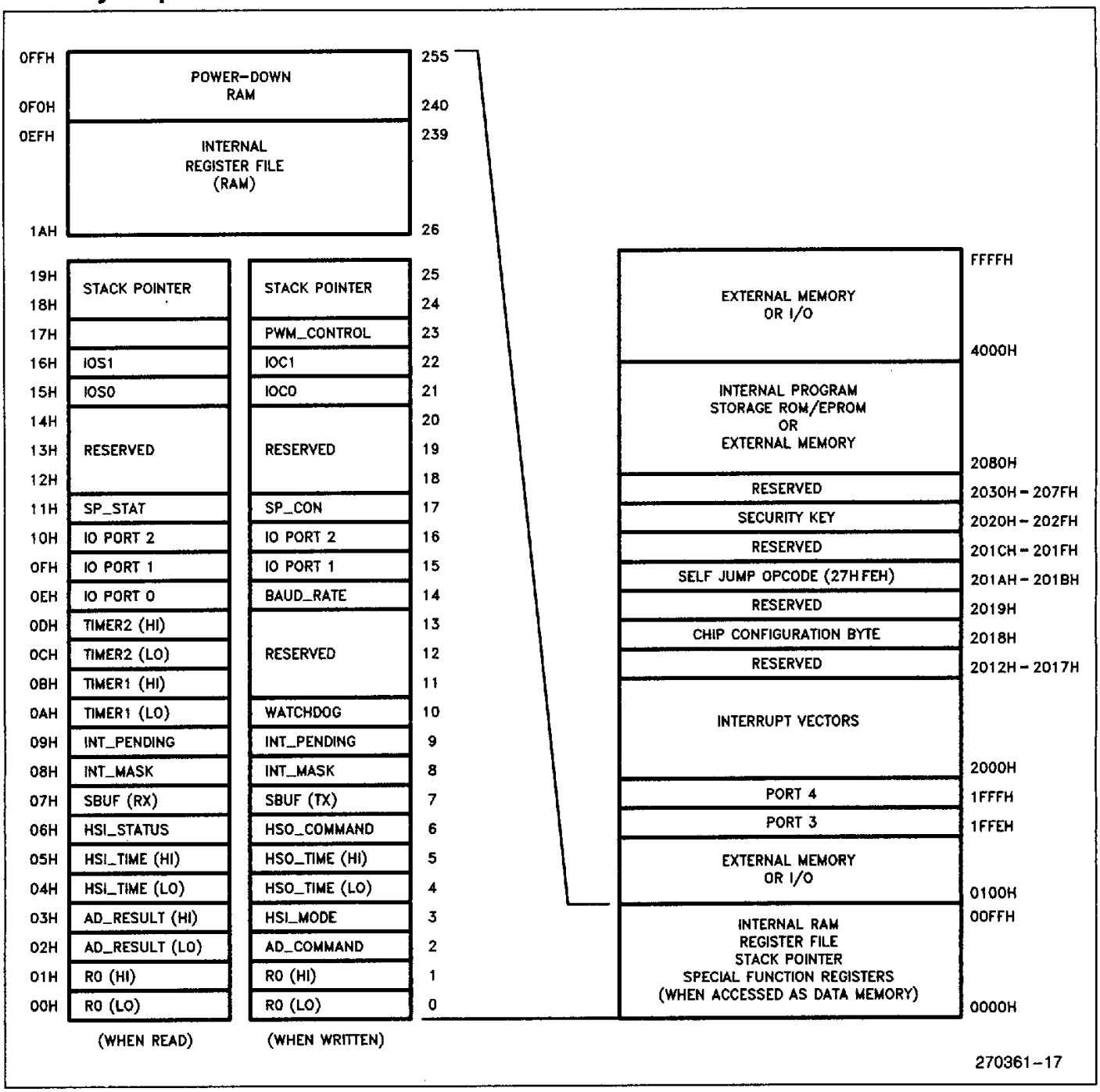
## PIN DESCRIPTIONS

| Symbol | Name and Function |
|---|---|
| $V_{CC}$ | Main supply voltage (5V). |
| $V_{SS}$ | Digital circuit ground (0V). There are two $V_{SS}$ pins, both of which must be connected. |
| $V_{PD}$ | RAM standby supply voltage (5V). This voltage must be present during normal operation. In a Power Down condition (i.e. $V_{CC}$ drops to zero), if $\overline{RESET}$ is activated before $V_{CC}$ drops below spec and $V_{PD}$ continues to be held within spec., the top 16 bytes in the Register File will retain their contents. $\overline{RESET}$ must be held low during the Power Down and should not be brought high until $V_{CC}$ is within spec and the oscillator has stabilized. |
| $V_{REF}$ | Reference voltage for the A/D converter (5V). $V_{REF}$ is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function. |
| ANGND | Reference ground for the A/D converter. Must be held at nominally the same potential as $V_{SS}$. |
| $V_{PP}$ | Programming voltage for the EPROM parts. It should be +12.75V for programming. This pin is $V_{BB}$ on 8X9X-90 parts. Systems that have this pin connected to ANGND through a capacitance (required on 8X9X-90 parts) do not need to change. Otherwise, tie to $V_{CC}$. |
| XTAL1 | Input of the oscillator inverter and of the internal clock generator. |
| XTAL2 | Output of the oscillator inverter. |
| CLKOUT | Output of the internal clock generator. The frequency of CLKOUT is 1/3 the oscillator frequency. It has a 33% duty cycle. |
| $\overline{RESET}$ | Reset input to the chip. Input low for at least 2 state times to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. $\overline{RESET}$ has an internal pullup. |
| BUSWIDTH | Input for bus width selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is high, a 16-bit bus cycle occurs. If BUSWIDTH is low, an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. This pin is the $\overline{TEST}$ pin on 8X9X-90 parts. Systems with $\overline{TEST}$ tied to $V_{CC}$ do not need to change. If this pin is left unconnected, it will rise to $V_{CC}$. |
| NMI | A positive transition causes a vector to external memory location 0000H. External memory from 00H through 0FFH is reserved for Intel development systems. |
| INST | Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses. |
| $\overline{EA}$ | Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{EA}$ has an internal pulldown, so it goes low unless driven otherwise. $\overline{EA}$ is latched at reset. |

## PIN DESCRIPTIONS (Continued)

| Symbol | Name and Function |
|---|---|
| ALE/$\overline{ADV}$ | Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive high at the end of the bus cycle. $\overline{ADV}$ can be used as a chip select for external memory. ALE/$\overline{ADV}$ is activated only during external memory accesses. |
| $\overline{RD}$ | Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads. |
| $\overline{WR}$/$\overline{WRL}$ | Write and Write Low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is activated only during external memory writes. |
| $\overline{BHE}$/$\overline{WRH}$ | Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{BHE}$ low selects the bank of memory that is connected to the high byte of the data bus. A0 low selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 low, $\overline{BHE}$ high), to the high byte only (A0 high, $\overline{BHE}$ low), or both bytes (A0 low, $\overline{BHE}$ low). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes. |
| READY | Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. The bus cycle can be lengthened by up to 1 $\mu$s. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available through configuration of CCR. READY has a weak internal pullup, so it goes high unless externally pulled low. |
| HSI | Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit. The HSI pins are also used as inputs by EPROM parts in Programming Mode. |
| HSO | Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit. |
| Port 0 | 8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also a mode input to EPROM parts in the Programming Mode. |
| Port 1 | 8-bit quasi-bidirectional I/O port. |
| Port 2 | 8-bit multi-functional port. Six of its pins are shared with other functions, the remaining 2 are quasi-bidirectional. These pins are also used to input and output control signals on EPROM parts in Programming Mode. |
| Ports 3 and 4 | 8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Ports 3 and 4 are also used as a command, address and data path by EPROM parts operating in the Programming Mode. |

## Memory Map


0FFH
POWER-DOWN RAM
0F0H
0EFH
INTERNAL REGISTER FILE (RAM)
1AH
255
240
239
26
19H
18H
17H
16H
15H
14H
13H
12H
11H
10H
0FH
0EH
0DH
0CH
0BH
0AH
09H
08H
07H
06H
05H
04H
03H
02H
01H
00H
STACK POINTER
IOS1
IOS0
RESERVED
SP_STAT
IO PORT 2
IO PORT 1
IO PORT 0
TIMER2 (HI)
TIMER2 (LO)
TIMER1 (HI)
TIMER1 (LO)
INT_PENDING
INT_MASK
SBUF (RX)
HSI_STATUS
HSI_TIME (HI)
HSI_TIME (LO)
AD_RESULT (HI)
AD_RESULT (LO)
R0 (HI)
R0 (LO)
(WHEN READ)
STACK POINTER
PWM_CONTROL
IOC1
IOC0
RESERVED
SP_CON
IO PORT 2
IO PORT 1
BAUD_RATE
RESERVED
WATCHDOG
INT_PENDING
INT_MASK
SBUF (TX)
HSO_COMMAND
HSO_TIME (HI)
HSO_TIME (LO)
HSI_MODE
AD_COMMAND
R0 (HI)
R0 (LO)
(WHEN WRITTEN)
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
FFFFH
EXTERNAL MEMORY OR I/O
4000H
INTERNAL PROGRAM STORAGE ROM/EPROM OR EXTERNAL MEMORY
2080H
RESERVED
2030H - 207FH
SECURITY KEY
2020H - 202FH
RESERVED
201CH - 201FH
SELF JUMP OPCODE (27H FEH)
201AH - 201BH
RESERVED
2019H
CHIP CONFIGURATION BYTE
2018H
RESERVED
2012H - 2017H
INTERRUPT VECTORS
2000H
PORT 4
1FFFH
PORT 3
1FFEH
EXTERNAL MEMORY OR I/O
0100H
00FFH
INTERNAL RAM REGISTER FILE STACK POINTER SPECIAL FUNCTION REGISTERS (WHEN ACCESSED AS DATA MEMORY)
0000H
270361-17

## ELECTRICAL CHARACTERISTICS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS**

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Case Temperature Under Bias . . . −40°C to +125°C

Storage Temperature . . . . . −60°C to +150°C

Voltage from $V_{PP}$ to $V_{SS}$ or ANGND . . . . . −0.3V to +13.0V

Voltage from Any Other Pin to $V_{SS}$ or ANGND . . . . . −0.3V to +7.0V**

**NOTE:
This includes $V_{PP}$ on ROM and CPU devices.

## OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_C$ | Case Temperature Under Bias | −40 | +125 | °C |
| $V_{CC}$ | Digital Supply Voltage | 4.50 | 5.50 | V |
| $V_{REF}$ | Analog Supply Voltage | 4.50 | 5.50 | V |
| $F_{OSC}$ | Oscillator Frequency | 6.0 | 12.0 | MHz |
| $V_{PD}$ | Power Down Supply Voltage | 4.50 | 5.50 | V |

**NOTE:**
ANGND and $V_{SS}$ should be nominally at the same potential.

## DC CHARACTERISTICS

Test Conditions: $V_{CC}$, $V_{REF}$, $V_{PD}$, $V_{PP}$, $V_{SS}$ = 5.0V ±0.5V; $F_{OSC}$ = 6.0 MHz to 12.0 MHz; $T_C$ = −40°C to +125°C; $V_{SS}$, ANGND = 0V

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $I_{CC}$ | $V_{CC}$ Supply Current (−40°C ≤ +125°C Case) | | 240 | mA | All Outputs Disconnected |
| $I_{CC1}$ | $V_{CC}$ Supply Current ($T_C$ = +125°C) | | 155 | mA | |
| $I_{PD}$ | $V_{PD}$ Supply Current | | 1 | mA | Normal Operation and Power Down |
| $I_{REF}$ | $V_{REF}$ Supply Current | | 10 | mA | |
| $V_{IL}$ | Input Low Voltage (Except $\overline{RESET}$) | −0.3 | +0.8 | V | |
| $V_{IL1}$ | Input Low Voltage, $\overline{RESET}$ | −0.3 | +0.8 | V | |
| $V_{IH}$ | Input High Voltage (Except $\overline{RESET}$, NMI, XTAL1) | 2.0 | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, $\overline{RESET}$ Rising | 2.4 | $V_{CC}$ + 0.5 | V | |
| $V_{IH2}$ | Input High Voltage, $\overline{RESET}$ Falling Hysteresis | 2.1 | $V_{CC}$ + 0.5 | V | |
| $V_{IH3}$ | Input High Voltage, NMI, XTAL1 | 2.3 | $V_{CC}$ + 0.5 | V | |
| $I_{LI}$ | Input Leakage Current, All HSI, P3, P4 and P2.1. | | ±10 | µA | $V_{IN}$ = 0 to $V_{CC}$ |
| $I_{LI1}$ | DC Input Leakage Current, All P0 | | +3 | µA | $V_{IN}$ = 0 to $V_{CC}$ |
| $I_{IH}$ | Input High Current to $\overline{EA}$ | | 100 | µA | $V_{IH}$ = 2.4V |
| $I_{IL}$ | Input Low Current, All P1, P2.6 and P2.7. | | −150 | µA | $V_{IL}$ = 0.45V |
| $I_{IL1}$ | Input Low Current to $\overline{RESET}$ | −0.25 | −2 | mA | $V_{IL}$ = 0.45V |
| $I_{IL2}$ | Input Low Current P2.2, P2.3, P2.4, READY, BUSWIDTH | | −50 | µA | $V_{IL}$ = 0.45V |
| $V_{OL}$ | Output Low Voltage, All Quasi-Bidirectional I/O, P3, P4 | | 0.45 | V | $I_{OL}$ = 0.8 mA (Note 1) |

## DC CHARACTERISTICS Test Conditions: $V_{CC}$, $V_{REF}$, $V_{PD}$, $V_{PP}$, $V_{SS}$ = 5.0V ±0.5V; $F_{OSC}$ = 6.0 MHz to 12.0 MHz; $T_C$ = −40°C to +125°C; $V_{SS}$, ANGND = 0V (Continued)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{OL1}$(4) | Output Low Voltage, All Quasi-Bidirectional I/O, P3, P4 | | 0.75 | V | $I_{OL}$ = 2.0 mA (Notes 1, 2, 3) |
| $V_{OL2}$ | Output Low Voltage on Standard I/O Bus, Control Pins | | 0.45 | V | $I_{OL}$ = 2.0 mA (Notes 2, 3) |
| $V_{OH}$ | Output High Voltage on Quasi-Bidirectional I/O | 2.4 | | V | $I_{OH}$ = −20 μA (Note 1) |
| $V_{OH1}$ | Output High Voltage on Standard I/O Bus, Control Pins | 2.4 | | V | $I_{OH}$ = −200 μA (Note 1) |
| $I_{OH3}$ | Output High Current on $\overline{RESET}$ | −50 | | μA | $V_{OH}$ = 2.4V (Note 4) |
| $C_S$ | Pin Capacitance (Any Pin to $V_{SS}$) | | 10 | pF | $F_{TEST}$ = 1.0 MHz (Note 4) |

**NOTES:**
1. Quasi-bidirectional pins include those on P1, P2.6 and P2.7. Standard Output Pins include TXD, RXD (Mode 0 only), PWM, and HSO pins. Bus/Control pins include CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, INST and AD0–15.
2. Maximum current per pin must be externally limited to the following values if $V_{OL}$ is held above 0.45V.
   $I_{OL}$ on quasi-bidirectional pins: 4.0 mA
   $I_{OL}$ on standard output pins and $\overline{RESET}$: 8.0 mA
   $I_{OL}$ on Bus/Control pins: 2.0 mA
   $I_{OL}$ on HSO.0, HSO.4, HSO.5 = 1.6 mA: @ $V_{OL}$ = 0.5V
3. During normal (non-transient) operation the following limits apply:
   Total $I_{OL}$ on Port 1 must not exceed 4.0 mA.
   Total $I_{OL}$ on P2.0, P2.6, $\overline{RESET}$ and all HSO pins must not exceed 17.0 mA.
   Total $I_{OL}$ on P2.5, P2.7 must not exceed 4.0 mA.
4. These values are not tested in production, and are based on theoretical estimates and/or laboratory tests.

## AC CHARACTERISTICS

$V_{CC}$, $V_{PD}$ = 5.0V ±0.5V; $T_C$ = −40°C to +125°C; $F_{OSC}$ = 6.0 MHz to 12.0 MHz

Test Conditions: Load Capacitance on Output Pins = 80 pF
Oscillator Frequency = 12 MHz

**TIMING REQUIREMENTS** (Other system components must meet these specifications)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CLYX}$ | READY Hold after CLKOUT Edge | 0 | | ns |
| $T_{LLYV}$ | End of ALE/$\overline{ADV}$ to READY Valid | | 2 $T_{OSC}$ − 70 | ns |
| $T_{LLYH}$ | End of ALE/$\overline{ADV}$ to READY High | 2 $T_{OSC}$ + 40 | 4 $T_{OSC}$ − 80 | ns |
| $T_{YLYH}$ | Non-Ready Time | | 1000 | ns |
| $T_{AVDV}$(1) | Address Valid to Input Data Valid | | 5 $T_{OSC}$ − 120 | ns |
| $T_{RLDV}$ | $\overline{RD}$ Active to Input Data Valid | | 3 $T_{OSC}$ − 100 | ns |
| $T_{RHDX}$ | Data Hold after $\overline{RD}$ Inactive | 0 | | ns |
| $T_{RHDZ}$ | $\overline{RD}$ Inactive to Input Data Float | 0 | $T_{OSC}$ − 25 | ns |
| $T_{AVGV}$(1) | Address Valid to BUSWIDTH Valid | | 2 $T_{OSC}$ − 125 | ns |
| $T_{LLGX}$ | BUSWIDTH Hold after ALE/$\overline{ADV}$ Low | $T_{OSC}$ + 40 | | ns |
| $T_{LLGV}$ | ALE/$\overline{ADV}$ Low to BUSWIDTH Valid | | $T_{OSC}$ − 95 | ns |

**NOTE:**
1. The term "Address Valid" applies to AD0–AD15, $\overline{BHE}$ and INST.

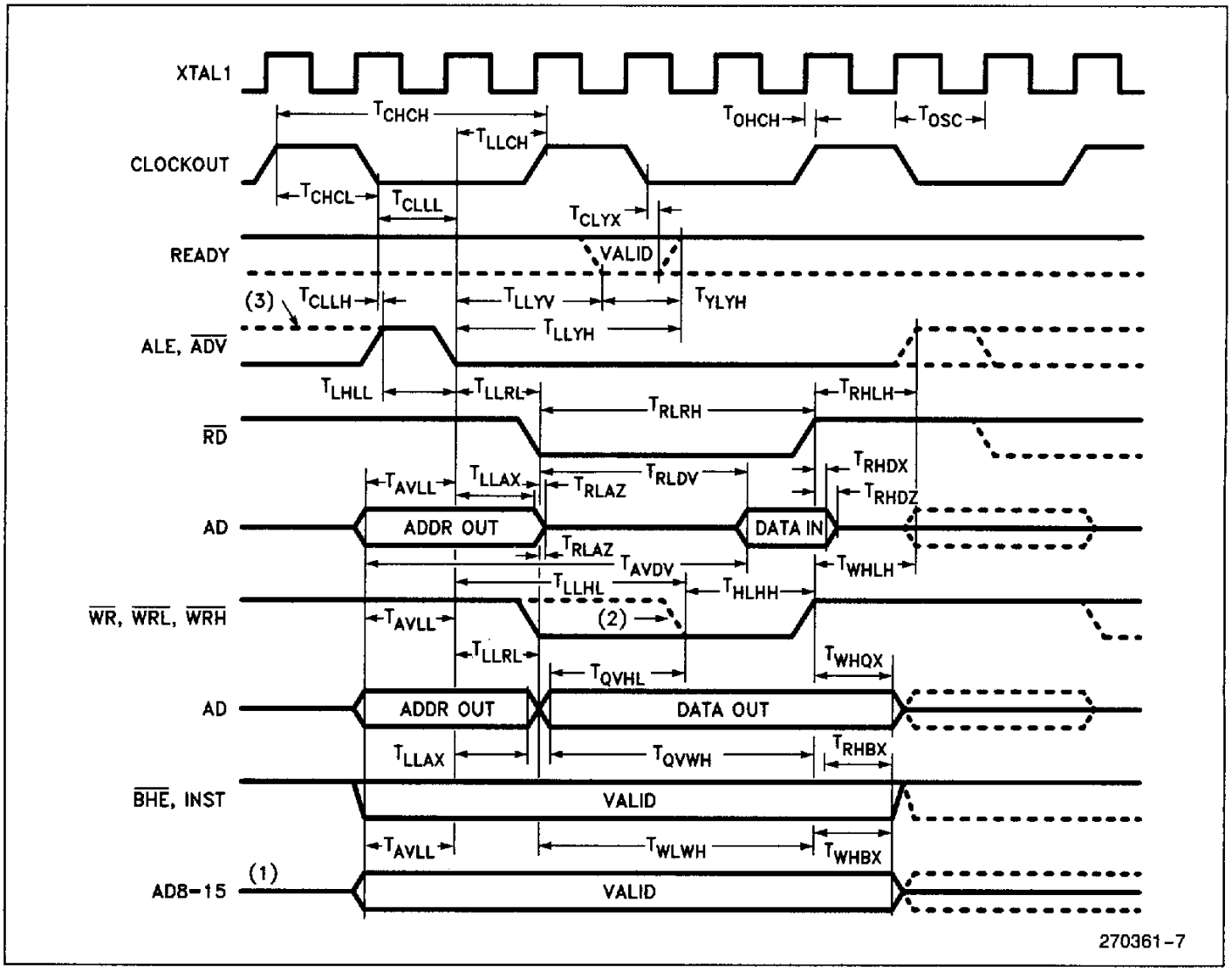
## AC CHARACTERISTICS (Continued)

**TIMING RESPONSES** (MCS 96 parts meet these specifications)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $F_{XTAL}$ | Oscillator Frequency | 6.0 | 12.0 | MHz |
| $T_{OSC}$ | Oscillator Period | 83 | 166 | ns |
| $T_{OHCH}$ | XTAL1 Rising Edge to Clockout Rising Edge | 0 | 120 | ns |
| $T_{CHCH}$ | CLKOUT Period(1) | 3 $T_{OSC}$(1) | 3 $T_{OSC}$(1) | ns |
| $T_{CHCL}$ | CLKOUT High Time | $T_{OSC}$ − 35 | $T_{OSC}$ + 10 | ns |
| $T_{CLLH}$ | CLKOUT Low to ALE High | −30 | 15 | ns |
| $T_{LLCH}$ | ALE/$\overline{ADV}$ Low to CLKOUT High | $T_{OSC}$ − 25 | $T_{OSC}$ + 45 | ns |
| $T_{LHLL}$ | ALE/$\overline{ADV}$ High Time | $T_{OSC}$ − 30 | $T_{OSC}$ + 35(2) | ns |
| $T_{AVLL}$(3) | Address Setup to End of ALE/$\overline{ADV}$ | $T_{OSC}$ − 50 | | ns |
| $T_{RLAZ}$(4) | $\overline{RD}$ or $\overline{WR}$ Low to Address Float | | 10(5) | ns |
| $T_{LLRL}$ | End of ALE/$\overline{ADV}$ to $\overline{RD}$ or $\overline{WR}$ Active | $T_{OSC}$ − 40 | | ns |
| $T_{LLAX}$ | Address Hold after End of ALE/$\overline{ADV}$ | $T_{OSC}$ − 40 | | ns |
| $T_{WLWH}$ | $\overline{WR}$ Pulse Width | 3 $T_{OSC}$ − 35 | | ns |
| $T_{QVWH}$ | Output Data Valid to End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ | 3 $T_{OSC}$ − 60 | | ns |
| $T_{WHQX}$ | Output Data Hold after $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ | $T_{OSC}$ − 50 | | ns |
| $T_{WHLH}$ | End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ to ALE/$\overline{ADV}$ High | $T_{OSC}$ − 75 | | ns |
| $T_{RLRH}$ | $\overline{RD}$ Pulse Width | 3 $T_{OSC}$ − 30 | | ns |
| $T_{RHLH}$ | End of $\overline{RD}$ to ALE/$\overline{ADV}$ High | $T_{OSC}$ − 45 | | ns |
| $T_{CLLL}$ | CLOCKOUT Low to ALE/$\overline{ADV}$ Low | $T_{OSC}$ − 40(5) | $T_{OSC}$ + 35(5) | ns |
| $T_{RHBX}$ | $\overline{RD}$ High to INST, $\overline{BHE}$, AD0–15 Inactive | $T_{OSC}$ − 25 | $T_{OSC}$ + 30 | ns |
| $T_{WHBX}$ | $\overline{WR}$ High to INST, $\overline{BHE}$, AD0–15 Inactive | $T_{OSC}$ − 50 | $T_{OSC}$ + 100 | ns |
| $T_{HLHH}$ | $\overline{WRL}$, $\overline{WRH}$ Low to $\overline{WRL}$, $\overline{WRH}$ High | 2 $T_{OSC}$ − 35 | 2 $T_{OSC}$ + 40 | ns |
| $T_{LLHL}$ | ALE/$\overline{ADV}$ Low to $\overline{WRL}$, $\overline{WRH}$ Low | 2 $T_{OSC}$ − 30 | 2 $T_{OSC}$ + 55 | ns |
| $T_{QVHL}$ | Output Data Valid to $\overline{WRL}$, $\overline{WRH}$ Low | $T_{OSC}$ − 60 | | ns |

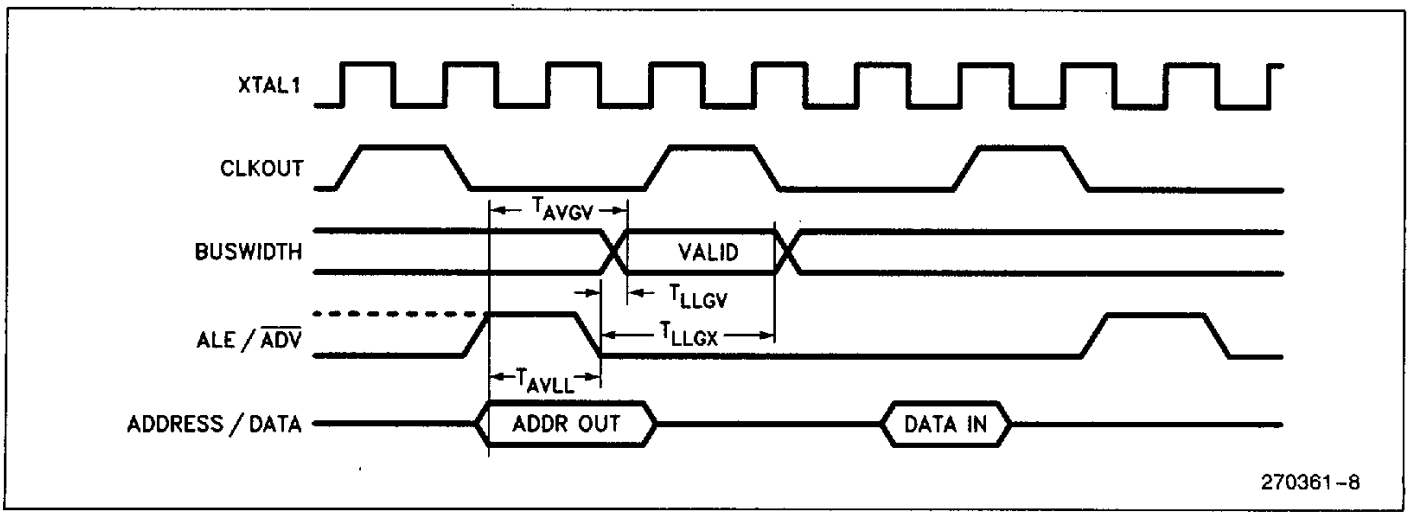
**NOTES:**
1. CLKOUT is directly generated as a divide by 3 of the oscillator. The period will be 3 $T_{OSC}$ ± 10 ns if $T_{OSC}$ is constant and the rise and fall times on XTAL1 are less than 10 ns.
2. Max spec applies only to ALE. Min spec applies to both ALE and $\overline{ADV}$.
3. The term " Address" in this definition applies to AD0–15, $\overline{BHE}$ and INST.
4. The term "Address" in this definition applies to AD0–7 for 8-bit cycles, and AD0–15 for 16-bit cycles.
5. Typical values.

## WAVEFORM




**NOTES:**
1. 8-bit bus only.
2. When write strobe mode selected.
3. When ADV selected.

## WAVEFORM—BUSWIDTH PIN



## AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

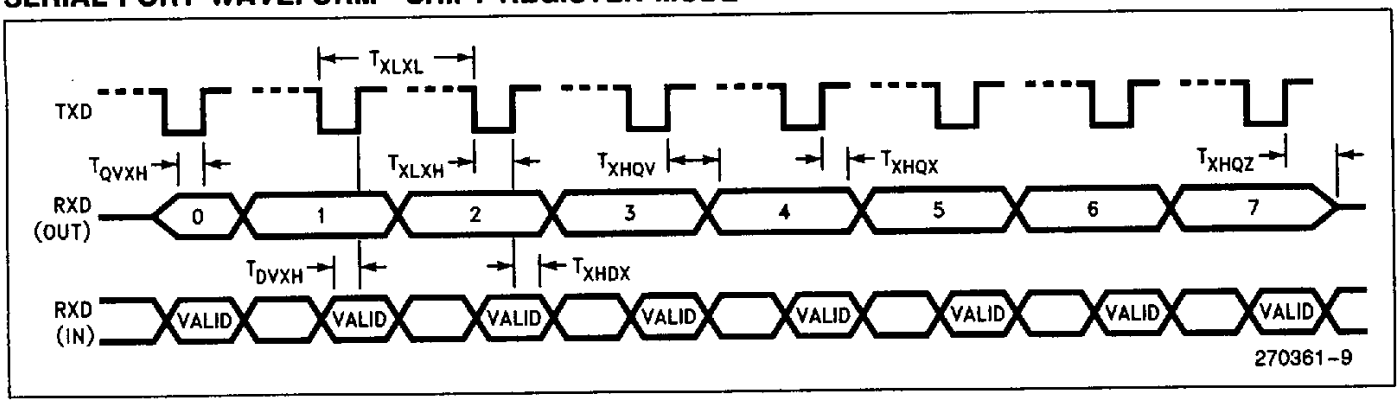
### SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: $T_C$ = −40°C to +125°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V; Load Capacitance = 80 pF

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{XLXL}$ | Serial Port Clock Period | 8 $T_{OSC}$ | | ns |
| $T_{XLXH}$ | Serial Port Clock Falling Edge to Rising Edge | 4 $T_{OSC}$ − 50 | 4 $T_{OSC}$ + 50 | ns |
| $T_{QVXH}$ | Output Data Setup to Clock Rising Edge | 3 $T_{OSC}$ | | ns |
| $T_{XHQX}$ | Output Data Hold After Clock Rising Edge | 2 $T_{OSC}$ − 70 | | ns |
| $T_{XHQV}$ | Next Output Data Valid After Clock Rising Edge | | 2 $T_{OSC}$ + 50 | ns |
| $T_{DVXH}$ | Input Data Setup to Clock Rising Edge | 2 $T_{OSC}$ + 200 | | ns |
| $T_{XHDX}$ | Input Data Hold After Clock Rising Edge | 0 | | ns |
| $T_{XHQZ}$ | Last Clock Rising to Output Float | | 5 $T_{OSC}$ | ns |

## WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

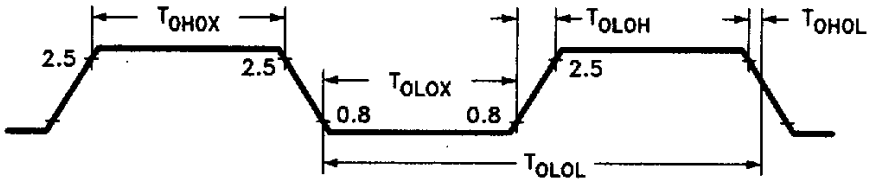
### SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



## EXTERNAL CLOCK DRIVE

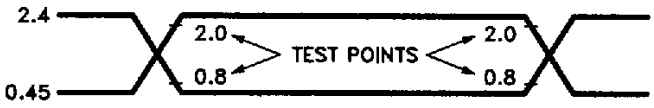
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $1/T_{OLOL}$ | Oscillator Frequency | 6 | 12 | MHz |
| $T_{OHOX}$ | High Time | 30 | | ns |
| $T_{OLOX}$ | Low Time | 30 | | ns |
| $T_{OLOH}$ | Rise Time | | 15 | ns |
| $T_{OHOL}$ | Fall Time | | 15 | ns |

### EXTERNAL CLOCK DRIVE WAVEFORMS




270361-10

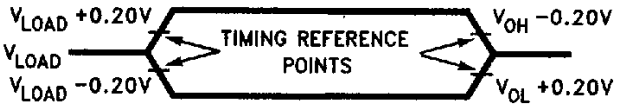
### AC TESTING INPUT, OUTPUT WAVEFORMS




270361-11

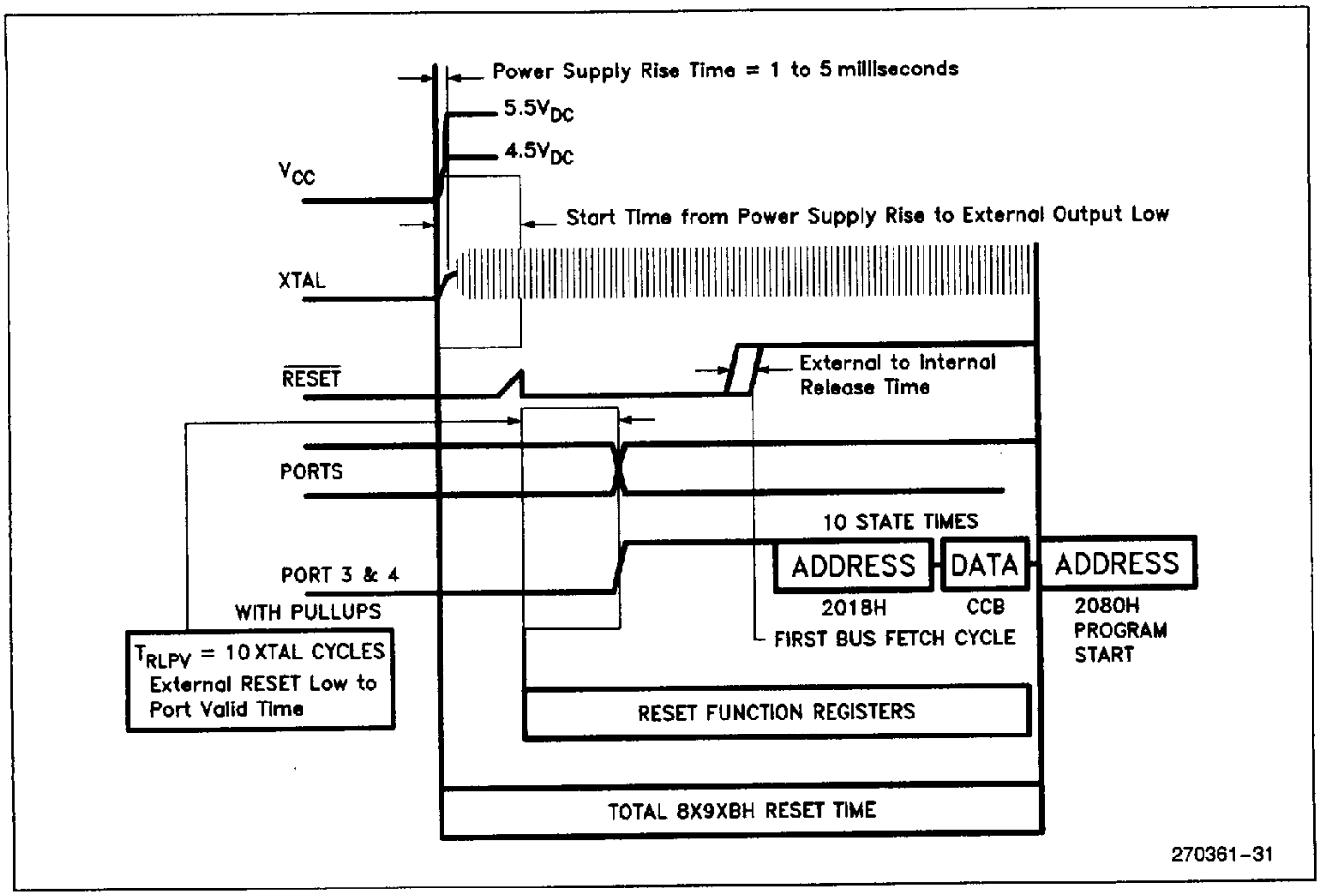
AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

### FLOAT WAVEFORMS

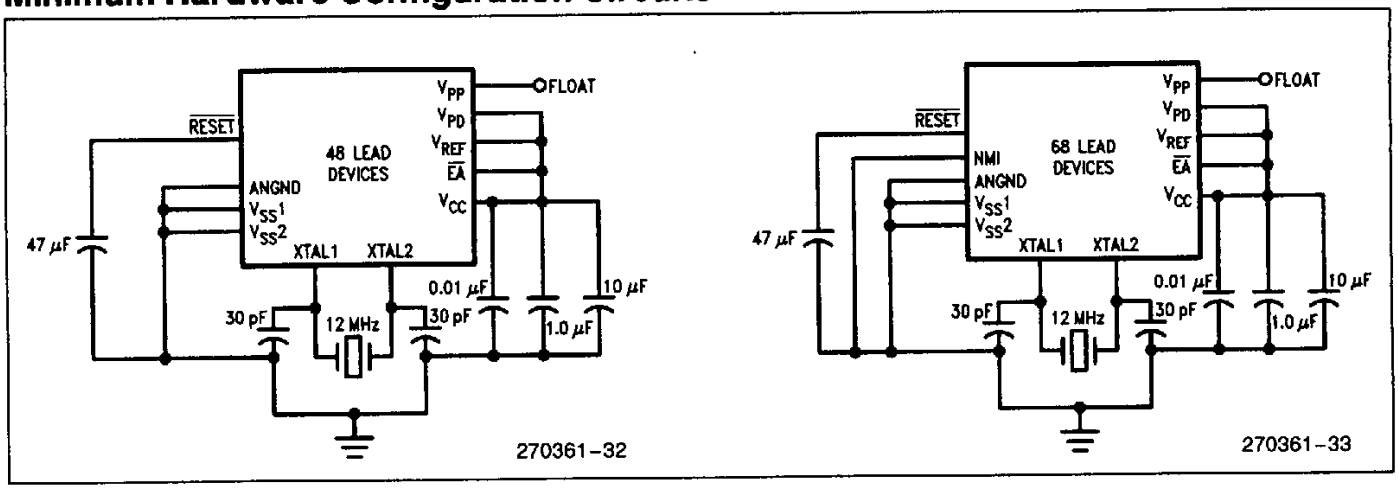



270361-12

For timing purposes a port pin is no longer floating when a 200 mV change from load voltage occurs, and begins to float when a 200 mV change from the loaded $V_{OH}/V_{OL}$ level occurs $I_{OL}/I_{OH} \geq \pm 8$ mA.




## Minimum Hardware Configuration Circuits



## A/D CONVERTER SPECIFICATIONS

The absolute conversion accuracy is dependent on the accuracy of $V_{REF}$. The specifications given below assume adherence to the Operating Conditions section of this datasheet. Testing is done at $V_{REF}$ = 5.120V.

### OPERATING CONDITIONS

$V_{CC}$, $V_{PD}$, $V_{REF}$ ..... 5.0V ±0.25V
$V_{SS}$, ANGND ..... 0.0V
$T_C$ ..... −40°C to +125°C
$F_{OSC}$ ..... 6.0 to 12.0 MHz
Test Conditions:
$V_{REF}$ ..... 5.120V
$V_{CC}$ ..... 5.0V

| Parameter | Typical*(1) | Minimum | Maximum | Units** | Notes |
|---|---|---|---|---|---|
| Resolution | | 1024<br>10 | 1024<br>10 | Levels<br>Bits | |
| Absolute Error | | 0 | ±4 | LSBs | |
| Full Scale Error | −0.5 ±0.5 | | | LSBs | |
| Zero Offset Error | ±0.5 | | | LSBs | |
| Non-Linearity | | | ±4 | LSBs | |
| Differential Non-Linearity | | 0 | ±2 | LSBs | |
| Channel-to-Channel Matching | | 0 | ±1 | LSBs | |
| Repeatability | ±0.25 | 0 | | LSBs | 1 |
| Temperature Coefficients:<br>Offset<br>Full Scale<br>Differential Non-Linearity | <br>0.009<br>0.009<br>0.009 | | | <br>LSB/°C<br>LSB/°C<br>LSB/°C | <br>1<br>1<br>1 |
| Off Isolation | | −60 | | dB | 1, 2, 4 |
| Feedthrough | −60 | | | dB | 1, 2 |
| $V_{CC}$ Power Supply Rejection | −60 | | | dB | 1, 2 |
| Input Resistance | | 1K | 5K | Ω | 1 |
| DC Input Leakage | | 0 | 3.0 | µA | |
| Sample Delay | | 3 $T_{OSC}$ − 50 | 3 $T_{OSC}$ + 50 | ns | 1, 3 |
| Sample Time | | 12 $T_{OSC}$ − 50 | 12 $T_{OSC}$ + 50 | ns | 1 |
| Sample Capacitance | | | 2 | pF | |

**NOTES:**
* These values are expected for most parts at 25°C.
** An "LSB", as used here, is defined in the glossary which follows and has a value of approximately 5 mV.
1. These values are not tested in production and are based on theoretical estimates and laboratory tests.
2. DC to 100 KHz.
3. For starting the A/D with an HSO Command.
4. Multiplexer Break-Before-Make Guaranteed.

# EPROM SPECIFICATIONS

## AC EPROM PROGRAMMING CHARACTERISTICS

Operating Conditions: Load Capacitance = 150 pF, $T_C$ = 25°C, ±5°C, $V_{CC}$, $V_{PD}$, $V_{REF}$ = 5.0V ±0.5V, $V_{SS}$, ANGND = 0V, $V_{PP}$ = 12.75V ±0.25V, $\overline{EA}$ = 11V ±2.0V, $F_{OSC}$ = 6.0 MHz

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{AVLL}$ | ADDRESS/COMMAND Valid to PALE Low | 0 | | $T_{OSC}$ |
| $T_{LLAX}$ | ADDRESS/COMMAND Hold After PALE Low | 80 | | $T_{OSC}$ |
| $T_{DVPL}$ | Output Data Setup Before $\overline{PROG}$ Low | 0 | | $T_{OSC}$ |
| $T_{PLDX}$ | Data Hold After $\overline{PROG}$ Falling | 80 | | $T_{OSC}$ |
| $T_{LLLH}$ | PALE Pulse Width | 180 | | $T_{OSC}$ |
| $T_{PLPH}$ | $\overline{PROG}$ Pulse Width | 250 $T_{OSC}$ | 100 µs + 144 $T_{OSC}$ | |
| $T_{LHPL}$ | PALE High to $\overline{PROG}$ Low | 250 | | $T_{OSC}$ |
| $T_{PHLL}$ | $\overline{PROG}$ High to Next PALE Low | 600 | | $T_{OSC}$ |
| $T_{PHDX}$ | Data Hold After $\overline{PROG}$ High | 30 | | $T_{OSC}$ |
| $T_{PHVV}$ | $\overline{PROG}$ High to PVER/$\overline{PDO}$ Valid | 500 | | $T_{OSC}$ |
| $T_{LLVH}$ | PALE Low to PVER/$\overline{PDO}$ High | 100 | | $T_{OSC}$ |
| $T_{PLDV}$ | $\overline{PROG}$ Low to VERIFICATION/DUMP Data Valid | 100 | | $T_{OSC}$ |
| $T_{SHLL}$ | RESET High to First PALE Low (not shown) | 2000 | | $T_{OSC}$ |

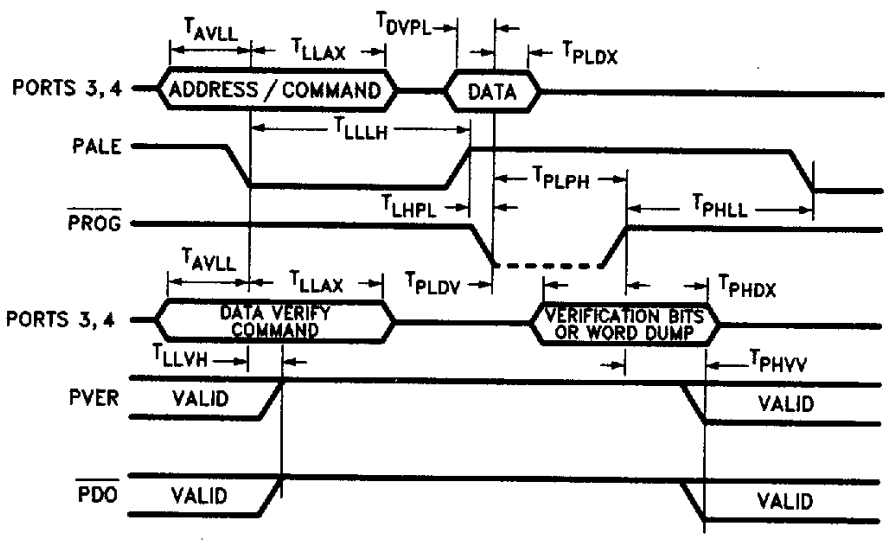
**NOTE:**
Run-time programming is done with $F_{OSC}$ = 6.0 MHz to 12.0 MHz, $V_{CC}$, $V_{PD}$, $V_{REF}$ = 5V ±0.5V, $T_C$ = 25°C ±5°C and $V_{PP}$ = 12.75V ± 0.25V. For run-time programming over a full operating range, contact the factory.

## DC EPROM PROGRAMMING CHARACTERISTICS

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $I_{PP}$ | $V_{PP}$ Supply Current (Whenever Programming) | | 100 | mA |

**NOTE:**
$V_{PP}$ must be within 1V of $V_{CC}$ while $V_{CC}$ < 4.5V. $V_{PP}$ must not have a low impedance path to ground or $V_{SS}$ while $V_{CC}$ > 4.5V.

## WAVEFORM—EPROM PROGRAMMING




**Reserved location warning:** Intel Reserved addresses can not be used by applications which use 8X9XBH internal ROM/EPROM. The data read from a reserved location is not guaranteed, and a write to any reserved location could cause unpredictable results. When attempting to program Intel Reserved addresses, the data must be 0FFFFH to ensure a harmless result. A memory map indicating reserved locations on the 8X9XBH is shown in Figure 2.

Intel Reserved locations, when mapped to external memory, must be filled with 0FFFFH to ensure compatibility with future devices.

## POWER SUPPLY SEQUENCE WHILE PROGRAMMING

For any 879XBH that is in any programming mode, high voltages must be applied to the device. To avoid damaging the devices, the following rules must not be violated.

RULE #1— $V_{PP}$ must not have a low impedance path to ground when $V_{CC}$ is above 4.5V.

RULE #2— $V_{CC}$ must be above 4.5V before $V_{PP}$ can be higher than 5.0V.

RULE #3— $V_{PP}$ must be within 1V of $V_{CC}$ while $V_{CC}$ is below 4.5V.

RULE #4— All voltages must be within tolerance and the oscillator stable before $\overline{RESET}$ rises.

RULE #5— $\overline{EA}$ must be brought high to place the devices in programming mode before $V_{PP}$ is brought high.

To adhere to these rules, the following power up and power down sequences can be followed.

POWER UP

$\overline{RESET}$ = 0;
CLOCK ON; if using an external clock
; instead of an oscillator
$V_{CC}$ = $V_{PP}$ = $V_{EA}$ = 5V;
PALE = $\overline{PROG}$ = PORT 34 = $V_{IH}$;*
SID AND PMODE VALID;
$\overline{EA}$ = 12.75V;
$V_{PP}$ = 12.75V;
WAIT; wait for supplies and clock to
; settle
$\overline{RESET}$ = 5V;
WAIT Tshll; See datasheet
BEGIN;

POWER DOWN

$\overline{RESET}$ = 0;
$V_{PP}$ = 5V;
$\overline{EA}$ = 5V;
PALE = $\overline{PROG}$ = SID = PMODE = PORT34 = 0V;
$V_{CC}$ = $V_{PP}$ = $V_{EA}$ = 0V;
CLOCK OFF;

**NOTE:**
*$V_{IH}$ = Logical "1", 2.4V Minimum

One final note on power up, power down. The maximum limit on $V_{PP}$ must never be violated, even for an instant. Therefore, an RC rise to the desired $V_{PP}$ is recommended. $V_{PP}$ is also sensitive to instantaneous voltage steps. This also can be avoided by using an RC ramp on $V_{PP}$.

## ADDITIONAL INFORMATION

**MCS-96 Thermal Characteristics**

| Package | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 68-Lead Plastic Leaded Chip Carrier | 36 | 13.4 |
| 68-Lead Plastic Flatpack | 36 | 13.4 |

**NOTES:**
$\theta_{JA}$ = Thermal resistance between junction and the surrounding environment (ambient). Measurements are taken 1 ft. away from case in air flow environment.
$\theta_{JC}$ = Thermal resistance between junction and package surface (case).

All values of $\theta_{JA}$ and $\theta_{JC}$ may fluctuate depending on the environment (with or without airflow, and how much air flow) and device power dissipation at temperature of operation. Typical variations are ±2°C/W.

The graph below shows a typical $\theta_{JA}$ vs. Air Flow rate for a PLCC package (with and without a heat speader).

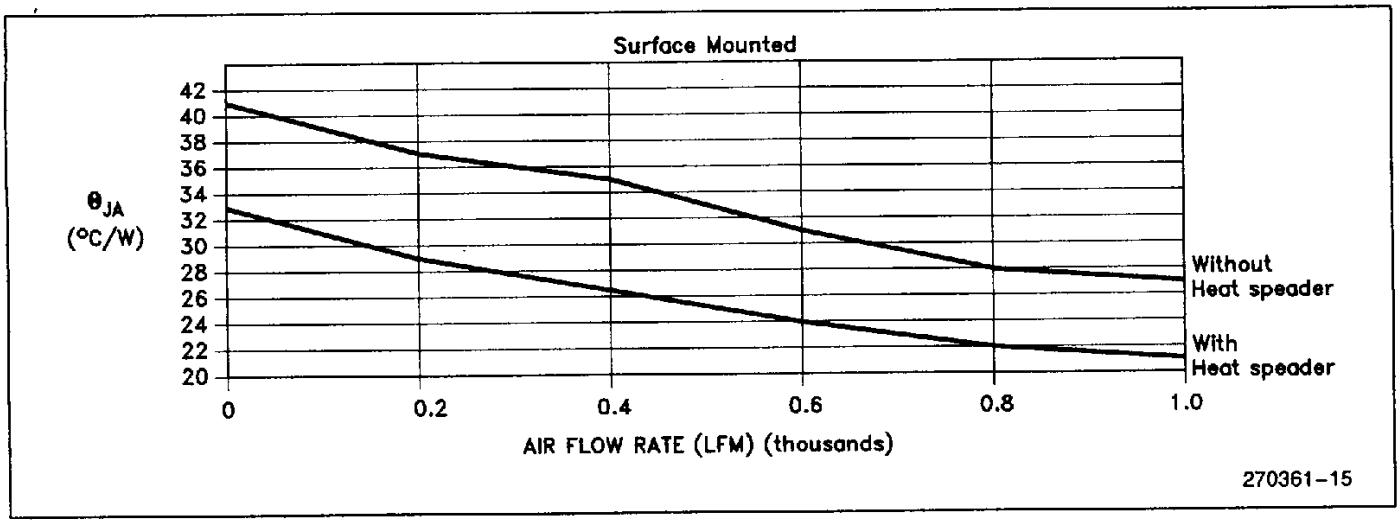



**Figure 7. $\theta_{JA}$ vs Linear Air Flow**

Figure 8 is an $I_{CC}$ vs. temperature plot for the 8X9XBH products. Test conditions are stated and actuals may vary depending on speed, package, $V_{CC}$ and temperature, but will not exceed maximum limit specified at any case temperature between specified temperature limits.

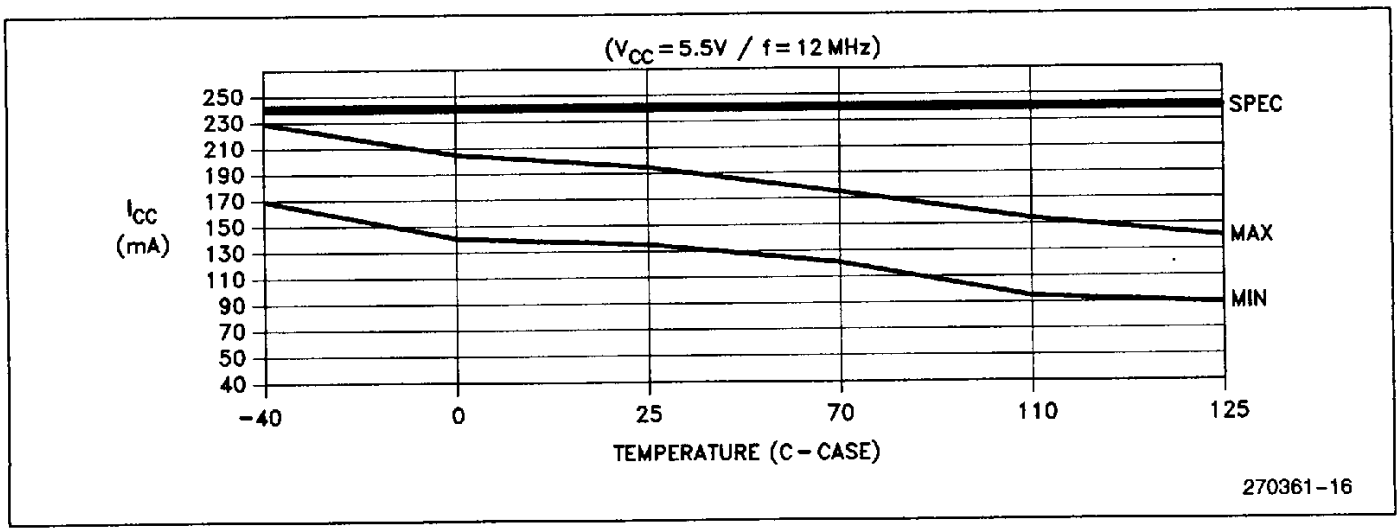



**Figure 8. 8X9XBH $I_{CC}$ vs TEMP**

## FUNCTIONAL DEVIATIONS

The following is a list of all known functional deviations for 8X9XBH devices.

## CPU Section

**1. Indexed, 3 Operand Multiply (Note C, D, E)**

In a three word multiply (MUL, MULB, MULU, MULUB) using indexed addressing mode, the displacement portion may not be in the range of 200H through 17FFH, inclusive. If the displacements in this range are necessary, the use of a two operand indexed multiply can be used with a move.

**2. JBS and JBC Directly with Port Pins (Note C)**

The JBS and JBC instructions when used directly with Port 2.1 or all pins of Port 0 cannot be used. If testing of these port pins is necessary, shadow the entire port data in a RAM register and test the bit in that RAM register.

**3. BUSWIDTH and 8-Bit Bus (Note C)**

If the BUSWIDTH pin is pulled high externally, or left to float, the internal pullup will pull this pin high. A high condition on this input equates to a 16-bit bus mode externally. During the CHIP CONFIGURATION BYTE fetch cycle, the port circuitry changes the CCB address about 25 ns after $\overline{RD}$ goes low. If the CCB being read is trying to configure an 8-bit bus, the upper address lines (AD8–AD15) will NOT be latched during the CCB read. Therefore, if the read from the CCR (2018H) is in a x8 address space, the BUSWIDTH pin MUST be held low for this fetch, or the address lines AD8–AD15 must be latched (via a latched external EPROM or TTL latch).

**4. FIFO/HSI Status Cleared (Note C, D)**

It is possible to have a time value in the FIFO with no status bits set in the HSI_STATUS register. When events are logged, the first event is loaded into the Holding Register, the next is loaded into slot #1 of the FIFO, the next in slot #2, etc. If the Holding Register is read after the #2 slot is loaded, the #1 slot will be moved into the Holding Register to be read next. If another event is logged, it will be placed in slot #3, not #1 (the one just vacated). There are 7 slots in the FIFO. If the FIFO is allowed to "roll over", that is a 9th event stored in the #1 slot again, before a cleared FIFO happens, the 9th event will have a valid time with a cleared status bits in the HSI_STATUS register (Bits 0, 2, 4 and 6 = 0). If the HSI_STATUS register status bits are cleared, there is no way of matching this time with an HSI input pin. It is important to note that in order to avoid this problem both interrupt routines and polling procedures which allow seven entries in the FIFO MUST clear all events from the FIFO before the next event is logged. If this is not possible, events will have cleared status bits and these routines should also handle that case.

To ensure proper operation of the High Speed Input FIFO, it is imperative that no more than seven FIFO entries be placed into an empty FIFO. This includes conditions that enter and clear multiple events but leave one or more entries in the FIFO (i.e., add three entries, read one out, add four more, read one out, is seven entries). All seven must be emptied before allowing further events to occur at the pins. The FIFO is empty even if there is an entry in the Holding Register. (An "event" is defined as a pin transition. An "entry" is defined as one or more pin events loaded into a single FIFO array location.)

Allowing more than seven FIFO entries to occur between cleared conditions will result in incorrect status information for either the eighth or ninth entry. This effectively limits the total number of entries to seven.

There is one exception that will allow the FIFO to correctly record eight entries. If the first two entries of a cleared FIFO and Holding Register are separated by greater than 16 state times, the ninth entry (rather than the eighth entry) will be recorded with incorrect status information. This is true even if the events following the first two entries were only separated by eight states.

**5. RESET (Note C)**

If the XTAL inputs are driven BEFORE $V_{CC}$ is stable (between 4.5 $V_{DC}$ – 5.5 $V_{DC}$), the state machine locks the device into a condition which floats the node in control of the pulldown gate on the RESET pin. The pulldown node will remain on until the floating node loses the stored charge and releases the pulldown. All subsequent RESET's after the Power-on-Reset will operate correctly. Make sure that $V_{CC}$ is stable before XTAL is driven.

Since RESET is asynchronous, it is possible to apply RESET during writes to quasi-bidirectional port pins. If this occurs, the QBD port pins may not RESET immediately to a logical one. Instead of the low impedance pullup being turned on, only the high impedance device is on, causing the signals on the QBD pins to rise more slowly than usual.

**6. Using T2CLK as source for Timer2 (Note C, D)**

TIMER2 has two selectable clock sources, the T2CLK or HSI.1 pins, selectable by bit IOC0.3. When using T2CLK as the clock for TIMER2, writing to IOC0 may cause TIMER2 to increment. The user should only write to IOC0 once during initialization, and then immediately clear TIMER2 using the HSO command OEH. Effectively, the customer cannot reset TIMER2 with bit IOC0.1, and can only use the external reset sources or the HSO command when using T2CLK as the clock source. If the HSI.1 pin is the source for TIMER2, only the first write to IOC0 may cause TIMER2 to increment, further writes will not increment TIMER2.

**7. HSI Resolution (Note E)**

The HSI resolution has changed from 8 state times on the BH D-step to 9 state times on the BH E-step. This decreases the maximum HSI input speed from once every 8 state times to once every 9 state times.

**8. Serial Port Flags (Note E)**

Reading SP_STAT may not clear the TI or RI flag if that flag was set within two state times prior to the read. In addition, the parity error bit (RPE/RB8) may not be correct if it is read within two state times after RI is set.

**9. Checksum on Reserved Locations (Note E)**

This is a design consideration, not an errata. A test register was added to location 201Ch on the 8X9XBH E-step that controls the readability and writability of certain SFR's during testing. The addition of these bits affects the readability and writability of this reserved location when it is read. If this location is included in a checksum (which it should not), a checksum difference could occur between the E-step and previous steppings. The User Guide states that reserved locations should not be read or written, this statement includes checksum reads also.

**Note:** C = present on C-step devices
D = present on D-step devices
E = present on E-step devices

E-step and later devices can be identified by a special mark following the eight digit FPO number on the top of the package. For E-step devices, this mark is an "E".

## DATASHEET REVISION HISTORY

The following are the key differences between this datasheet and the -005 version:

1. The "preliminary" status was dropped and replaced with production status (no label).
2. Trademarks were updated.