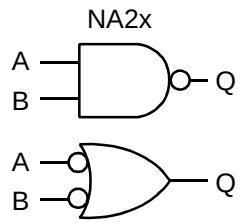
Description

NA2x is a family of 2-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... NA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NA21	NA22	NA23	NA24	NA26
A	1.0	2.1	4.3	2.1	2.1
B	1.0	2.1	4.3	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA21	1.0	TBD	0.8
NA22	2.0	TBD	1.7
NA23	4.0	TBD	3.4
NA24	5.0	TBD	10.5
NA26	6.0	TBD	14.8

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.09 0.17	0.13 0.22	0.24 0.36	0.33 0.50	0.38 0.59
NA22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.08 0.12	0.13 0.20	0.20 0.30	0.26 0.42	0.31 0.51
NA23	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.07 0.12	0.13 0.23	0.19 0.30	0.23 0.38	0.28 0.46
NA24	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.30 0.37	0.39 0.48	0.46 0.60	0.55 0.71	0.65 0.80
NA26	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.42	0.43 0.54	0.53 0.65	0.62 0.74	0.72 0.86

Delay will vary with input conditions. See page 2-17 for interconnect estimates.