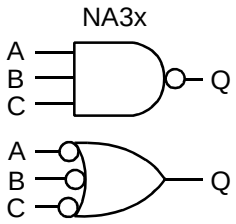
Description

NA3x is a family of 3-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

HDL Syntax

Verilog ..... NA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NA31	NA32	NA33	NA34	NA36
A	1.0	2.1	2.1	2.1	2.1
B	1.0	2.1	2.1	2.1	2.1
C	1.0	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA31	2.0	TBD	1.6
NA32	3.0	TBD	2.7
NA33	6.0	TBD	8.3
NA34	6.0	TBD	13.3
NA36	8.0	TBD	16.0

a. See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.11 0.22	0.14 0.29	0.22 0.42	0.28 0.54	0.34 0.68
NA32	**Number of Equivalent Loads**		**1**	**3**	**6**	**9**	**12 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.08 0.16	0.12 0.23	0.17 0.33	0.22 0.43	0.26 0.52
NA33	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.29 0.43	0.41 0.54	0.51 0.65	0.60 0.76	0.70 0.89
NA34	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.49	0.40 0.59	0.50 0.69	0.59 0.79	0.68 0.89
NA36	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.55	0.44 0.68	0.54 0.78	0.62 0.87	0.72 0.96

Delay will vary with input conditions. See page 2-17 for interconnect estimates.