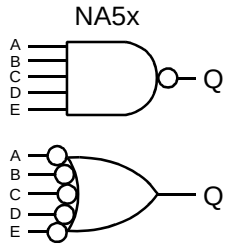
Description

NA5x is a family of 5-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

HDL Syntax

Verilog ..... NA5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NA5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NA51	NA52	NA53	NA54	NA56
A	1.0	1.0	2.1	2.1	2.1
B	1.0	1.0	2.1	2.1	2.1
C	1.0	1.0	2.1	2.1	2.1
D	1.0	1.0	2.1	2.1	2.1
E	1.0	1.0	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA51	3.0	TBD	2.7
NA52	4.0	TBD	7.5
NA53	8.0	TBD	12.4
NA54	10.0	TBD	16.5
NA56	12.0	TBD	21.2

a. See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.14 0.30	0.17 0.40	0.21 0.49	0.24 0.58	0.29 0.77
NA52	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.46	0.41 0.58	0.53 0.71	0.68 0.88	0.79 1.01
NA53	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.49	0.43 0.66	0.53 0.78	0.62 0.89	0.73 1.01
NA54	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.39	0.41 0.58	0.51 0.73	0.61 0.85	0.70 0.95
NA56	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.60	0.46 0.75	0.57 0.86	0.66 0.96	0.74 1.08

Delay will vary with input conditions. See page 2-17 for interconnect estimates.