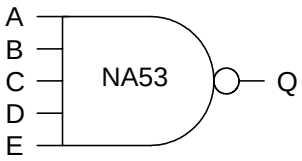
NA53 is a 5-input NAND gate with 3x drive strength.

Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L



Capacitance

	Ci (pF)
A	0.050
B	0.050
C	0.053
D	0.056
E	0.056

Area

1.22 $mils^2$

Power

14.31 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 5V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.3	L = 2.1	L = 3.0	L = 0.3	L = 2.1	L = 3.0
Delay A to Q	tpdar	0.57	1.56	2.09	0.91	1.88	2.37
	tpdaf	0.51	1.38	1.82	0.49	1.35	1.80
Delay B to Q	tpdbr	0.65	1.64	2.16	1.02	2.01	2.53
	tpdbf	0.56	1.44	1.86	0.52	1.38	1.82
Delay C to Q	tpdcr	0.72	1.71	2.24	1.10	2.11	2.58
	tpdcf	0.59	1.45	1.90	0.51	1.38	1.82
Delay D to Q	tpddr	0.78	1.78	2.30	1.19	2.19	2.67
	tpddf	0.61	1.48	1.95	0.49	1.35	1.79
Delay E to Q	tpder	0.84	1.83	2.35	1.26	2.25	2.74
	tpdef	0.61	1.50	1.92	0.44	1.30	1.73
Output Slope A to Q	op_slar	0.67	3.93	5.46	0.65	3.90	5.57
	op_slaf	0.55	2.87	4.03	0.53	2.87	3.92
Output Slope B to Q	op_slbr	0.67	3.93	5.48	0.67	3.91	5.55
	op_slbf	0.52	2.90	4.05	0.53	2.91	4.07
Output Slope C to Q	op_slcr	0.67	3.95	5.46	0.68	3.92	5.58
	op_slcf	0.52	2.85	4.01	0.53	2.90	4.08
Output Slope D to Q	op_sldr	0.67	3.90	5.57	0.68	3.93	5.52
	op_sldf	0.53	2.86	4.12	0.53	2.88	4.07
Output Slope E to Q	op_sler	0.68	3.88	5.53	0.67	3.93	5.57
	op_slef	0.52	2.91	4.05	0.53	2.87	4.07