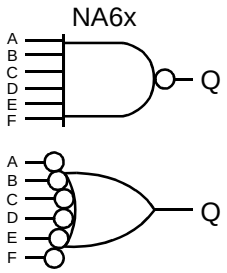
Description

NA6x is a family of 6-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: NA6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads				
	NA61	NA62	NA63	NA64	NA66
A	1.0	2.1	2.1	2.1	2.1
B	1.0	2.1	2.1	2.1	2.1
C	1.0	2.1	2.1	2.1	2.1
D	1.0	2.1	2.1	2.1	2.1
E	1.0	2.1	2.1	2.1	2.1
F	1.0	2.1	2.1	2.1	2.1

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA61	5.0	TBD	8.7
NA62	9.0	TBD	14.7
NA63	12.0	TBD	18.6
NA64	12.0	TBD	19.0
NA66	11.0	TBD	20.0

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA61	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.56	0.42 0.68	0.54 0.82	0.69 0.97	0.81 1.08
NA62	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.28 0.48	0.38 0.62	0.49 0.74	0.59 0.86	0.71 0.98
NA63	**Number of Equivalent Loads**		**1**	**11**	**22**	**32**	**43 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.30 0.54	0.43 0.69	0.54 0.82	0.64 0.91	0.74 1.01
NA64	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.27 0.58	0.39 0.73	0.49 0.85	0.59 0.95	0.68 1.04
NA66	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.61	0.44 0.77	0.54 0.89	0.62 1.00	0.71 1.11

Delay will vary with input conditions. See page 2-17 for interconnect estimates.