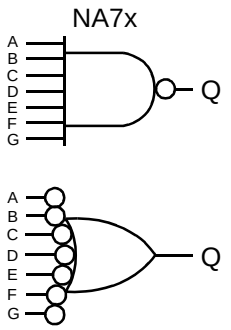
Description

NA7x is a family of 7-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	X	X	X	X	X	X	H
X	L	X	X	X	X	X	H
X	X	L	X	X	X	X	H
X	X	X	L	X	X	X	H
X	X	X	X	L	X	X	H
X	X	X	X	X	L	X	H
X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA7x *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: NA7x port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads				
	NA71	NA72	NA73	NA74	NA76
A	2.1	2.1	2.1	2.1	2.1
B	2.1	2.1	2.1	2.1	2.1
C	2.1	2.1	2.1	2.1	2.1
D	2.1	2.1	2.1	2.1	2.1
E	2.1	2.1	2.1	2.1	2.1
F	2.1	2.1	2.1	2.2	2.1
G	2.1	2.1	2.1	2.1	2.1

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA71	12.0	TBD	15.3
NA72	11.0	TBD	19.8
NA73	12.0	TBD	20.5
NA74	12.0	TBD	22.8
NA76	14.0	TBD	26.1

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA71	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.34 0.68	0.43 0.82	0.55 0.97	0.68 1.13	0.79 1.26
NA72	Number of Equivalent Loads		1	8	15	22	30 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.67	0.44 0.81	0.54 0.94	0.64 1.07	0.75 1.22
NA73	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.67	0.44 0.84	0.55 0.98	0.64 1.09	0.74 1.21
NA74	Number of Equivalent Loads		1	14	28	42	56 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.76	0.44 0.96	0.55 1.10	0.64 1.21	0.71 1.30
NA76	Number of Equivalent Loads		1	21	42	62	83 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.86	0.50 1.03	0.61 1.17	0.70 1.29	0.79 1.41

Delay will vary with input conditions. See page 2-17 for interconnect estimates.