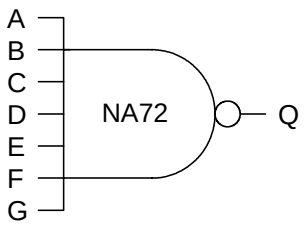
NA72 is a 7-input NAND gate with 2x drive strength.

Truth Table

A	B	C	D	E	F	G	Q
L	X	X	X	X	X	X	H
X	L	X	X	X	X	X	H
X	X	L	X	X	X	X	H
X	X	X	L	X	X	X	H
X	X	X	X	L	X	X	H
X	X	X	X	X	L	X	H
X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	L



Capacitance

	Ci (pF)
A	0.034
B	0.023
C	0.031
D	0.036
E	0.025
F	0.027
G	0.031

Area

1.22 $mils^2$

Power

4.23 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.2	L = 1.4	L = 2.0	L = 0.2	L = 1.4	L = 2.0
Delay A to Q	tpdar	1.03	2.39	3.11	1.38	2.75	3.40
	tpdaf	0.89	2.02	2.58	0.99	2.13	2.66
Delay B to Q	tpdbr	1.09	2.44	3.17	1.45	2.82	3.53
	tpdbf	0.92	2.05	2.60	0.96	2.11	2.63
Delay C to Q	tpdcr	1.14	2.49	3.22	1.52	2.91	3.59
	tpdcf	0.93	2.07	2.59	0.89	2.03	2.57
Delay D to Q	tpddr	0.97	2.33	3.00	1.32	2.68	3.42
	tpddf	0.88	2.01	2.59	0.95	2.06	2.61
Delay E to Q	tpder	1.05	2.40	3.14	1.42	2.77	3.51
	tpdef	0.93	2.04	2.63	0.95	2.10	2.65
Delay F to Q	tpdfr	1.13	2.47	3.22	1.50	2.84	3.58
	tpdff	0.95	2.09	2.64	0.93	2.06	2.60
Delay G to Q	tpdgr	1.22	2.59	3.30	1.57	2.96	3.60
	tpdgf	0.96	2.08	2.67	0.89	2.02	2.57
Output Slope A to Q	op_slar	0.96	5.30	7.31	0.91	5.13	7.51
	op_slaf	0.73	3.72	5.08	0.73	3.62	4.97

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.2	L = 1.4	L = 2.0	L = 0.2	L = 1.4	L = 2.0
Output Slope B to Q	op_slbr	0.97	5.30	7.31	0.96	5.31	7.28
	op_slbf	0.73	3.71	5.01	0.72	3.67	5.02
Output Slope C to Q	op_slcr	0.95	5.31	7.35	0.92	5.16	7.30
	op_slcf	0.73	3.65	4.97	0.75	3.62	5.00
Output Slope D to Q	op_sldr	0.92	5.10	7.52	0.93	5.27	7.41
	op_sldf	0.72	3.53	5.12	0.72	3.56	5.00
Output Slope E to Q	op_sler	0.96	5.30	7.33	0.95	5.27	7.36
	op_slef	0.75	3.52	5.12	0.73	3.63	5.08
Output Slope F to Q	op_slfr	0.95	5.27	7.37	0.95	5.23	7.38
	op_slff	0.73	3.63	5.36	0.72	3.75	4.98
Output Slope G to Q	op_slgr	0.96	5.30	7.27	0.93	5.15	7.50
	op_slgf	0.73	3.55	5.13	0.72	3.81	4.96