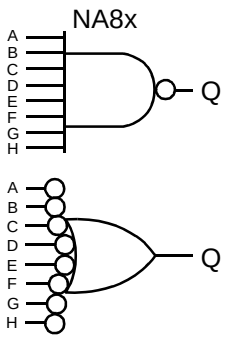
Description

NA8x is a family of 8-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA8x *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: NA8x port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads				
	NA81	NA82	NA83	NA84	NA86
A	1.0	2.1	2.1	2.1	2.1
B	1.0	2.1	2.1	2.1	2.1
C	1.0	2.1	2.1	2.1	2.1
D	1.0	2.1	2.1	2.1	2.1
E	1.0	2.1	2.1	2.1	2.1
F	1.0	2.1	2.1	2.1	2.1
G	1.0	2.1	2.1	2.1	2.1
H	1.0	2.1	2.1	2.1	2.1

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA81	6.0	TBD	8.5
NA82	12.0	TBD	20.1
NA83	16.0	TBD	24.5
NA84	16.0	TBD	24.0
NA86	14.0	TBD	25.4

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA81	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.34 0.62	0.43 0.72	0.55 0.85	0.70 1.01	0.81 1.13
NA82	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.65	0.45 0.83	0.55 0.96	0.65 1.07	0.75 1.19
NA83	**Number of Equivalent Loads**		**1**	**11**	**22**	**32**	**43 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.70	0.47 0.88	0.57 1.01	0.67 1.11	0.78 1.21
NA84	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.34 0.74	0.47 0.92	0.57 1.04	0.66 1.16	0.74 1.27
NA86	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.81	0.48 1.00	0.58 1.16	0.67 1.29	0.77 1.41

Delay will vary with input conditions. See page 2-17 for interconnect estimates.