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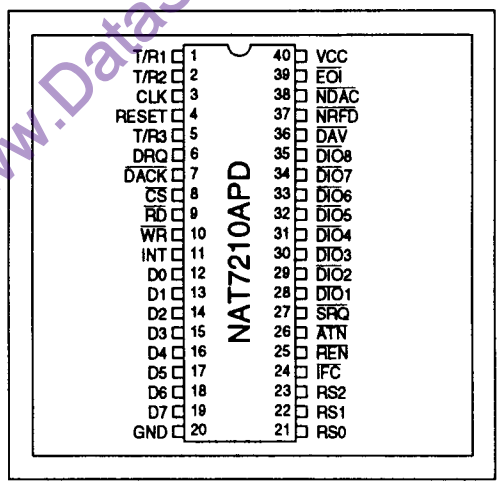
IEEE 488.2 Controller Chip

NAT7210APD
(Preliminary)



NAT7210APD

Features

- Performs all IEEE 488.1 interface functions
  - Source Handshake (SH1)
  - Acceptor Handshake (AH1)
  - Talker or Extended Talker (T5 or TE5)
  - Listener or Extended Listener (L3 or LE3)
  - Service Request (SR1)
  - Remote/Local (RL1)
  - Parallel Poll
    - remote configuration (PP1)
    - local configuration (PP2)
  - Device Clear (DC1)
  - Device Trigger (DT1)
  - Controller, all capabilities (C1, 2, 3, 4, 5)
- Pin compatible with NEC μPD7210
- Meets all IEEE 488.2 requirements
  - Bus line monitoring
  - Preferred implementation of requesting service
  - Will not send messages when there are no Listeners
- Uses 6 primary and secondary addressing modes
  - Automatic single or dual primary addressing detection
  - Automatic single primary with single secondary address detection
  - Single or dual primary with multiple secondary addressing
  - Multiple primary addressing
- Software compatible with NEC μPD7210 or TI TMS9914A controller chips
- Automatic EOS and/or NL message detection
- Direct memory access (DMA)
- Programmable data transfer rate (T1 delays of 350 nsec, 500 nsec, 1.1 μsec, and 2 μsec)
- Automatically processes IEEE 488 commands and reads undefined commands
- Programmably compatible with bus transceivers (TI, National Semiconductor, Motorola, and Intel)
- TTL-compatible CMOS device
- Programmable clock rate up to 20 MHz
- Reduces driver overhead
  - Does not lose a data byte if ATN is asserted while transmitting data
  - Static interrupt status bits that do not clear when read
  - Internal timer interrupt

Description

The NAT7210APD™ is an IEEE 488.2 controller chip that can perform all the interface functions that the IEEE Standard 488.1-1987 defines, and also meets the additional requirements and recommendations of the IEEE Standard 488.2-1987. Connected between the processor and the IEEE 488 bus, the NAT7210APD provides high-level management of the IEEE 488 bus, significantly increases the throughput of driver software, and simplifies both the hardware and software design. The NAT7210APD performs complete IEEE 488 Talker, Listener, and Controller functions. In addition to its numerous improvements, the NAT7210APD is also completely software compatible with the NEC μPD7210 and TI TMS9914A controller chips, and thus is compatible with software from existing designs.

IEEE 488.2 Overview

In 1987, the IEEE 488.2 standard removed the ambiguities of IEEE 488.1 by standardizing the way instruments and controllers operate. It defines data formats, status reporting, error handling, and common configuration commands to which all IEEE 488.2 instruments must respond in a precise manner. It also defines a set of controller requirements. The benefits of IEEE 488.2 for the test system developer are reduced development time and cost, because systems are more compatible and reliable. The future of GPIB is based on IEEE 488.2. The NAT7210APD brings the full power of IEEE 488.2 to the design engineer along with numerous other design and performance benefits.

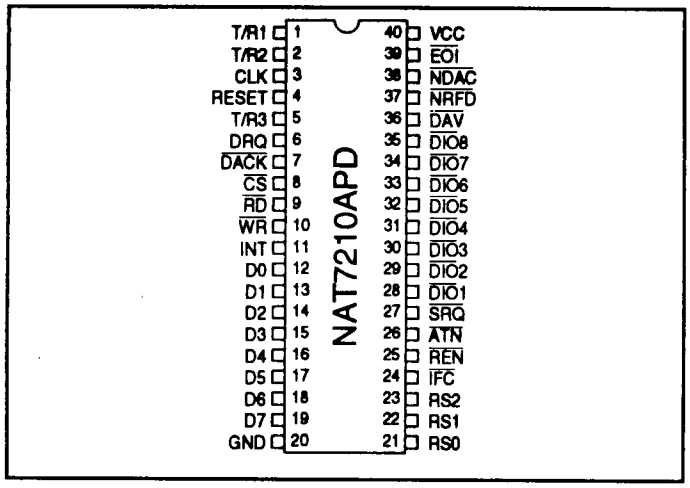


Figure 1. NAT7210 Pin Configuration

Pin Identification

Mnemonic	Type	Description
D(7-0)	I/O¥	Bidirectional 3-state data bus transfers commands, data, and status between the NAT7210APD and the CPU
CS*	I	The chip select gives access to the register selected by a read or write operation, and the register selects RS(2-0)
RD*	I	With the read input, you can place the contents of the register that RS(2-0) and CS* selects onto the data bus D(7-0)
WR*	I¥	The write input latches the contents of the data bus D(7-0) into the register that RS(2-0) selects
DACK*	I¥	The DMA Acknowledge signal selects the DIR or CDOR for the current read or write cycle
DRQ	O	The DMA Request output asserts to request a DMA Acknowledge cycle
CLK	I	The CLK input can be up to 20 MHz
RESET	I	Asserting the RESET input places the NAT7210APD in an initial, idle state
INT	O¥	The interrupt output asserts when one of the unmask interrupt conditions is true
RS(2-0)	I¥	The register selects determine which register to access during a read or write operation
IFC*	I/O¥	Bidirectional control line initializes the IEEE 488 interface functions
REN*	I/O¥	Bidirectional control line selects either remote or local control of devices
ATN*	I/O¥	Bidirectional control line indicates whether data on the DIO lines is an interface or device-dependent message
SRQ*	I/O¥	Bidirectional control line requests service from the controller
DIO(8-1)*	I/O¥	8-bit bidirectional IEEE 488 data bus
DAV*	I/O¥	Handshake line indicates that the data on the DIO(8-1)* lines is valid
NRFD*	I/O¥	Handshake line indicates that the device is ready for data
NDAC*	I/O¥	Handshake line indicates the completion of a message reception
EOI*	I/O¥	Bidirectional control line indicates the last byte of a data message or executes a parallel poll.
T/R1	O	Talk Enable controls the direction of the IEEE 488 data transceiver
T/R(3) T/R(2)	O	These pins are the input/output control for the IEEE 488 transceivers
VCC	-	Power pin – +5 V (±5%)
GND	-	Ground pin – 0 V

¥ The pin contains an internal pull-up resistor of 25 to 100 kΩ.
* Active low.

General

The NAT7210APD manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The NAT7210APD mode determines the function of these registers. When in 7210 mode, the registers resemble the μPD7210 register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. In this mode, the NAT7210APD is completely pin compatible with the NEC μPD7210. When in 9914A mode, the registers resemble the TMS9914A register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. Figure 2 shows the key components of the NAT7210APD.

7210 Mode Registers

The NAT7210APD registers include all the NEC μPD7210 registers plus two types of additional registers – extra auxiliary registers and paged-in registers. You write the extra auxiliary registers the same as standard μPD7210 auxiliary registers. Upon issuing an auxiliary page-in command, the paged-in registers appear at the same offsets as existing μPD7210 registers. At the end of the next CPU access, the chip pages out the paged-in registers. The following table lists all the registers in the 7210 mode register set, along with their associated addressing information.

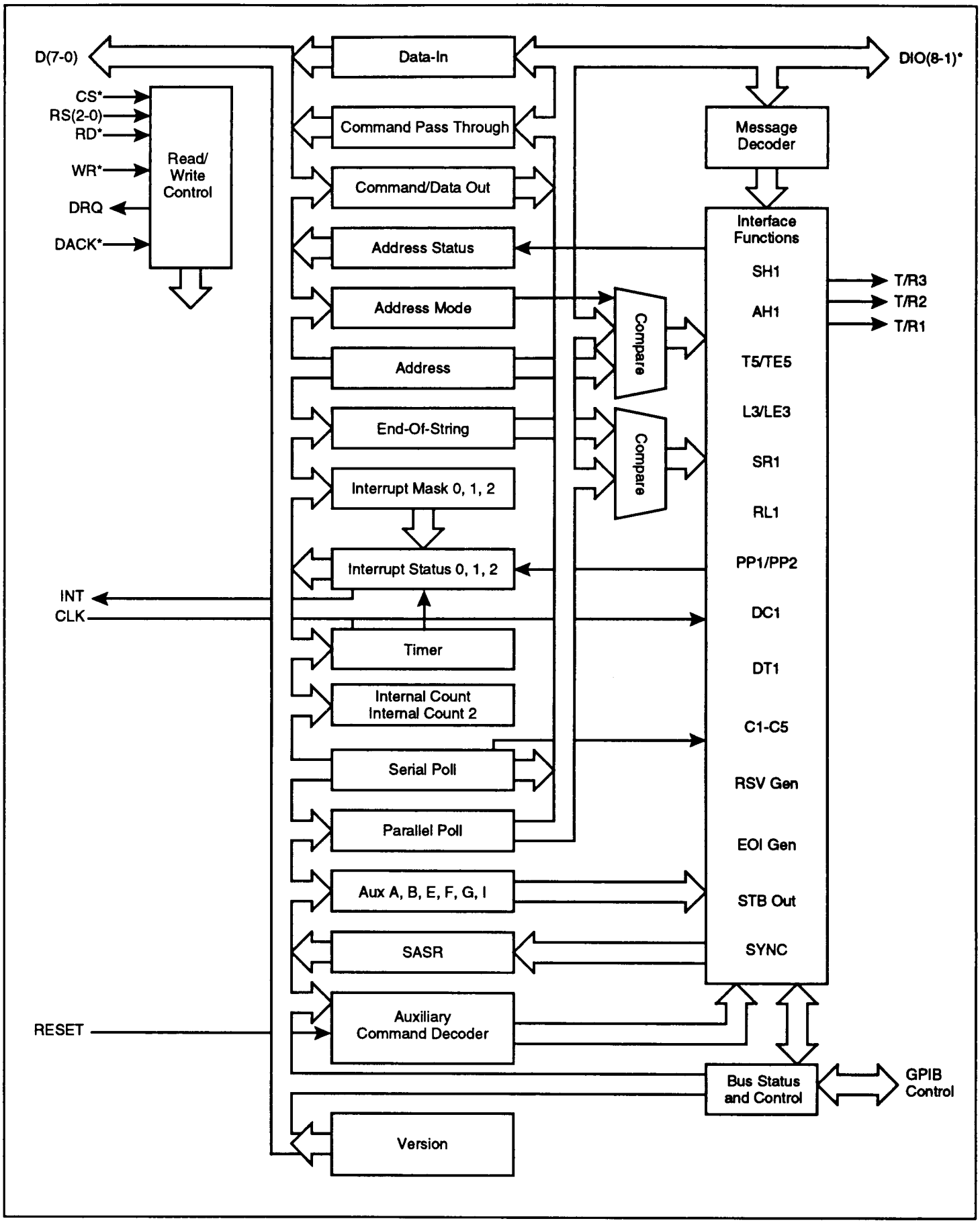


Figure 2. NAT7210 Block Diagram

7210 Register Set

Register	PAGE-IN	A(2-0)	WR*	RD*	CS*	DACK*
Data-In	U	0 0 0	1	0	0	1
Data-In	X	X X X	1	0	X	0
Command/Data-Out	U	0 0 0	0	1	0	1
Command/Data-Out	X	X X X	0	1	X	0
Interrupt Status 1	U	0 0 1	1	0	0	1
Interrupt Mask 1	U	0 0 1	0	1	0	1
Interrupt Status 2	U	0 1 0	1	0	0	1
Interrupt Mask 2	U	0 1 0	0	1	0	1
Serial Poll Status	N	0 1 1	1	0	0	1
Serial Poll Mode	N	0 1 1	0	1	0	1
Version	P	0 1 1	1	0	0	1
Internal Counter 2	P	0 1 1	0	1	0	1
Address Status	U	1 0 0	1	0	0	1
Address Mode	U	1 0 0	0	1	0	1
Command Pass Through	N	1 0 1	1	0	0	1
Auxiliary Mode	U	1 0 1	0	1	0	1
Source/Acceptor Status†	P	1 0 1	1	0	0	1
Address 0	N	1 1 0	1	0	0	1
Address	N	1 1 0	0	1	0	1
Interrupt Status 0†	P	1 1 0	1	0	0	1
Interrupt Mask 0†	P	1 1 0	0	1	0	1
Address 1	N	1 1 1	1	0	0	1
End-Of-String	N	1 1 1	0	1	0	1
Bus Status†	P	1 1 1	1	0	0	1
Bus Control†	P	1 1 1	0	1	0	1

Notes for the PAGE-IN Column

U = The page-in auxiliary command does not affect the register.

N = The register offset is alway valid except for immediately after a page-in auxiliary command.

P = The register is valid only immediately after a page-in auxiliary command.

The '†' symbol denotes features (such as registers and auxiliary commands) that are not available in the µPD7210 or TMS9914A.

DATA REGISTERS

Data-In Register (DIR)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Command/Data-Out Register (CDOR)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

The data registers transfer data and commands between the IEEE 488 bus and the CPU. The Data-In Register (DIR) holds data sent from the GPIB to the CPU, and the Command/Data-Out Register (CDOR) holds information to transfer onto the IEEE 488 bus.

INTERRUPT REGISTERS

Interrupt Status Register 0 (ISR0) †

CDBA	STBO	NL	EOS	IFCI	ATNI	TO	SYNC

Interrupt Status Register 1 (ISR1)

CPT	APT	DET	END	DEC	ERR	DO	DI

Interrupt Status Register 2 (ISR2)

INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

Interrupt Mask Register 0 (IMR0) †

GLINT	STBO	NLEN	BTO	IFCI	ATNI	TO	SYNC

Interrupt Mask Register 1 (IMR1)

CPT	APT	DET	END	DEC	ERR	DO	DI

Interrupt Mask Register 2 (IMR2)

X	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

The interrupt registers consist of interrupt status bits, interrupt mask bits, and some noninterrupt-related bits. There are 18 conditions that can cause an interrupt. The interrupt status bit sets if its condition is true and an interrupt is generated if you set the corresponding interrupt mask bit. Unless you set the SISB bit in Auxiliary Register I, most interrupt status bits clear when read. In this case, the status bits clear when you issue another auxiliary command or take another action. The following tables list the individual bits in the interrupt registers along with descriptions.

Interrupt Status/Mask Register Bits

Bit	Description
INT	OR of all unmasked interrupt status bits
STBO†	Status Byte Out Request
IFCI†	Interface Clear (IFC) asserted
ATNI†	Attention (ATN) asserted
TO†	Time Out
SYNC†	GPIB Handshake Synchronized
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger (DTAS)
END	END (EOI or EOS message received)
DEC	Device Clear (DCAS)
ERR	Data Transmission Error (No Listener)
DO	Data Out (SGNS)
DI	Data In
SRQI	Service Request Input
CO	Command Out
LOKC	Lockout State Change
REMC	Remote State Change
ADSC	Address Status Change
GLINT†	Global Interrupt Enable

Noninterrupt-Related, Readable Bits

Bit	Description
CDBA†	Command or Data Byte Available
NL†	New Line Received
EOS†	End-Of-String
LOK	Lockout (LWLS = RWLS)
REM	Remote (REMS = RWLS)

Noninterrupt-Related, Writable Bits

Bit	Description
NLEN†	New Line character enabled for EOS
BTO†	Enable/Disable Byte Timeouts
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

SERIAL POLL REGISTERS

Serial Poll Status Register (SPSR)

S8	PEND	S6	S5	S4	S3	S2	S1

Serial Poll Mode Register (SPMR)

S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode Register holds the STB (status byte: S8, S6 through S1) that transmits over the GPIB when you serial poll the NAT7210APD, and also holds the local rsv message (request service). The STB automatically transmits when you serial poll the NAT7210APD and you clear the STBO bit in IMR0. When you set STBO (†), the STB does not transmit during serial polls until you write to the SPMR. You can read the SPMR through the SPSR. Setting rsv sets the PEND bit. The PEND bit clears when entering Negative Poll Response State (NPRS) and when rsv clears.

Version Register (VSR) †

V3	V2	V1	V0	X	X	X	X

V(3:0) in the VSR indicates the version of the NAT7210 and should read 0100 for the NAT7210APD.

ADDRESS REGISTERS

The NAT7210APD contains several registers that control the GPIB address mode and store the GPIB address(es). These registers also monitor the GPIB address status.

Address Status Register (ADSR)

CIC	ATN*	SPMS	LPAS	TPAS	LA	TA	MJMN

Address Mode Register (ADMR)

TON	LON	TRM1	TRM0	0	0	ADM1	ADM0

The Address Mode Register selects the NAT7210APD address mode and controls the mode for the transceiver control outputs, T/R2 and T/R3. The TRM1 and TRM0 bit values control T/R2 and T/R3, as demonstrated in the following table.

Function of T/R2 and T/R3

TRM1	TRM0	T/R2	T/R3
0	0	EOIOE	TRIG
0	1	CIC	TRIG
1	0	CIC	EOIOE
1	1	CIC	PE

Notes for the T/R2 and T/R3 columns

EOIOE = TACS + SPAS + CIC & ~CSBS
CIC = ~(CIDS + CADS)
PE = CIC + ~PPAS
TRIG = DTAS or trigger auxiliary command issued

The following table lists the different addressing modes of the NAT7210APD.

Address Modes

ton	lon	adm1	adm0	Address Mode	Contents of Registers ADR0	ADR1
1	0	0	0	Talk Only	GPIB address not necessary (no controller)	
0	1	0	0	Listen Only	GPIB address not necessary (no controller)	
0	0	0	1	Address Mode 1	Major address	Minor address
0	0	1	0	Address Mode 2	Primary address	Secondary address
0	0	1	1	Address Mode 3	Primary major address	Primary minor address

Notes for the Address Mode column

Mode 1 The NAT7210APD recognizes its MTA/MLA if the received address matches either ADR0 or ADR1; interface function Talker/Listener (T/L).

Mode 2 Address Register 0 = primary address; Address Register 1= secondary address; interface function Talker Extended/ Listener Extended (TE/LE).

Mode 3 The CPU must read the secondary address through the Command Pass Through Register; interface function Talker Extended/Listener Extended (TE/LE).

Address Status Bits

Bit	Description
ATN*	GPIB ATN signal
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller-In-Charge
LA	Listener Addressed
TA	Talker Addressed
MJMN	Set if minor T/L addressed Clear if major T/L addressed
SPMS	Serial Poll Mode State

Address Register 0 (ADR0)

X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0

Address Register 1 (ADR1)

EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1

Address Register 0/1 (ADR)

ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

The NAT7210APD automatically detects two types of addresses in ADR0 and ADR1. The following table describes the function of each bit.

Address Register 0/1 Bits

Bit	Description
ARS	Selects either address register 0 or 1
DT1-0	Prohibits the talk address from being detected
DL1-0	Prohibits the listen address from being detected
AD5-0	Lower five bits of GPIB address
EOI	Holds the value of EOI line when data is received

COMMAND PASS THROUGH REGISTER (CPTR)

CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

With the Command Pass Through Register, the CPU can read GPIB DIO lines 8 through 1 in the cases of undefined commands, secondary addresses, or parallel poll responses.

END-OF-STRING REGISTER (EOSR)

EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0

The End-Of-String Register holds either the seven or eight-bit EOS message byte that the GPIB system uses to detect the end of a data block.

GPIB SOURCE/ACCEPTOR STATUS REGISTER (SASR)

CDBA	AEHS	ANHS1	ANHS2	ADHS	ACRDY	SH1A	SH1B

The CPU can monitor the Source and Acceptor handshake functions via the Source/Acceptor Status Register. The following table lists each bit in the SASR, along with a description.

Source/Acceptor Status Bits

Bit	Description
CDBA	Command or Data Byte Available local message
AEHS	Acceptor Holding Off on End State
ANHS1	Acceptor Holding Off on All or End State
ANHS2	Acceptor Holding Off because a Holdoff Handshake Immediate command was issued
ADHS	Acceptor in a DAC Holdoff State
ACRDY	Acceptor in ACRS
SH1(A-B)	Source Handshake Status SH1(A-B)=00 SH1 in SIDS or SGNS SH1(A-B)=1X SH1 in SDYS SH1(A-B)=01 SH1 in STRS

AUXILIARY MODE REGISTER (AUXMR)

CNT2	CNT1	CNT0	CNT4	CNT3	CNT2	CNT1	CNT0

The Auxiliary Mode Register is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits and COM4. The following table shows bit patterns that you must write to the AUXMR to access the hidden registers.

Auxiliary Mode Operations

CNT			COM					
2	1	0	4	3	2	1	0	Operation
0	X	0	C4	C3	C2	C1	C0	Issues an auxiliary command that C4 to C0 specifies
0	0	1	0	T3	T2	T1	T0	Writes to the Internal Counter Register
0	1	1	U	S	P3	P2	P1	Writes to the parallel poll register
1	0	0	A4	A3	A2	A1	A0	Writes to the Auxiliary Register A
1	0	1	B4	B3	B2	B1	B0	Writes to the Auxiliary Register B
1	1	0	0	E3†	E2†	E1	E0	Writes to the Auxiliary Register E
1	1	0	1	F3	F2	F1	F0	Writes to the Auxiliary Register F (†)
0	1	0	0	G3	G2	G1	G0	Writes to the Auxiliary Register G (†)
1	1	1	0	I3	I2	I1	I0	Writes to the Auxiliary Register I (†)
1	1	1	1	J3	J2	J1	J0	Writes to the Auxiliary Register J (†)

Auxiliary Commands

CNT	COM		
210	43210	Command	Operation
000	00000	pon	Generates the local pon message
000	00010	chrst	Chip reset
000	00011	rhdf	Release RFD holdoff
000	00100	trig	Trigger
000	0x101	rtl	Sets the Return to Local (rtl) message if x =1; clears or pulses rtl if x =0
000	00110	seoi	Send EOI with next byte
000	00111	nvld	Nonvalid (OSA reception); release DAC holdoff
000	01111	vld	Valid (MSA Reception, CPT,DEC,DET); release DAC holdoff
000	01000†	rqc	Request Control
000	00001	ist=0	Clear parallel poll flag: ist
000	01001	ist=1	Sets parallel poll flag: ist
000	01010†	rlc	Release Control
000	01011†	lut	Untalk
000	01100†	lul	Unlisten
000	01110†	nbaf	New Byte Available False
000	10000	gts	Go To Standby
000	10001	tca	Take Control Asynchronously
000	10010	tcs	Take Control Synchronously
000	11010	tcse	Take Control Synchronously on End
000	10011	ltn	Listen
000	11011	ltn&cnt	Listen in Continuous Mode
000	11100	lun	Local Unlisten
000	10100	~rsc	Disable System Control
000	10101†	9914	Switch to 9914A Mode
000	11110	sic&rsc	Sets IFC and rsc
000	10110	~sic	Clears IFC
000	11111	sre&rsc	Sets REN and rsc
000	10111	~sre	Clears REN
000	11000†	reqt	Issue reqt message
000	11001†	reqf	Issue reqf message
000	11101	rpp	Execute a parallel poll
010	10000†	page	Page in additional registers
010	10001†	hldi	Holdoff handshake immediately
010	1001X	rsvd	Reserved
010	10100†	clrDET	Clear DET bit in ISR1
010	10101†	clrEND	Clear END bit in ISR1
010	10110†	clrDEC	Clear DEC bit in ISR1
010	10111†	clrERR	Clear ERR bit in ISR1
010	11000†	clrSRQI	Clear SRQI bit in ISR2
010	11001†	clrLOKC	Clear LOKC bit in ISR2
010	11010†	clrREMC	Clear REMC bit in ISR2
010	11011†	clrADSC	Clear ADSC bit in ISR2
010	11100†	clrIFCI	Clear IFCI bit in ISR0
010	11101†	clrATNI	Clear ATNI bit in ISR0
010	11110†	clrSYNC	Clear SYNC bit in ISR0
010	11111†	setSYNC	Set SYNC bit in ISR0

INTERNAL COUNTER REGISTER (ICR)

0	0	1	0	T3	T2	T1	T0

The Internal Counter Register tells the internal circuitry in the NAT7210APD the clock frequency supplied to the CLK input.

For Proper operation, set T(3-0) and MICR as follows:

Clock Frequency	MICR	T(3-0)
1	0	0001
2	0	0010
3	0	0011
4	0	0100
5	0	0101
6	0	0110
7	0	0111
8	0	1000
10	1	0101
16	1	1000
20	1	1010

Note: On a hardware reset, T(3-0) and MICR are set to 8 MHz.

Internal Counter Register 2 (ICR2) †

1	0	0	0	0	0	0	MICR

The Internal Counter Register 2 contains bits that control NAT7210 functions. Setting the MICR bit in the KCR doubles the operating frequency of the clock input that T(3-0) specifies in the Internal Counter Register. If MICR = 0, T(3-0) = 0-8 MHz; if MCR=1 T(3-0) = 0-20 MHz. The Internal Counter Register 2, along with the Internal Counter Register, determines the length of delays that IEEE 488.1 requires. Refer to the Internal Counter Register description for information on the proper setting of this register.

PARALLEL POLL RESPONSE REGISTER (PPR)

0	1	1	U	S	P3	P2	P1

The Parallel Poll Response Register determines the NAT7210APD parallel poll response. The following table shows each bit in the register, along with the function of each bit.

Parallel Bit	Response Poll	Function
U	0 1	Respond to parallel polls Do not respond to parallel polls
S	0 1	Reverse Phase In Phase
P3-P1	000-111	Status bit output line DIO1(P3-1= 000) to DIO8(P3-1 = 111)

AUXILIARY REGISTER A (AUXRA)

1	0	0	A4	A3	A2	A1	A0

Auxiliary Register A, a five-bit register, controls the NAT7210APD GPIB data receiving mode; and controls how the EOS message is used, as listed in the table below.

Data Receiving Modes

A1	A0	Data Receiving Mode
0	0	Normal Handshake Mode
0	1	RFD Holdoff on All Data Mode
1	0	RFD Holdoff on END Mode
1	1	Continuous Mode

EOS

Bit		Function
A2	0 Prohibit 1 Permit	Permits (prohibits) the setting of the END bit by the reception of the EOS message
A3	0 Prohibit 1 Permit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message while in TACS
A4	0 7-bit 1 8-bit	Selects 7 or 8-bits as the valid length of the EOS message

AUXILIARY REGISTER B (AUXRB)

1	0	1	B4	B3	B2	B1	B0

Auxiliary Register B, a five-bit register, controls special NAT7210APD operating features, as listed in the table below.

Special Features

Bit		Function
B0	0 Prohibit 1 Permit	Permits (prohibits) the detection of an undefined command by setting the CPT bit on receipt of an undefined command and performing a DAC holdoff
B1	0 Prohibit 1 Permit	Permits (prohibits) the transmission of the END message when in Serial Poll Active State (SPAS)
B2	0 low-speed 1 high-speed	Permits high-speed T1 (500 to 350 ns) in the source handshake function after transmission of first byte following ATN unasserting. If cleared, prohibits high-speed T1
B3	0 high 1 low	Specifies the active level of the INT pin
B4	1 SRQS 0 Parallel Poll flag	Determines if the ist local message value is equal to SRQS or the Parallel Poll Flag

AUXILIARY REGISTER E (AUXRE)

1	1	0	0	E3	E2	E1	E0

Auxiliary Register E, four-bit register, controls DAC holdoff modes, as listed in the table below.

Special Features

Bit	Name	Function
E0	DHDC	DAC Holdoff on DCAS
E1	DHDT	DAC Holdoff on DTAS
E2 †	DHADC	DAC Holdoff on DCL or SDC
E3 †	DHADT	DAC Holdoff on GET

AUXILIARY REGISTER F †(AUXRF)

1	1	0	1	F3	F2	F1	F0

Auxiliary Register F, a four-bit register, controls DAC Holdoff modes, as listed in the table below.

Special Features

Bit	Name	Function
F0	DHALL	DAC Holdoff on all UCG, ACG, and SCG commands
F1	DHUNLT	DAC Holdoff on UNL and UNT
F2	DHALA	DAC Holdoff on all Listener addresses
F3	DHATA	DAC Holdoff on all Talker addresses

AUXILIARY REGISTER G †(AUXRG)

0	1	0	0	G3	G2	G1	G0

Auxiliary Register G, a four-bit register, controls special NAT7210APD operational features, as listed in the table below.

Special Features

Bit	Name	Function
G0	CHES	Enables END detector circuitry clearing on the reception of a data byte without END
G1	DISTCT	When this bit is set, the NAT7210APD cannot take control when control is passed to it
G2	RPP2	Request Parallel Poll local message
G3	NTNL	Setting this bit prevents the NAT7210APD from sourcing a data or command byte when there are no listeners on the GPIB

AUXILIARY REGISTER I †(AUXRI)

1	1	1	0	I3	I2	0	I0

Auxiliary Register I, a four-bit register, controls special NAT7210APD operational features. The following table lists these features.

Special Features

Bit	Name	Function
I0	SISB=0	Reads of the Interrupt status registers clear Interrupt status bits
	SISB=1	Issuing the appropriate auxiliary command (or the conditions listed below) clears Interrupt status bits
I2	PP2	When set, the NAT7210APD ignores remote GPIB parallel poll configure commands
I3	USTD	This bit and AUXRB bit B2 control the T1 delay used when sourcing command and data bytes (see chart below)

The following table lists the different T1 delays that the NAT7210APD handles.

AUX B2 Bit	AUX I3 Bit	T1 for first data and all commands	T1 for the second and remaining data
0	0	2 µsec	2 µsec
0	1	1.1 µsec	1.1 µsec
1	0	2 µsec	500 nsec
1	1	1.1 µsec	350 nsec

The following table lists the clear conditions of each interrupt status bit when SISB is set.

Bit	Clear Condition when SISB=1
CPT	pon + read CPTR
APT	pon + Valid + Non-Valid
DET	pon + Clear DET
END	pon + Clear END
DEC	pon + Clear DEC
ERR	pon + Clear ERR
DO	pon + ~TACS + ~SGNS + nba
DI	pon + (finish handshake) * (Holdoff mode) + read DIR
SRQI	pon + clear SRQI
CO	pon + ~CACS + ~SGNS + nba
LOKC	pon + clear LOKC
REMC	pon + clear REMC
ADSC	pon + clear ADSC + ton + lon
IFCI	pon + clear IFCI
ATNI	pon + clear ATNI

AUXILIARY REGISTER J †(AUXRJ)

1	1	1	1	J3	J2	J1	J0

Auxiliary Register J, a four-bit register, sets the timeout value of the timer interrupt. You can set the timeout value between the range of 15 µsec to 125 sec. The timer starts when the AUXRJ is written with a non-zero value and sets the TO bit in the ISR0 when the timeout value has expired. The following chart lists the approximate timeout values.

J3-0	Timeout Value (> or =)
0000	Disabled
0001	15 µsec
0010	30 µsec
0011	125 µsec
0100	250 µsec
0101	1 msec
0110	4 msec
0111	15 msec
1000	30 msec
1001	125 msec
1010	250 msec
1011	1 sec
1100	4 sec
1101	15 sec
1110	30 sec
1111	125 sec

The timer handles two different types of timeouts, depending on the BTO bit value. If BTO is cleared, the timer operates in global mode. In global mode, the timer starts upon writing a nonzero value to the AUXRJ, and continues counting until it reaches the timeout value, which sets the TO bit. If BTO is set, the timer operates in byte timeout mode. In byte timeout mode, the timer starts upon writing a nonzero value to the AUXRJ, and continues counting until it reaches the timeout value. However, DIR reads or CDOR writes will clear the timer and force it to start counting again. In Byte Timeout mode, after TO is set, it will remain set until the AUXRJ is written. Further reads of DIR or writes of CDOR will have no effect on TO until the AUXRJ is written.

GPIB BUS CONTROL/STATUS REGISTERS † (BCR/BSR)

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

The CPU can monitor the GPIB by reading the Bus Status Register. You can assert (drive low) GPIB signals by setting the corresponding bit in the GPIB Control Register to 1.

9914 Mode Registers

In 9914 mode, the NAT7210APD registers consist of all the TI TMS9914A registers and two types of additional registers – newly defined registers and paged-in registers. The NAT7210 maps the newly defined registers into the unused portion of the 9914 address space. Each paged-in register appears at offset 2 immediately after you issue an auxiliary page-in command, and it remains there until you page another register into the same space or you issue a reset. The following table lists all the registers in the 9914 register set.

9914 Register Set

Register	Page In	RS(2-0)	WR*	RD*	CS*	DACK*
Interrupt Status 0	U	0 0 0	1	0	0	1
Interrupt Mask 0	U	0 0 0	0	1	0	1
Interrupt Status 1	U	0 0 1	1	0	0	1
Interrupt Mask 1	U	0 0 1	0	1	0	1
Address Status	U	0 1 0	1	0	0	1
Interrupt Mask 2 †	P	0 1 0	0	1	0	1
End-of-String †	P	0 1 0	0	1	0	1
Bus Control †	P	0 1 0	0	1	0	1
Accessory †	P	0 1 0	0	1	0	1
Bus Status	U	0 1 1	1	0	0	1
Auxiliary Command	U	0 1 1	0	1	0	1
Interrupt Status 2 †	P	1 0 0	1	0	0	1
Address	U	1 0 0	0	1	0	1
Serial Poll Status †	P	1 0 1	1	0	0	1
Serial Poll Mode	U	1 0 1	0	1	0	1
Command Pass Thru	U	1 1 0	1	0	0	1
Parallel Poll	U	1 1 0	0	1	0	1
Data-In	U	1 1 1	1	0	0	1
Data-In	U	X X X	1	0	X	0
Command/Data-Out	U	1 1 1	0	1	0	1
Command/Data-Out	U	X X X	0	1	X	0

Notes for the PAGE-IN column

U = Page-in auxiliary commands do not affect the register offset.

P = The register offset is valid only after a page-in auxiliary command.

DATA REGISTERS

Data-In Register (DIR)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Command/Data Out Register (CDOR)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

The data registers transfer data and commands between the IEEE 488 bus and the CPU. The Data-In Register (DIR) holds data sent from the GPIB to the CPU, and the CDOR holds information to transfer onto the IEEE 488 bus.

INTERRUPT REGISTERS

Interrupt Status Register 0 (ISR0)

INT0	INT1	BI	BO	END	SPAS	RLC	MAC

Interrupt Status Register 1 (ISR1)

GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC

Interrupt Status Register 2 (ISR2) †

CDBA	STBO	NL	EOS	LLOC	ATN	TO	CIC

Interrupt Mask Register 0 (IMR0)

DMAO†	DMAI†	BI IE	BO IE	END IE	SPAS IE	RLC IE	MAC IE

Interrupt Mask Register 1 (IMR1)

GET IE	ERR IE	UNC IE	APT IE	DCAS IE	MA IE	SRQ IE	IFC IE

Interrupt Mask Register 2 (IMR2) †

GL INT	STBO IE	NL EN	BTO	LLOC IE	ATN IE	TO IE	CIC IE

The interrupt registers consist of interrupt status bits, interrupt mask bits, and some noninterrupt-related bits. There are 19 conditions that can cause an interrupt. The interrupt status sets if its condition is true and an interrupt will be generated if you set the corresponding mask bit. Most interrupt status bits are cleared when read. The following tables list the individual bits in the interrupt registers, along with descriptions.

Interrupt Status and/or Mask Register Bits

Bits	Description
INT0	OR of all unmasked ISR0 bits
INT1	OR of all unmasked ISR1 bits
BI	Byte In
BO	Byte Out
END	END (EOI or EOS message received)
SPAS	SPAS (Serial Poll Active State)
RLC	Remote/Local Change
MAC	My Address Change
GET	Group Execute Trigger
ERR	Data Transmission Error
UNC	Unrecognized Command
APT	Address Pass Through
DCAS	Device Clear Active State
MA	My Address
SRQ	Service Request (SRQ)
IFC	Interface Clear (IFC) asserted
STBO †	Status Byte Out Request
LLOC †	Lockout State Change
ATN †	Attention (ATN) asserted
TO †	Time Out
CIC †	Controller-In-Charge
GLINT †	Global Interrupt Enable

Noninterrupt-Related, Readable Bits

Bits	Description
CDBA †	Command or Data Byte Available
NL †	New Line Received
EOS †	End-Of-String

Noninterrupt-Related, Writable Bits

Bits	Description
NLEN †	New Line character enabled for EOS
BTO †	Enable/Disable Byte Timeouts
DMAO †	Enable/Disable DMA Out
DMAI †	Enable/Disable DMA In

SERIAL POLL REGISTERS

Serial Poll Status Register (SPSR) †

S8	PEND	S6	S5	S4	S3	S2	S1

Serial Poll Mode Register (SPMR)

S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode Register holds the STB (status byte: S8, S6 through S1) that transmits over the GPIB when you serial poll the NAT7210APD and also holds the local rsv message (request service). The STB automatically transmits when you serial poll the NAT7210APD and when you clear the STBO IE. When you set the STBO IE bit in IMR2 (†), the STB does not transmit during serial polls until you write to the SMPR. You can read the SPMR through the SPSR. SPSR is only accessable if a register pages into offset 2. The PEND bit sets when rsv sets and clears by Negative Poll Response State when rsv clears.

ADDRESS REGISTERS

The NAT7210APD contains two registers that control the GPIB address mode, store the GPIB address, and monitor the GPIB address status.

ADDRESS STATUS REGISTER (ADSR)

REM	LLO	ATN	LPAS	TPAS	LA	TA	ULPA

The address status register monitors the NAT7210APD address state. The following table lists the ADSR bits, along with a description of each bit.

Address Status Bits

Bit	Description
REM	The NAT7210 is in the Remote state
LLO	The NAT7210 is in the Local Lockout state
ATN	GPIB ATN signal
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
LA	Listener Addressed
TA	Talker Addressed
ULPA	Stores the LSB of the last address recognized by the NAT7210

ADDRESS REGISTER (ADR)

EDPA	DAL	DAT	A5	A4	A3	A2	A1

The NAT7210APD can automatically detect the address in ADR as its MTA or MLA. The following table lists the function of each bit.

Address Register Bits

Bit	Description
EDPA	Enables Dual Addressing mode, in which the least significant address bit is ignored, giving the NAT7210APD two consecutive GPIB addresses
DAL	Prohibits the Listen address from being detected
DAT	Prohibits the Talk address from being detected
A5-0	GPIB primary address

COMMAND PASS THROUGH REGISTER (CPTR)

CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

With the Command Pass Through Register (CPTR), the CPU can read the GPIB DIO (8-1) lines in the cases of undefined commands, secondary addresses, or parallel poll responses.

PARALLEL POLL REGISTER (PPR)

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1

The PPR contains the value that the NAT7210APD outputs on the GPIB when the Controller-In Charge conducts a parallel poll. To participate in a parallel poll, the bit corresponding to the desired parallel poll response is set to 1. The parallel poll register is double buffered. Therefore, if it is written during a parallel poll, the register updates with the new value at the end of the parallel poll.

END-OF-STRING REGISTER † (EOSR)

EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0

The EOS Register holds either the seven or eight-bit EOS message byte that the GPIB system uses to detect the end of a data block.

AUXILIARY COMMAND REGISTER

C/S	X	X	F4	F3	F2	F1	F0

A write to this register generates one of the following operations according to the C/S and F (4-0) values.

Auxiliary Commands

C/S	F 43210	Command	Operation
0/1	00000	swrst	Clear/Set software reset
0	00001	dacr	Invalid DAC release Holdoff
1	00001	dacr	Valid DAC release Holdoff
X	00010	rhdf	Release RFD Holdoff
0/1	00011	hlda	Clear/Set Holdoff on All Data

(continues)

(continued)

C/S	F 43210	Command	Operation
0/1	00100	hlde	Clear/Set Holdoff on END only
X	00101	nbaf	New Byte Available False
0/1	00110	fget	Clear/Set Force Group Execute Trigger
0/1	00111	rtl	Clear/Set Return to Local
X	01000	seoi	Send EOI with next byte
0/1	01001	lon	Clear/Set Listen Only
0/1	01010	ton	Clear/Set Talk Only
X	01011	gts	Go To Standby
X	01100	tca	Take Control Asynchronously
X	01101	tcs	Take Control Synchronously
0/1	01110	rpp	Clear/Set Request Parallel Poll
0/1	01111	sic	Clear/Set Send Interface Clear
0/1	10000	sre	Clear/Set Send Remote Enable
X	10001	rqc	Request Control
X	10010	rlc	Release Control
0/1	10011	dai	Clear/Set Disable All Interrupts
X	10100	pts	Pass Through Next Secondary
0/1	10101	stdl	Clear/Set Short T1 settling time
0/1	10110	shdw	Clear/Set Shadow Handshake
0/1	10111	vstdl	Clear/Set Very Short T1 delay
0/1	11000	rsv2	Clear/Set Request Service Bit 2
0	11001	rsvd	Reserved
1	11001 †	sw7210	Switch to µPD7210 Mode
0	11010 †	reqf	Send Reqf
1	11010 †	reqt	Send Reqt
X	11011	rsvd	Reserved
0	11100 †	chrst	Chip Reset
1	11100 †	clrpi	Clear Page-In Registers
0/1	11101 †	ist	Clear/Set Parallel Poll Flag
0	11110 †	piimr2	Page-In Interrupt Mask 2 Register
1	11110 †	pieosr	Page-In End-Of-String Register
0	11111 †	pibcr	Page-In Board Control Register
1	11111 †	piaccr	Page-In Accessory Register

ACCESSORY REGISTER † (ACCR)

CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

The ACCR is a multipurpose register. A write to this register generates one of the following operations according to the CNT bit and COM4 values.

Auxiliary Mode Operations

CNT			COM					Operation
2	1	0	4	3	2	1	0	
0	0	1	0	T3	T2	T1	T0	Writes to the Internal Counter Register
1	0	0	A4	A3	A2	0	0	Writes to the Auxiliary Register A
1	0	1	B4	B3	B2	B1	B0	Writes to the Auxiliary Register B
1	1	0	0	E3	E2	E1	E0	Writes to the Auxiliary Register E
1	1	0	1	F3	F2	F1	F0	Writes to the Auxiliary Register F
1	1	0	0	I3	I2	I1	I0	Writes to the Auxiliary Register I
1	1	0	0	J3	J2	J1	J0	Writes to the Auxiliary Register J

INTERNAL COUNTER REGISTER (ICR)

0	0	1	0	T3	T2	T1	T0

The Internal Counter Register tells the internal circuitry in the NAT7210 the clock frequency supplied to the CLK input.

For proper operation, set T(3-0) and MICR as follows:

Clock Frequency	MICR	T(3-0)
1	0	0001
2	0	0010
3	0	0011
4	0	0100
5	0	0101
6	0	0110
7	0	0111
8	0	1000
10	1	0101
16	1	1000
20	1	1010

Note: On a hardware reset, T(3-0) and MICR are set to 8 MHz.

AUXILIARY REGISTER A † (AUXRA)

1	0	0	A4	A3	A2	0	0

Auxiliary Register A, a three-bit register, controls how you use the EOS message, as listed in the table below.

EOS Message

Bit		Function
A2	**0 Prohibit** 1 Permit	Permits (prohibits) setting End bit when receiving the EOS message
A3	**0 Prohibit** 1 Permit	Permits (prohibits) automatic transmission of END message simultaneously with EOS message transmission while in TACS
A4	**0 7-bit** 1 8-bit	Selects 7 or 8 bits as the valid EOS message length

AUXILIARY REGISTER B † (AUXRB)

1	0	1	B4	B3	B2	B1	B0

Auxiliary Register B, a five-bit register, controls special NAT7210APD operating features, as listed in the table below.

Special Features

Bit		Function
B0	**0 Prohibit** 1 Permit	Permits (prohibits) the NAT7210APD to automatically take control of the GPIB when control is passed to it (TCT)
B1	**0 Prohibit** 1 Permit	Permits (prohibits) END message transmission when in Serial Poll Active State (SPAS)
B2	**0 Prohibit** 1 Permit	Permits (prohibits) the NAT7210APD to accept and respond to the GPIB commands that it sources
B3	**0 high** 1 low	Specifies the INT pin active level
B4	**1 SRQS** 0 Parallel Poll flag	Determines if the ist local message value is equal to SRQS (B4=1) or the Parallel Poll Flag (B4=0)

AUXILIARY REGISTER E †(AUXRE)

1	1	0	0	E3	E2	E1	E0

AUXRE, a four-bit register, controls DAC holdoff modes, as listed in the table below.

Special Features

Bit	Name	Function
E0	DHDC	DAC Holdoff on DCAS
E1	DHDT	DAC Holdoff on DTAS
E2	DHADC	DAC Holdoff on DCL or SDC
E3	DHADT	DAC Holdoff on GET

AUXILIARY REGISTER F † (AUXRF)

1	1	0	1	F3	F2	F1	F0

AUXRF, a four-bit register, controls DAC Holdoff modes, as listed in the table below.

Special Features

Bit	Name	Function
F0	DHALL	DAC Holdoff on all UCG, ACG, and SCG commands
F1	DHUNLT	DAC Holdoff on UNL and UNT
F2	DHALA	DAC Holdoff on all Listener addresses
F3	DHATA	DAC Holdoff on all Talker addresses

AUXILIARY REGISTER I † (AUXRI)

1	1	1	0	I3	I2	0	I0

AUXRI, a four-bit register, controls special NAT7210APD operational features, as listed in the table below.

Special Features

Bit	Name	Function
I0	DMAEN=0 DMAEN=1	DRQ is asserted if either a Byte In (BI) or Byte Out (BO) condition occurs DRQ is asserted if the BI and DMAI bits are set or the BO and the DMAO bits are set
I2	PP1	When set, the NAT7210APD responds to remote GPIB parallel poll configure commands and automatically responds to parallel polls
I3	USTD	Enables 350 nsec (T1) delays

AUXILIARY REGISTER J †(AUXRJ)

1	1	1	1	J3	J2	J1	J0

AUXRJ, a four-bit register, sets the timeout value of the timer interrupt. You can set the timeout value between the range of 15 µsec to 125 sec. The timer starts when the AUXRJ is written with a nonzero value. When the timeout value expires, the TO bit in ISR0 sets. The following chart lists the approximate timeout values.

J3-0	Timeout Value (> or =)
0000	Disabled
0001	15 µsec
0010	30 µsec
0011	125 µsec
0100	250 µsec
0101	1 msec
0110	4 msec
0111	15 msec
1000	30 msec
1001	125 msec
1010	250 msec
1011	1 sec
1100	4 sec
1101	15 sec
1110	30 sec
1111	125 sec

The timer handles two different types of timeouts depending on the BTO bit value. If you clear BTO, the timer operates in global mode. In global mode, the timer starts upon writing a non-zero value to the AUXRJ and continues counting until the chip reaches the timeout value, which sets the TO bit. If you set BTO, the timer operates in byte timeout mode. In byte timeout mode, the timer starts writing a nonzero value to the AUXRJ and continues counting until the chip reaches the timeout value. However, DIR reads or CDOR writes will clear the timer and force it to start counting again. In byte timeout mode, after the chip sets TO, it will remain set until you write to the AUXRJ. Further reads of DIR or writes of CDOR will have no effect on TO until you write to the AUXRJ.

GPIB CONTROL/STATUS REGISTERS † (BCR/BSR)

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

The CPU can monitor the GPIB by reading the Bus Status register. You can assert (drive low) GPIB signals by setting the corresponding bit in the GPIB Control Register to 1.

Advanced DC Characteristics

T_A 0 to 70°C; V_{CC} = 5 V ± 5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Voltage input low	V_{IL}	-0.5	+0.8	V	
Voltage input high	V_{IH}	+2.0	V_{CC}	V	
Voltage output low	V_{OL}	0	0.4	V	
Voltage output high	V_{OH}	+2.4	VCC	V	
Input/output leakage current		-10	+10	µA	without internal pull-up
Onput/output leakage current		TBD	TBD	µA	with internal pull-up
Supply current			TBD	mA	
Output current low					
All pins except T/R1	I_{OL}		2	mA	0.4 V @ I_{OL}
T/R1	I_{OL}		4	mA	0.4 V @ I_{OL}
Input current low/high	I_{IL}/I_{IT}	TBD			without pull-up with pull-up

Capacitance

T_A 0 to 70°C; V_{CC} = 5 V ± 5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Input capacitance	C_{IN}		TBD	pF	
Output capacitance	C_{OUT}		TBD	pF	
I/O capacitance	$C_{I/O}$		TBD	pF	

Absolute Maximum Ratings

Property	Range
Supply voltage, V_{CC}	-0.5 to +6.0 V
Input voltage, V_I	-0.5 to V_{CC} +0.5
Operating temperature, T_{OPR}	0 to +70° C
Storage temperature, T_{STG}	-40 to +125° C

Comment: Exposing the device to stresses above those listed could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Timing Waveforms

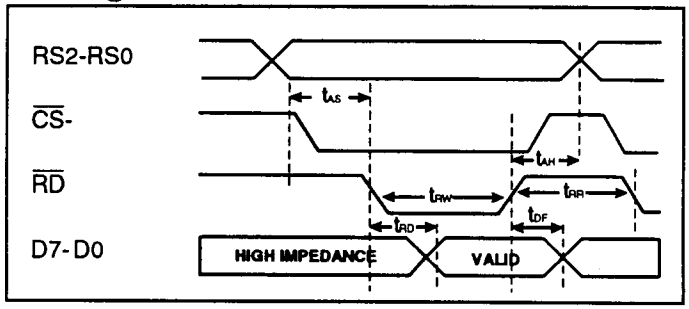


Figure 3. CPU Read

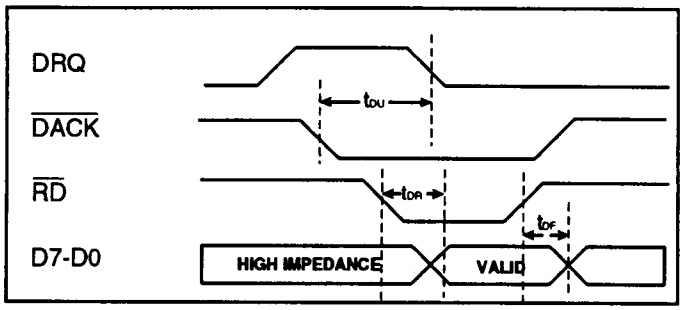


Figure 4. DMA Read

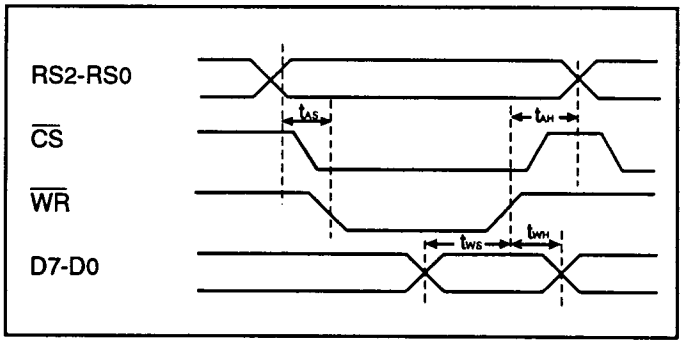


Figure 5. CPU Write

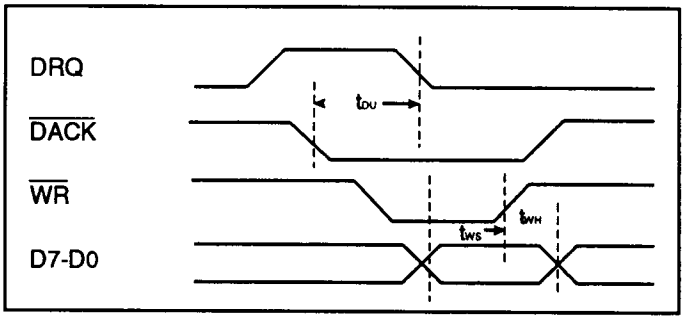


Figure 6. DMA Write

AC Characteristics

T_A 0 to 70°C; V_{CC} = 5 V ± 5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Address setup to $\overline{RD}$↓, $\overline{WR}$↓	t_{AS}	TBD		nsec	
Data delay from $\overline{RD}$↓, $\overline{CS}$=0	t_{RD}		TBD	nsec	
Data float from $\overline{RD}$↑	t_{DF}		TBD	nsec	
$\overline{RD}$ pulse width	t_{RW}	TBD		nsec	
$\overline{RD}$ recovery width	t_{RR}	TBD		nsec	
Address hold from $\overline{RD}$↑, $\overline{WR}$↑	t_{AH}	TBD		nsec	
DRQ unassertion	t_{DU}		TBD	nsec	
Data dalay from $\overline{RD}$↓, $\overline{DACK}$=0	t_{DR}		TBD	nsec	
Data setup to $\overline{WR}$↑	t_{WS}	TBD		nsec	
Data hold from $\overline{WR}$↑	t_{WH}	TBD		nsec	

Timing Waveforms

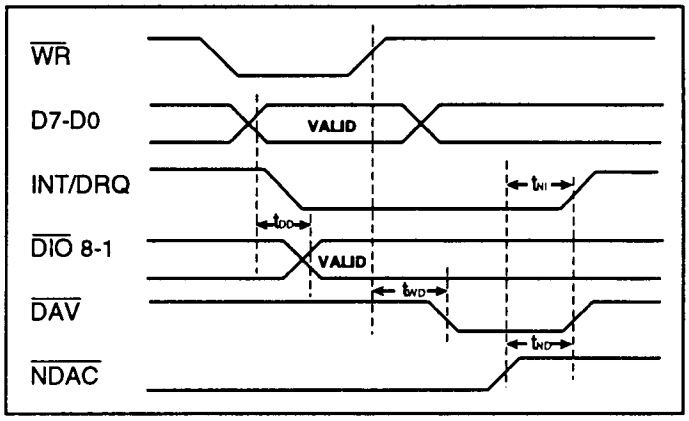


Figure 7. Source Handshake

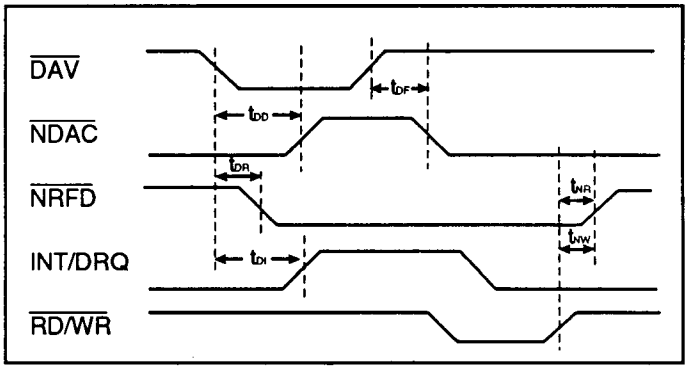


Figure 8. Acceptor Handshake

Response to ATN

Parameter	Symbol	Limits (nsec) Min	Limits (nsec) Max	Test Condition
$\overline{EOI}\downarrow$ to $\overline{DIO}$ valid			TBD	PPSS ↔ PPAS, $\overline{ATN}$ = TRUE
$\overline{EOI}\downarrow$ to TE↑			TBD	PPSS ↔ PPAS, $\overline{ATN}$ = TRUE
$\overline{EOI}\uparrow$ to TE↓			TBD	PPSS ↔ PPAS, $\overline{ATN}$ = TRUE
$\overline{ATN}\downarrow$ to $\overline{NDAC}\downarrow$			TBD	AIDS → ANRS
$\overline{ATN}\uparrow$ to $\overline{NRFD}\downarrow$			TBD	Acceptor handshake holdoff
$\overline{ATN}\downarrow$ to TE↓			TBD	TACS → TADS

Source Handshake

Parameter	Symbol	Limits (nsec) Min	Limits (nsec) Max	Test Condition
Delay of $\overline{DIO}$ valid from D valid	t_{DD}		TBD	
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		TBD	2 µsec T1
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		TBD	1.1 µsec T1
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		TBD	500 nsec T1
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		TBD	350 nsec T1
Delay of $\overline{DAV}\downarrow$ from $\overline{WR}\uparrow$	t_{WD}		TBD	200 nsec T1
Delay of $\overline{DAV}\uparrow$ from $\overline{NDAC}\uparrow$	t_{ND}		TBD	
Delay of INT↑ or DRQ↑ from $\overline{NDAC}\uparrow$	t_{NI}		TBD	INT(DOIE Bit=1) DRQ(DMAO Bit=1)

ø = a rising edge on CLK

Acceptor Handshake

Parameter	Symbol	Limits (nsec) Min	Limits (nsec) Max	Test Condition
Delay of $\overline{NDAC}\uparrow$ from $\overline{DAV}\downarrow$	t_{DD}		TBD	
Delay of $\overline{NRFD}\downarrow$ from $\overline{DAV}\downarrow$	t_{DR}		TBD	
Delay of INT↑ or DRQ↑ from $\overline{DAV}\downarrow$	t_{DI}		TBD	INT(DIIE Bit=1), DRQ (DMAI Bit=1)
Delay of $\overline{NDAC}\downarrow$ from $\overline{DAV}\uparrow$	t_{DF}		TBD	
Delay of $\overline{NRFD}\uparrow$ from $\overline{RD}\uparrow$	t_{NR}		TBD	Read of DIR, not in Holdoff state
Delay of $\overline{NRFD}\uparrow$ from $\overline{WR}\uparrow$	t_{NW}		TBD	In Holdoff state, issuing finish handshake auxiliary command

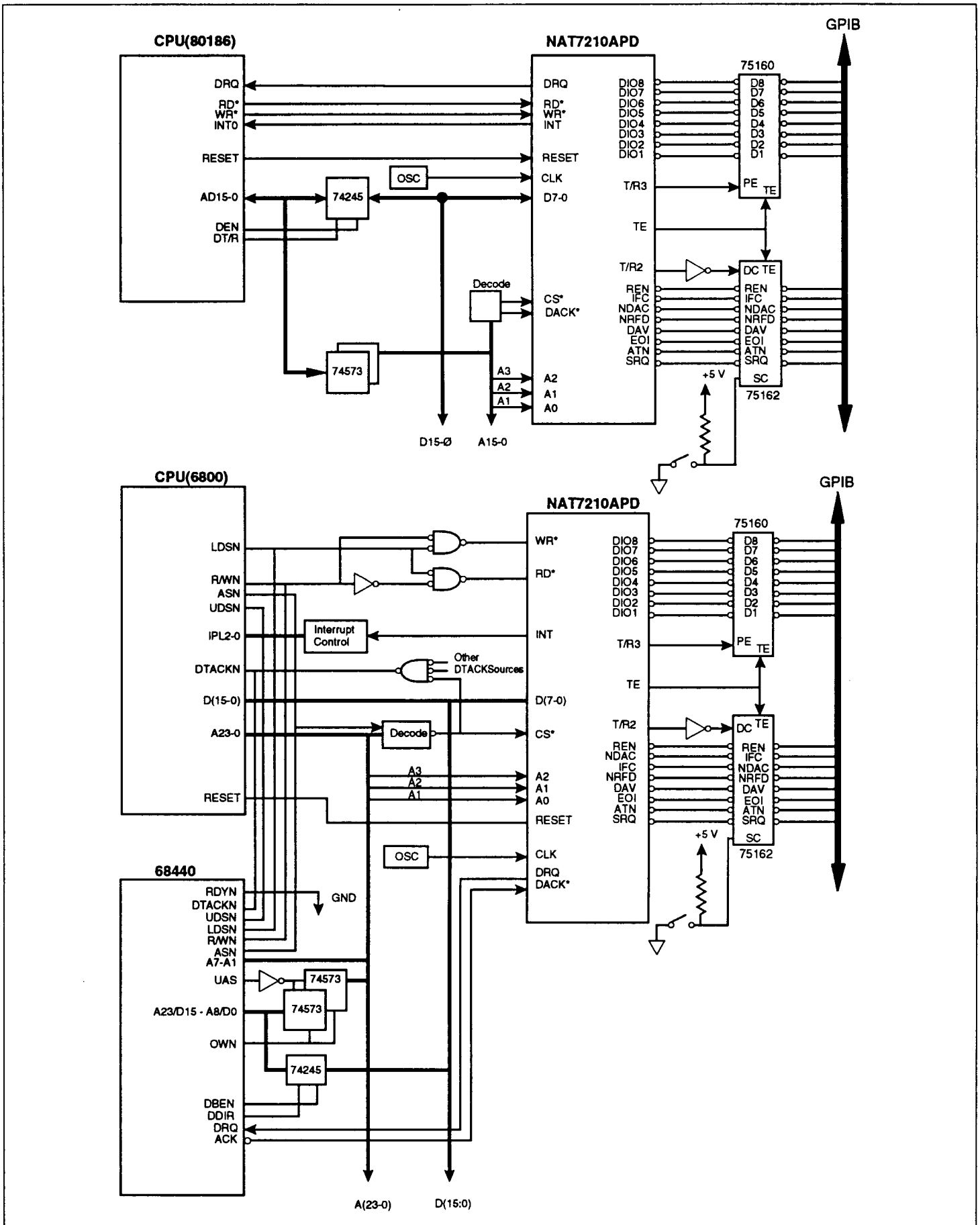


Figure 9. Typical CPU Systems with NAT7210 APD

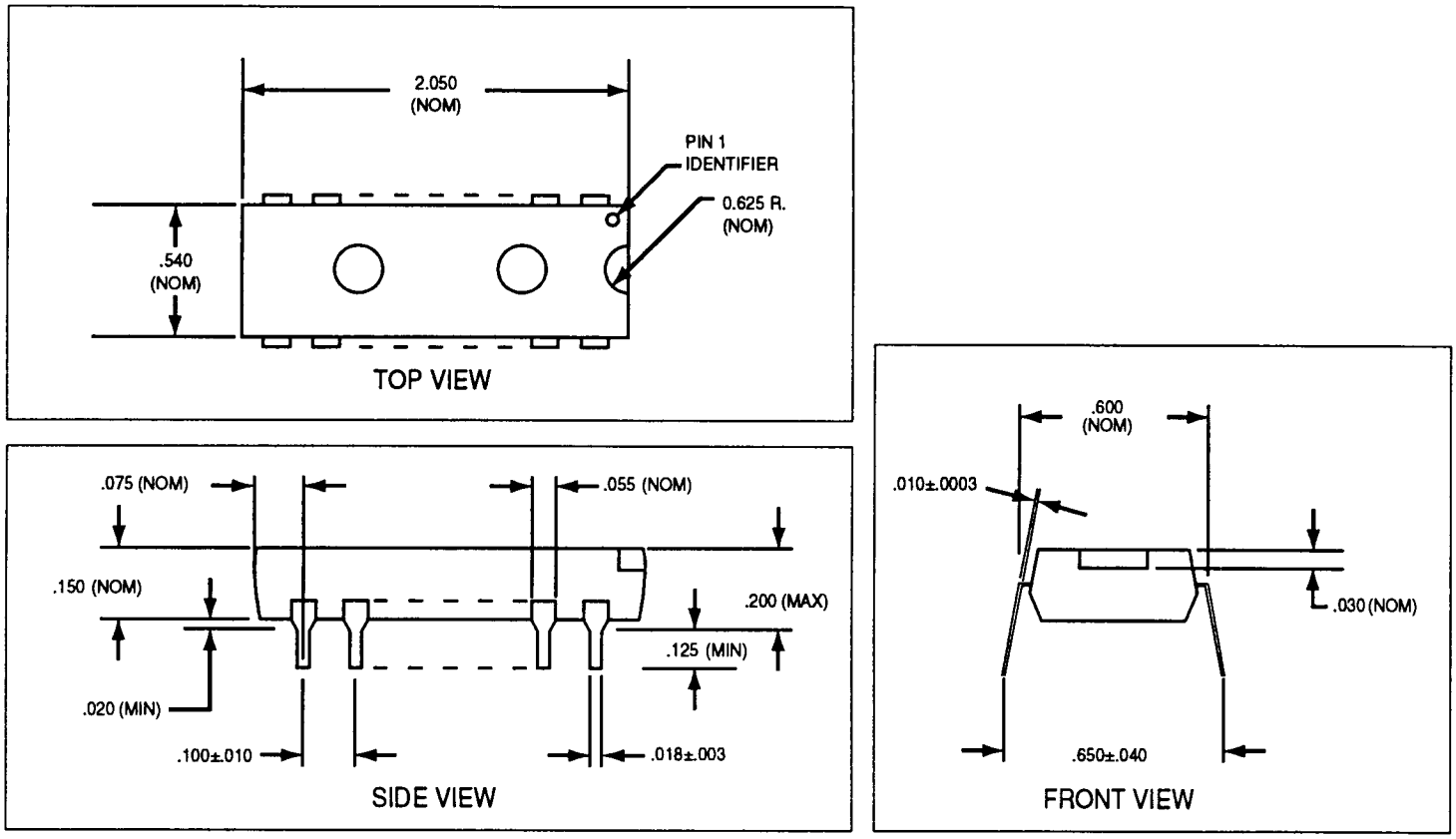


Figure 10. Mechanical Data 40-Pin Plastic DIP

Ordering Information

Corporate Headquarters
6504 Bridge Point Parkway
Austin, TX 78730-5039
(512) 794-0100
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Fax: (512) 794-8411

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