NB3L8543S

2.5 V/3.3 V Differential 2:1 MUX to 4 LVDS Clock Fanout Buffer Outputs with Clock Enable and Clock Select

ON Semiconductor®

www.onsemi.com

Description

The NB3L8543S is a high performance, low skew 1−to−4 LVDS Clock Fanout Buffer.

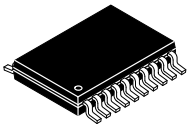
The NB3L8543S features a multiplexed input which can be driven by either a differential or single−ended input to allow for the distribution of a lower speed clock along with the high speed system clock.

The CLK_SEL pin will select the differential CLK and $\overline{\text{CLK}}$ inputs when LOW (or left open and pulled LOW by the internal pull−down resistor). When CLK_SEL is HIGH, the differential PCLK and $\overline{\text{PCLK}}$ inputs are selected.

The common clock enable pin, CLK_EN, is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse on the outputs during asynchronous assertion/deassertion of the clock enable pin. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

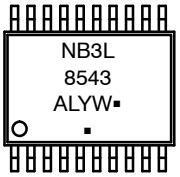
Features

- Four Differential LVDS Output Pairs
- Two Selectable Differential Clock Inputs
- CLK/$\overline{\text{CLK}}$ Can Accept LVPECL, LVDS, HCSL, SSTL and HSTL
- PCLK/$\overline{\text{PCLK}}$ Can Accept LVPECL, LVDS, CML and SSTL
- Maximum Output Frequency: 650 MHz
- Additive Phase Jitter, RMS: 50 fs (typical)
- Output Skew: 40 ps (maximum)
- Part−to−part Skew: 200 ps (maximum)
- Propagation Delay: 1.9 ns (maximum)
- Operating Range: V_{DD} = 2.5 V ±5% or 3.3 V ±10%
- −40°C to +85°C Ambient Operating Temperature Range
- TSSOP−20 Package
- These are Pb−Free Devices



TSSOP−20
DT SUFFIX
CASE 948E

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

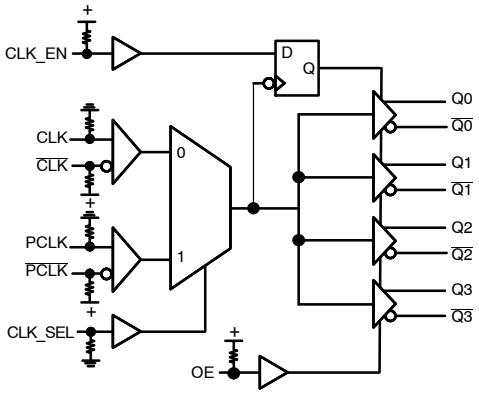


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

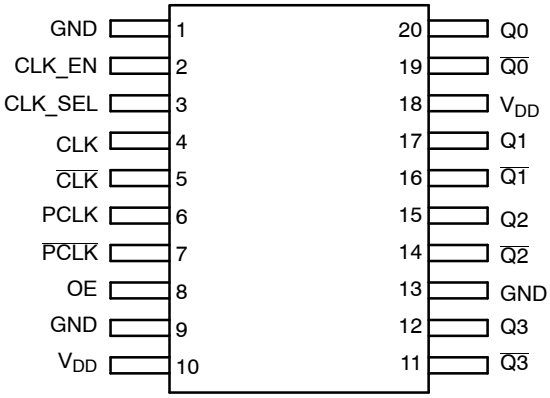


Figure 2. Pinout Diagram (Top View)

Table 1. PIN DESCRIPTION

Number	Name	I/O	Open Default	Description
1, 9, 13	GND	Power		Negative (Ground) Power Supply pins must be externally connected to power supply to guarantee proper operation.
2	CLK_EN	NC	Pullup	Synchronized Clock Enable when HIGH. When LOW, outputs are disabled (Qx HIGH, $\overline{Qx}$ LOW). See Figure 3.
3	CLK_SEL	NC	Pulldown	Clock Input Select (HIGH selects PCLK/$\overline{PCLK}$, LOW selects CLK/$\overline{CLK}$ input
4	CLK	Input	Pulldown	True Standard Clock Input. Float open when unused.
5	$\overline{CLK}$	Input	Pullup	Invert Standard Clock Inputs. Float open when unused.
6	PCLK	Input	Pulldown	True Peripheral Clock Input. Float open when unused.
7	$\overline{PCLK}$	Input	Pullup	Invert Peripheral Clock Inputs. Float open when unused.
8	OE	NC	Pullup	Output Enable Control. When HIGH, the outputs are active and enabled. When LOW, the outputs are high impedance disabled.
10 ,18	VDD	Power		Positive Power Supply pin must be externally connected to power supply to guarantee proper operation.
11, 14, 16, 19	$\overline{Q[3:0]}$	Output		Invert LVDS Outputs
12, 15, 17, 20	Q[3:0]	Output		True LVDS Outputs

Table 2. FUNCTIONS

	Inputs			Outputs		
OE	CLK_EN	CLK_SEL	Input Function	Output Function	Qx	$\overline{Qx}$
0	X	X			HI−Z	HI−Z
1	0	0	CLK input selected	Disabled	LOW	HIGH
1	0	1	PCLK Input Selected	Disabled	LOW	HIGH
1	1	0	CLK input selected	Enabled	CLK	Invert of CLK
1	1	1	PCLK Input Selected	Enabled	PCLK	Invert of PCLK

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in Figure 3.

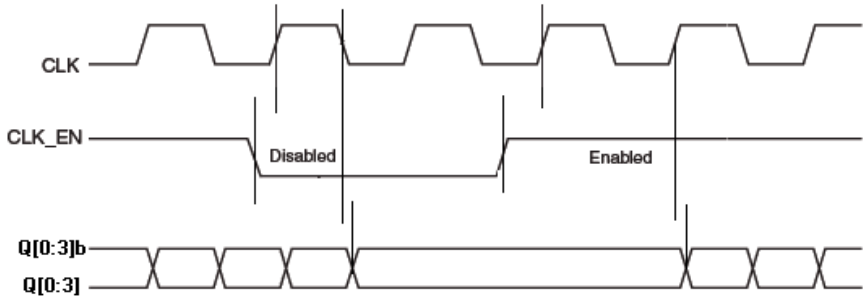


Figure 3. CLK_EN TIMING DIAGRAM

Table 3. ATTRIBUTES (Note 2)

Characteristics		Value
Internal Input Pullup Resistor		50 kΩ
Internal Input Pulldown Resistor		50 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2)		Level 1
Flammability Rating Oxygen Index		UL 94 V−0 @ 0.125 in 28 to 34
Transistor Count		430
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{DD}	Supply Voltage			4.6	V
V_{in}	Input Voltage			$-0.5 \le V_I \le V_{DD} + 0.5$	V
C_{in}	Input Capacitance			4	pF
I_D	Output Current	Continuous Surge		10 15	mA
T_A	Operating Temperature Range, Industrial			−40 to ≤ +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−20	140 50	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 4)	TSSOP−20	23 to 41	°C/W
T_{sol}	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS V_{DD} = 2.5 V ±5% or 3.3 V ±10%, GND = 0 V, T_A = −40°C to +85°C (Note 5)

Symbol	Characteristic		Min	Typ	Max	Unit
POWER SUPPLY						
V_{DD}	Power Supply Voltage	V_{DD} = 3.3 V V_{DD} = 2.5 V	2.97 2.375	3.3 2.5	3.63 2.625	V
I_{DD}	Power Supply Current				50	mA
LVCMOS/LVTTL INPUTS (CLK_EN, CLK_SEL, OE)						
V_{IH}	Input HIGH Voltage	V_{DD} = 3.3 V V_{DD} = 2.5 V	2 1.7		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	V_{DD} = 3.3 V V_{DD} = 2.5 V			0.8 0.7	V
I_{IH}	Input High Current (V_{DD} = V_{IN} = 3.63 V)	CLK_EN, OE $\overline{CLK\_SEL}$			5 150	μA
I_{IL}	Input LOW Current (V_{DD} = 3.63 V, V_{IN} = 0 V)	CLK_EN, OE $\overline{CLK\_SEL}$	−150 −5			μA
DIFFERENTIAL INPUTS (see Figures 5 and 6) (Note 8)						
V_{IHD}	Differential Input HIGH Voltage	CLK PCLK	0.5 1.5		V_{DD}−0.85 V_{DD}	V
V_{ILD}	Differential Input LOW Voltage	CLK PCLK	0 0.5		V_{IHD}−0.15 V_{IHD}	V
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	CLK PCLK	0.15 0.30		1.3 1.0	V
V_{IHCMR}	Common Mode Input Voltage; (Note 9)	CLK PCLK	0.5 1.5		V_{DD}−0.85 V_{DD}	V
I_{IH}	Input HIGH Current	V_{DD} = V_{IN} = 3.63 V CLK, PCLK $\overline{CLK}$, $\overline{PCLK}$			150 5	μA
I_{IL}	Input LOW Current	V_{DD} = 3.63 V, V_{IN} = 0 V CLK, PCLK $\overline{CLK}$, $\overline{PCLK}$	−5 −150			μA
LVDS OUTPUTS						
V_{OD}	Differential Output Voltage		200	300	360	mV
ΔV_{OD}	VOD Magnitude Change			0	40	mV
V_{OS}	Differential Output Voltage Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	VOS Magnitude Change			5	25	mV
I_{OZ}	Output High Impedance Leakage Current		−10		+10	μA
I_{OS}	Output Short Circuit Current			−5		mA
V_{OH}	Output HIGH Voltage			1.34	1.6	V
V_{OL}	Output LOW Voltage		0.9	1.06		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Outputs terminated 100 Ω across Qx and $\overline{Qx}$, see Figure 4. DC Measurements per Figure 10 reference.
6. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
7. V_{th} is applied to the complementary input when operating in single−ended mode.
8. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
9. The common mode voltage is defined as V_{IH}.

Table 6. AC CHARACTERISTICS V_{DD} = 2.5 V ±5% or 3.3 V ±10%, GND = 0 V, T_A = −40°C to +85°C (Note 10)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{MAX}	Maximum Operating Frequency, V_{OUTPP} ≥ 200 mV	V_{DD} = 3.3 V V_{DD} = 2.5 V	0 0		650 500	MHz
t_{PD}	Propagation Delay		0.9		1.9	ns
$t_{J\phi n}$	Additive Phase Jitter, RMS; fC = 156.25 MHz Integration Range: 12 kHz – 20 MHz			0.05		ps
$t_{SKEWO-O}$	Output−to−Output Skew Within A Device			15	40	ps
$t_{SKEWD-D}$	Device−to−Device Skew, similar path and conditions				200	ps
tr/tf	Output rise and fall times @ 50 MHz, 20% to 80%	V_{DD} = 3.3 V V_{DD} = 2.5 V	150 150	250	500 550	ps
ODC	Output Clock Duty Cycle		45	50	55	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Outputs terminated100 Ω across Qx and $\overline{Qx}$, see Figure 4. Measured from differential crosspoints to differential crosspoints, see Figure 11.

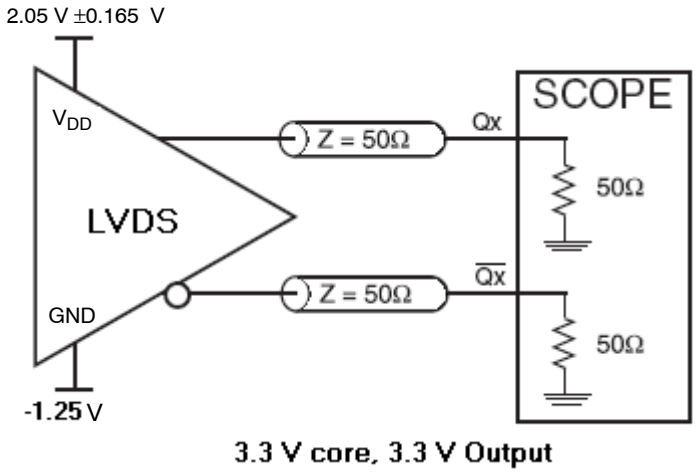


Figure 4. Typical Test Setup and Termination for Evaluation. The V_{DD} of 2.05 V ±0.165 V and GND of −1.25 V Split supply allows a direct connection to an oscilloscope 50 Ω impedance input module.

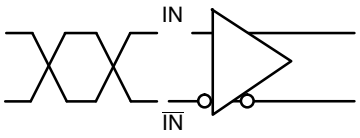


Figure 5. Differential Inputs Driven Differentially

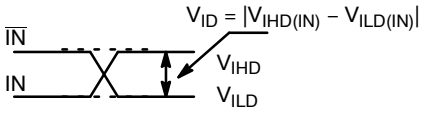


Figure 6. Differential Inputs Driven Differentially

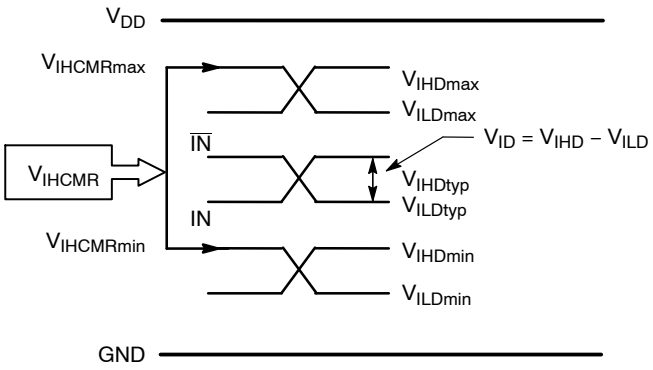


Figure 7. V_{IHCMR} Diagram

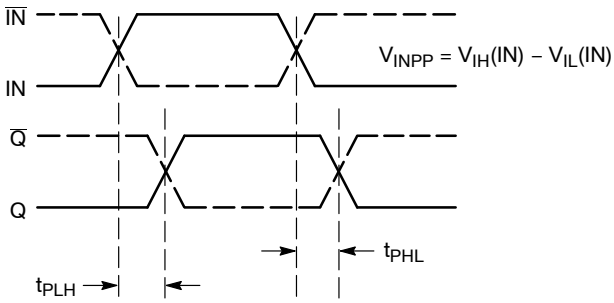


Figure 8. AC Reference Measurement

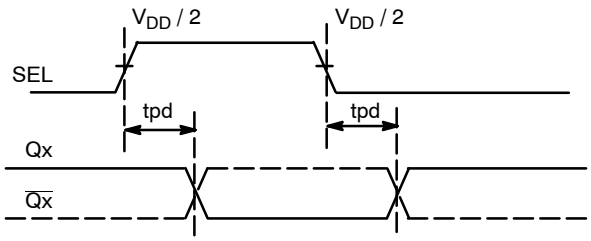
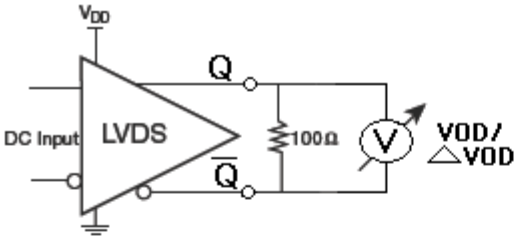
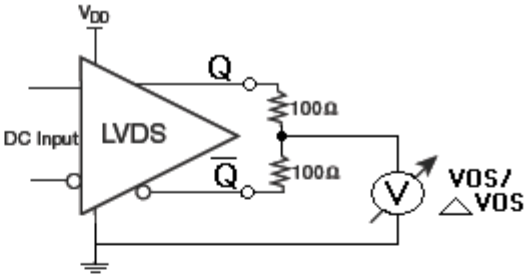


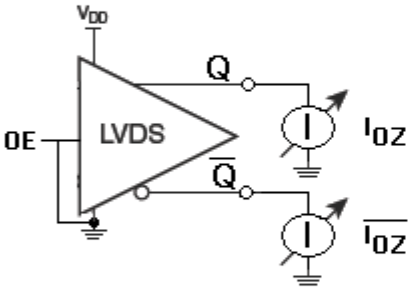
Figure 9. SEL to Qx Timing Diagram



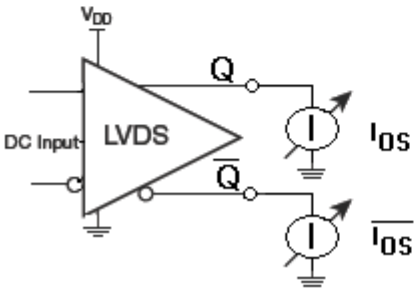
DIFFERENTIAL OUTPUT VOLTAGE



OFFSET VOLTAGE



HIGH IMPEDANCE LEAKAGE CURRENT



OUTPUT SHORT CIRCUIT CURRENT

Figure 10. DC Measurement Reference

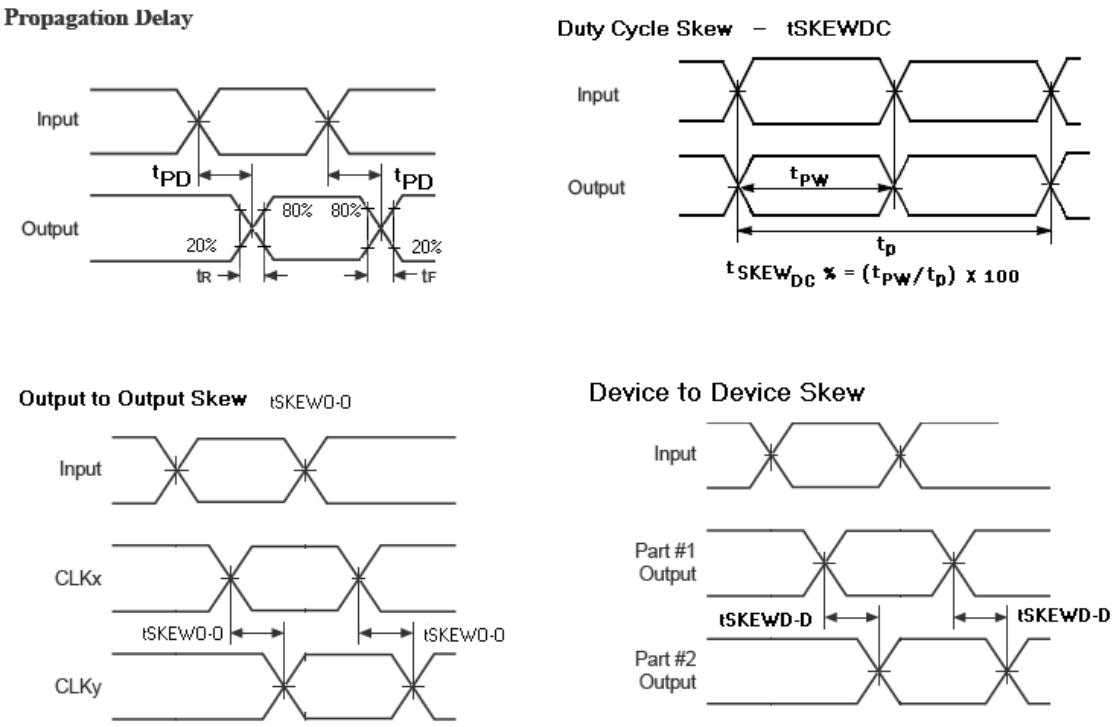


Figure 11. AC Measurement Reference

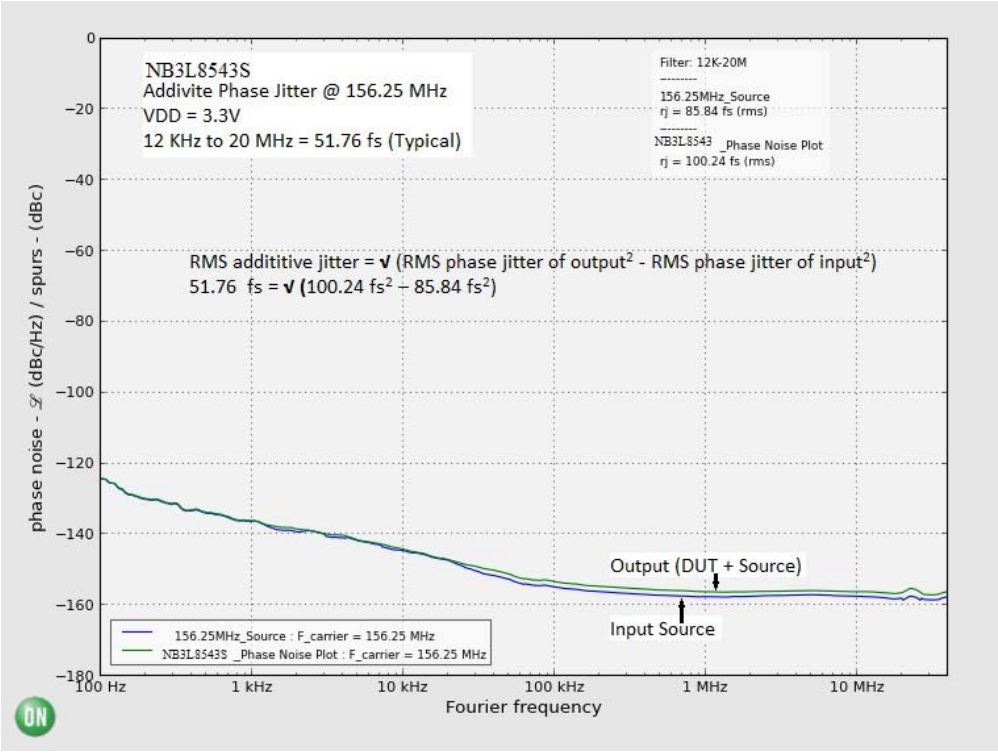


Figure 12. Typical Phase Noise Plot at $f_{carrier}$ = 156.25 MHz at an Operating Voltage of 3.3 V, Room Temperature

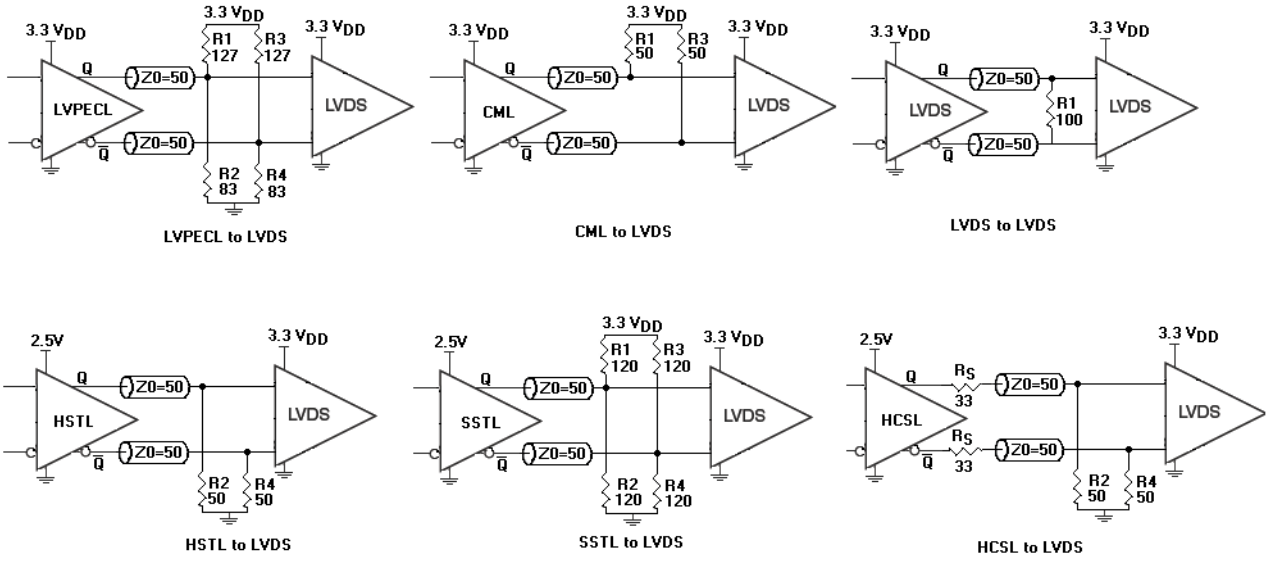


Figure 13. Differential Input Interface From LVPECL, CML, LVDS, HSTL, SSTL, or HCSL

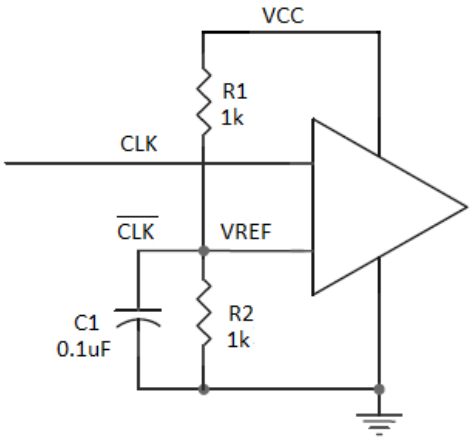


Figure 14. Differential Input Driven Single−ended

Differential Clock Input to Accept Single−ended Input

Figure 14 shows how the CLK input can be driven by a single−ended Clock signal. C1 is connected to the V_{ref} node as a bypass capacitor. Locate these components close the device pins. R1 and R2 must be adjusted to position V_{ref} to the center of the input swing on CLK.

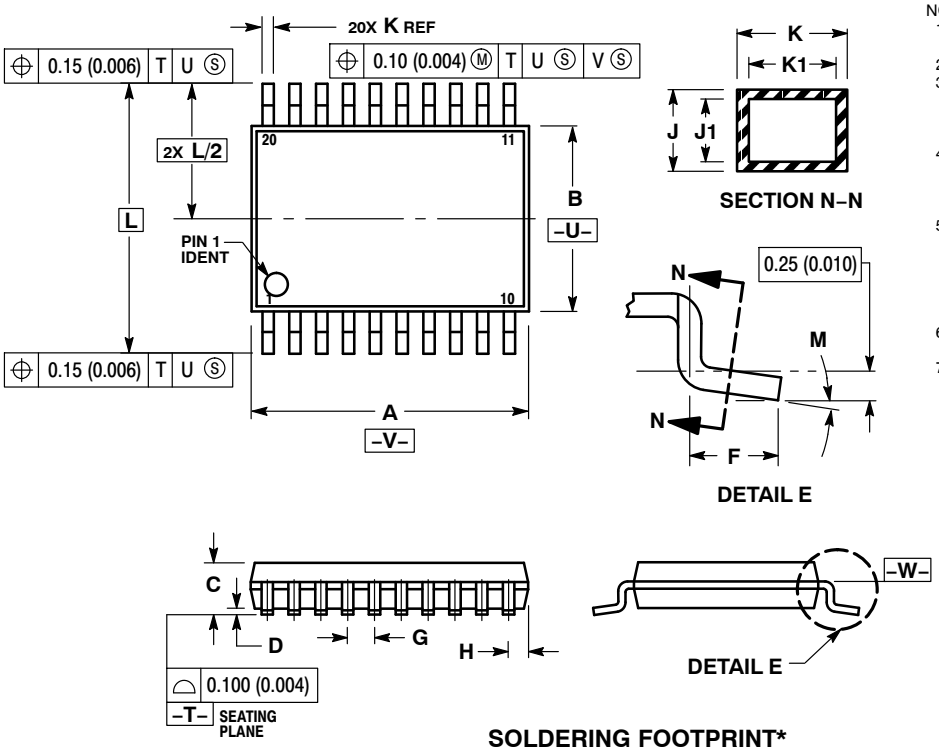
ORDERING INFORMATION

Device	Package	Shipping†
NB3L8543SDTG	TSSOP−20 (Pb−Free)	75 Units / Rail
NB3L8543SDTR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

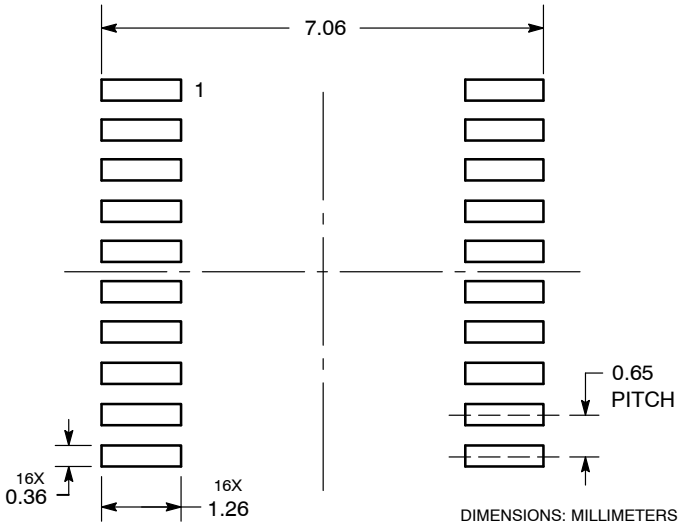
TSSOP−20
CASE 948E−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NB3L8543S/D