

NB3N3002

3.3V, Crystal to 25MHz, 100MHz, 125MHz and 200MHz HCSL Clock Generator



ON Semiconductor®

<http://onsemi.com>

Description

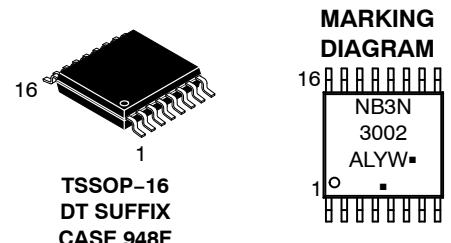
The NB3N3002 is a precision, low phase noise clock generator that supports PCI-Express and Ethernet requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal and generates a differential HCSL output at 25 MHz, 100 MHz, 125 MHz or 200 MHz clock frequencies. Outputs can interface with LVDS with proper termination (See Figure 5).

This device is housed in 5.0 mm x 4.4 mm narrow body TSSOP 16 pin package.

Features

- Uses 25 MHz Fundamental Mode Parallel Resonant Crystal
- External Loop Filter is Not Required
- HCSL Differential Output or LVDS with Proper Termination
- For Selectable Multipliers of the Input Frequency
- Output Enable with Tri-State Outputs
- PCIe Gen1, Gen2, Gen3 Jitter Compliant
- Typical TIE RMS jitter of 2.5 ps
- Phase Noise: @ 100 MHz

Offset	Noise Power
100 Hz	-109.4 dBc
1 kHz	-127.8 dBc
10 kHz	-136.2 dBc
100 kHz	-138.8 dBc
1 MHz	-138.2 dBc
10 MHz	-161.4 dBc
20 MHz	-163.00 dBc
- Operating Range 3.3 V \pm 5%
- Industrial Temperature Range -40°C to +85°C
- These are Pb-Free Devices



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

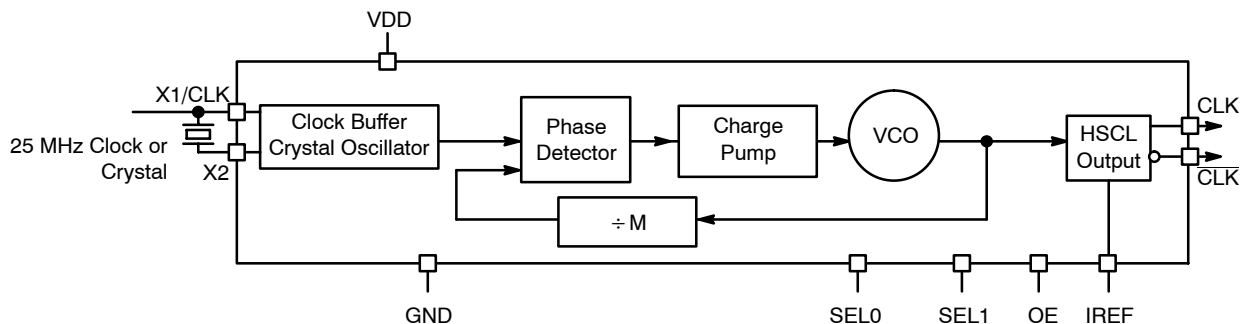


Figure 1. NB3N3002 Simplified Logic Diagram

NB3N3002

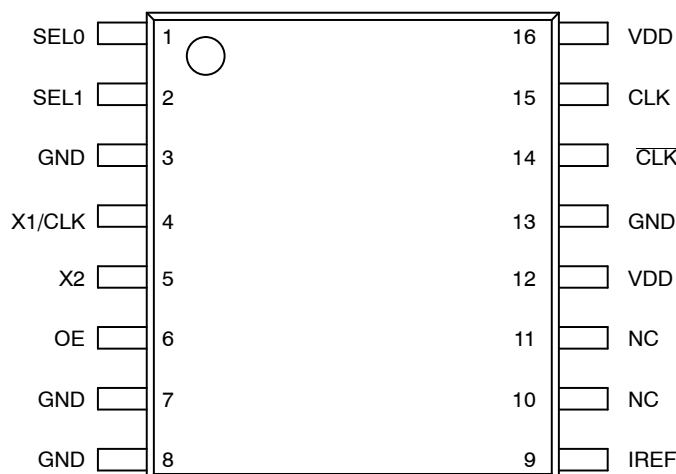


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Symbol	I/O	Description
1	Sel0	Input	LVTTL/LVCMOS frequency select input 0. Internal pullup resistor to V _{DD} . See output select table 2 for details.
2	Sel1	Input	LVTTL/LVCMOS frequency select input 1. Internal pullup resistor to V _{DD} . See output select Table 2 for details.
12, 16	V _{DD}	Power Supply	Positive supply voltage pins are connected to +3.3 V supply voltage.
4	X1/CLK	Input	Crystal or Clock input. Connect to 25 MHz crystal source or single-ended clock.
5	X2	Input	Crystal input. Connect to a 25 MHz crystal or leave unconnected for clock input.
6	OE	Input	Output enable tri-states output when connected to GND. Internal pullup resistor to V _{DD} .
3, 7, 8, 13	GND	Power Supply	Ground 0 V. These pins provide GND return path for the devices.
9	I _{REF}	Output	Output current reference pin. Precision resistor (typ. 475 Ω) is connected from pin 9 to GND to set the output current.
15	CLK	HCSL or LVDS Output	Noninverted clock output. (For LVDS levels see Figure 5)
14	CLK	HCSL or LVDS Output	Inverted clock output. (For LVDS levels see Figure 5)
10,11	NC		Do not connect

Table 2. OUTPUT FREQUENCY SELECT TABLE WITH 25MHz CRYSTALS

SEL1*	SEL0*	CLK Multiplier	f _{CLK} (MHz)
L	L	1x	25
L	H	4x	100
H	L	5x	125
H	H	8x	200

*Pins SEL1 and SEL0 default high when left open.

Recommended Crystal Parameters

Crystal	Fundamental AT-Cut
Frequency	25 MHz
Load Capacitance	16–20 pF
Shunt Capacitance, C ₀	7 pF Max
Equivalent Series Resistance	50 Ω Max
Initial Accuracy at 25 °C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm

NB3N3002

Table 3. ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model	> 2 kV
RPU – OE, SEL0 and SEL1 Pull-up Resistor	100 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	7623
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{DD}	Positive Power Supply	GND = 0 V		4.6	V
V _I	Input Voltage (V _{IN})	GND = 0 V	GND ≤ V _I ≤ V _{DD}	-0.5 V to V _{DD} +0.5 V	V
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-16 TSSOP-16	138 108	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 3)	TSSOP-16	33 to 36	°C/W
T _{sol}	Wave Solder			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
- JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS (V_{DD} = 3.3 V ±5%, GND = 0 V, T_A = -40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I _{DD}	Power Supply Current (Note 4)	65		95	mA
I _{DDOE}	Power Supply Current when OE is Set Low	35		65	mA
V _{IH}	Input HIGH Voltage (X1/CLK, Sel0, Sel1, and OE)	0.7 * V _{DD}		V _{DD} + 300	mV
V _{IL}	Input LOW Voltage (X1/CLK, Sel0, Sel1, and OE)	GND – 300		0.3* V _{DD}	mV
V _{OH}	Output HIGH Voltage (See Figure 4)	660	700	850	mV
V _{OL}	Output LOW Voltage (See Figure 4)	-150	0	150	mV
V _{cross}	Crossing Voltage Magnitude (Absolute)	250		400	mV
ΔV _{cross}	Change in Magnitude of V _{cross}			150	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- NB3N circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
- Measurement taken with outputs terminated with R_S = 33.2 Ω, R_L = 49.9 Ω, with load capacitance of 2 pF and current biasing resistor, R_{REF} from I_{REF} (Pin 9) to GND of 475 Ω. See Figure 3.

NB3N3002

Table 6. AC CHARACTERISTICS ($V_{DD} = 3.3\text{ V} \pm 5\%$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; Note 7)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{CLKIN}	Clock/Crystal Input Frequency		25		MHz
f_{CLKOUT}	Output Clock Frequency	25		200	MHz
θ_{NOISE}	Phase-Noise Performance	$f_{CLK} = 200\text{ MHz}/100\text{ MHz}$			dBc/Hz
		@ 100 Hz offset from carrier	-103/-109		
		@ 1 kHz offset from carrier	-118/-127.8		
		@ 10 kHz offset from carrier	-122/-136.2		
		@ 100 kHz offset from carrier	-130/-138.8		
		@ 1 MHz offset from carrier	-138/-138.2		
	@ 10 MHz offset from carrier	-149/-164			
$t_{jit(\phi)}$	RMS Phase Jitter (at 125 MHz @ 1 MHz – 40 MHz)		0.25	0.50	ps
t_{jitter} (TIE)	TIE RMS Jitter (Note 8)	$f_{CLK} = 200\text{ MHz}$	2.5		ps
	Cycle-to-Cycle RMS Jitter (Note 9)	$f_{CLK} = 200\text{ MHz}$	2	5	
	Cycle-to-Cycle Peak to Peak Jitter (Note 9)	$f_{CLK} = 200\text{ MHz}$	20	35	
	Period RMS Jitter (Note 9)	$f_{CLK} = 200\text{ MHz}$	1.5	3	
	Period Peak-to-Peak Jitter (Note 9)	$f_{CLK} = 200\text{ MHz}$	10	20	
OE	Output Enable/Disable Time			1.0	μs
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at cross point)	45	50	55	%
t_R	Output Risetime (Measured from 175 mV to 525 mV, Figure 4)	175	340	700	ps
t_F	Output Falltime (Measured from 525 mV to 175 mV, Figure 4)	175	340	700	ps
Δt_R	Output Risetime Variation (Single-Ended)			125	ps
Δt_F	Output Falltime Variation (Single-Ended)			125	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. NB3N circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.
7. Measurement taken from differential output on single-ended channel terminated with $R_S = 33.2\ \Omega$, $R_L = 49.9\ \Omega$, with load capacitance of 2 pF and current biasing resistor, R_{REF} from I_{REF} (Pin 9) to GND of 475 Ω . See Figures 3 and 4.
8. Sampled with 20000 cycles to capture jitter component down to 100 kHz.
9. Sampled with 20000 cycles.

Table 7. AC ELECTRICAL CHARACTERISTICS – PCI EXPRESS JITTER SPECIFICATIONS,

$V_{DD} = 3.3 V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Characteristic	Test Conditions	Min	Typ	Max	PCIe Industry Spec	Unit
Phase Jitter P-P (Notes 11 and 14)	T_J PCIe Gen1	$f = 100$ MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2)		6	21	86	ps
Phase Jitter RMS (Notes 11 and 14)	$t_{REFCLK_HF_RMS}$ (PCIe Gen 2)	$f = 100$ MHz, 25 MHz Crystal Input High Band: 1.5 MHz – Nyquist (clock frequency/2)		0.6	3	3.1	ps
Phase Jitter RMS (Notes 11 and 14)	$t_{REFCLK_LF_RMS}$ (PCIe Gen 2)	$f = 100$ MHz, 25 MHz Crystal Input Low Band: 10 kHz – 1.5 MHz		0.08	0.3	3	ps
Phase Jitter RMS (Notes 13 and 14)	t_{REFCLK_RMS} (PCIe Gen 3)	$f = 100$ MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2)		0.23	0.7	0.8	ps

10. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
11. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86 ps peak-to-peak for a sample size of 106 clock periods.
12. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1 ps RMS for $t_{REFCLK_HF_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK_LF_RMS}$ (Low Band).
13. RMS jitter after applying system transfer function for the common clock architecture.
14. This parameter is guaranteed by characterization. Not tested in production

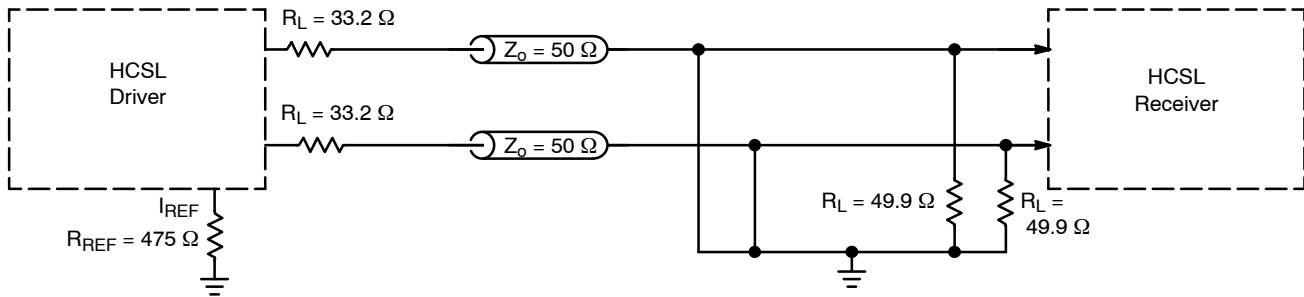


Figure 3. Typical Termination for Output Driver and Device Evaluation

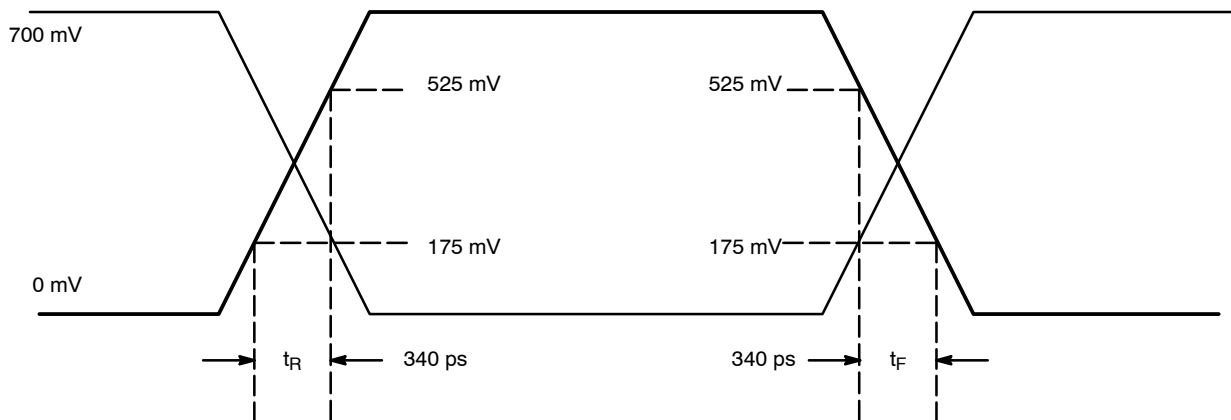


Figure 4. HCSL Output Parameter Characteristics

NB3N3002

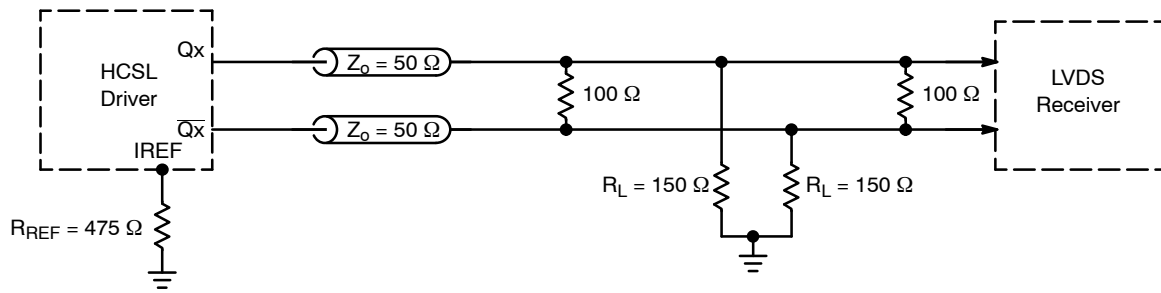


Figure 5. HCSL Interface Termination to LVDS

ORDERING INFORMATION

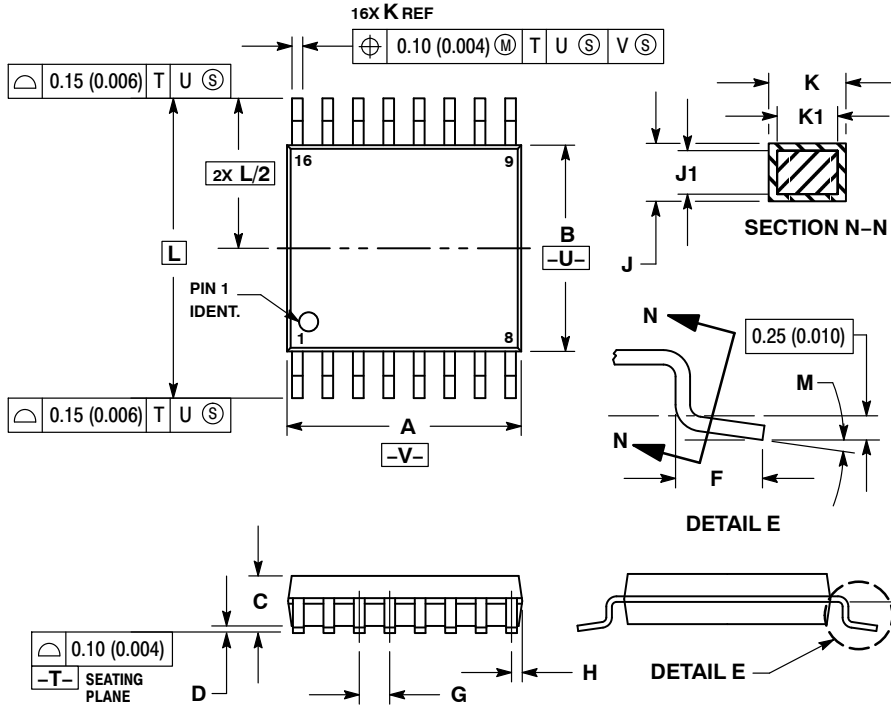
Device	Package	Shipping†
NB3N3002DTG	TSSOP-16 (Pb-Free)	96 Units / Rail
NB3N3002DTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB3N3002

PACKAGE DIMENSIONS

TSSOP-16
CASE 948F
ISSUE B

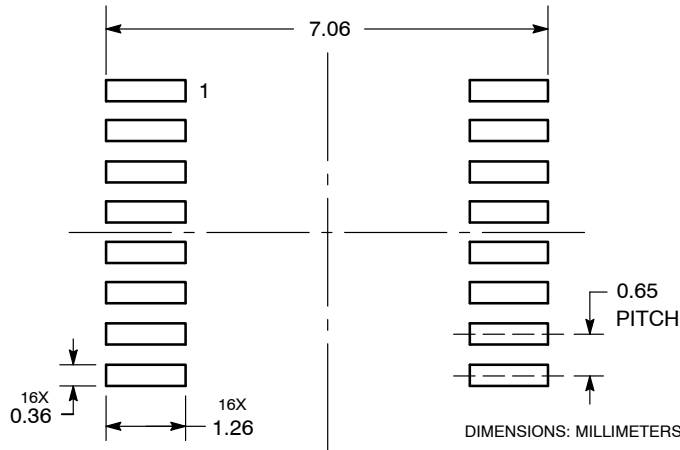


NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative