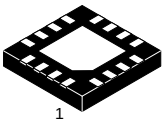
NB7VPQ702M

1.8 V USB 3.1 Dual Channel Re-driver

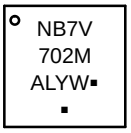
ON Semiconductor®

www.onsemi.com



UQFN16
CASE 523AF

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

Description

The NB7VPQ702M is a 1.8 V dual channel re−driver for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter−symbol interference (ISI). The NB7VPQ702M compensates for these losses by engaging varying levels of equalization at the input receiver. The output transmitter circuitry provides user selectable de−emphasis settings to create the best eye openings for the outgoing data signals.

The NB7VPQ702M features an intelligent LFPS circuit. This senses the low frequency signals and automatically disables driver de−emphasis to meet full USB 3.1 Gen 1 and USB 3.1 Gen 2 compliances.

After power up, the NB7VPQ702M periodically checks both of the TX output pairs for a receiver connection. When the receiver is detected the RX termination becomes enabled and the NB7VPQ702M is set to perform the re−driver function.

The NB7VPQ702M comes in a small 3 x 3 mm UQFN16 package and is specified to operate across the entire industrial temperature range, –40°C to 85°C.

Features

- 1.8 V ± 5% Power Supply
- Device Supports USB 3.1 Gen 1 and USB 3.1 Gen 2 Data Rates
- Automatic LFPS De−Emphasis Control
- Automatic Receiver Termination Detection
- Integrated Input and Output Termination
- Selectable Equalization and De−Emphasis
- Hot−Plug Capable
- ESD Protection ±4 kV HBM
- Operating Temperature Range: –40°C to 85°C
- Small 3 x 3 x 0.5 mm UQFN16 Package
- This is a Pb−Free Device

Typical Applications

- USB3.1 Type−C Signal Routing
- Mobile Phone and Tablet
- Computer and Laptop
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V.

ORDERING INFORMATION

Device	Package	Shipping†
NB7VPQ702MMUTXG	UQFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

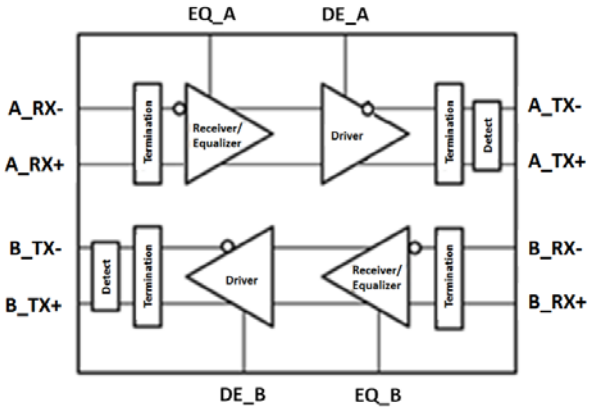


Figure 1. Logic Diagram of NB7VPQ702M

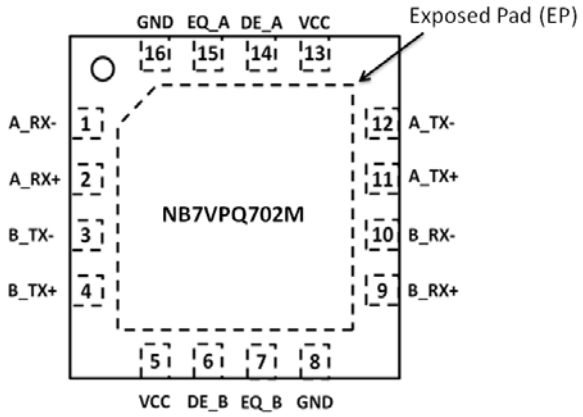


Figure 2. UQFN16 Package Pinout
(Top View)

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
1	A_RX-	DIFF IN	Channel A Differential input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
2	A_RX+		
3	B_TX−	DIFF OUT	Channel B Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
4	B_TX+		
5	VCC	Power	1.8−V power supply
6	DE_B	LVCMOS IN	Sets the output de−emphasis gain on Channel B. 3−state input with integrated 150 kΩ pull−up and pull−down resistors.
7	EQ_B	LVCMOS IN	Sets the receiver equalizer gain on Channel B. 3−state input with integrated 150 kΩ pull−up and pull−down resistors.
8	GND	GND	Reference Ground
9	B_RX+	DIFF IN	Channel B Differential input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
10	B_RX−		
11	A_TX+	DIFF OUT	Channel A Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
12	A_TX-		
13	VCC	Power	1.8−V power supply
14	DE_A	LVCMOS IN	Sets the output de−emphasis gain on Channel A. 3−state input with integrated 150 kΩ pull−up and pull−down resistors.
15	EQ_A	LVCMOS IN	Sets the receiver equalizer gain on Channel A. 3−state input with integrated 150 kΩ pull−up and pull−down resistors.
16	GND	GND	Reference Ground
EP	GND	GND	Exposed pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The pad is not electrically connected to the die, but is recommended to be soldered to GND on the PC Board.

DEVICE CONFIGURATION

Table 2. CONTROL PIN EFFECTS (Typical Values)

Pin	Description	Logic State	Equalization Gain
EQ	Equalization Amount	Low	3 dB
		Mid	6 dB
		High	9 dB
Pin	**Description**	**Logic State**	**De−emphasis Ratio** (Note 1)
DE	De−Emphasis Amount	Low	−1 dB
		Mid	−4.5 dB
		High	−6.5 dB

1. dB Decrease = 20 log * (V_{TX-DE} / $V_{TX-DIFF-PP}$)

Table 3. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	> 4 kV > 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−O @ 0.125 in
Transistor Count		1555
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. ABSOLUTE MAXIMUM RATINGS

Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 3)	V_{CC}	−0.3	2.5	V
Voltage range at any input or output terminal	Differential I/O	−0.5	1.89	V
	LVCMOS inputs	−0.3	V_{CC} + 0.3	V
Storage Temperature Range, T_{SG}		−65	150	°C
Maximum Junction Temperature, T_J			125	°C
Operating Ambient Temperature Range, T_A		−40	85	°C
Junction−to−Ambient Thermal Resistance @ 500 lfm, θ_{JA} (Note 4)			34	°C/W
Wave Solder, Pb−Free, T_{SOL}			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. All voltage values are with respect to the GND terminals.
4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. RECOMMENDED OPERATING CONDITIONS

Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Nom	Max	Unit
V_{CC}	Main power supply	1.71	1.8	1.89	V
T_A	Operating free−air temperature	−40		+85	°C
C_{AC}	AC coupling capacitor	75	100	200	nF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. POWER SUPPLY CHARACTERISTICS

Parameter		Test Conditions	Min	Typ (Note 5)	Max	Unit
I_{CC}	Active	Link in U0 with Super Speed Plus data transmission DE = low −1 dB, EQ = low 3 dB		140		mA
	Idle State	Link has some activity, not in U0 DE = mid −4.5 dB, EQ = mid 6dB		95		mA
	U2/U3	Link in U2 or U3 power saving state DE = mid −4.5 dB, EQ = mid 6 dB		8.9		mA
	No USB Connection	No connection state, termination disabled DE = mid −4.5 dB, EQ = mid 6 dB		8.9		mA

5. TYP values use V_{CC} = 1.8 V, T_A = 25°C.

Table 7. LVCMOS CONTROL PIN CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
3−State LVCMOS Inputs (EQ, DE)						
V_{IH}	High−level input voltage		0.8 * V_{CC}		V_{CC}	V
V_{IM}	Mid−level input voltage		0.4 * V_{CC}	V_{CC} / 2	0.6 * V_{CC}	V
V_{IL}	Low−level input voltage		GND		0.2 * V_{CC}	V
V_F	Floating voltage	V_{IN} = High impedance		V_{CC} / 2		V
R_{PU}	Internal pull−up resistance			150		kΩ
R_{PD}	Internal pull−down resistance			150		kΩ
I_{IH}	High−level input current	V_{IN} = 1.89 V			20	μA
I_{IL}	Low−level input current	V_{IN} = GND, V_{CC} = 1.89 V	−20			μA

Table 8. RECEIVER AC/DC CHARACTERISTICS Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{RX-DIFF-pp}$	Input differential voltage swing	AC−coupled, peak−to−peak	250		1200	mV_{PP}
V_{RX-CM}	Common−mode voltage bias in the receiver (DC)			V_{CC}− 0.25		V
$Z_{RX-DIFF}$	Differential input impedance (DC)	Present after an USB device is detected on TX+/TX−	80	100	120	Ω
Z_{RX-CM}	Common−mode input impedance (DC)	Present after an USB device is detected on TX+/TX−	20	25	30	Ω
$Z_{RX-HIGH-IMP}$	Common−mode input impedance with termination disabled (DC)	Present when no USB device is detected on TX+	25	115		kΩ
$V_{TH-LFPS-pp}$	Low Frequency Periodic Signaling (LFPS) Detect Threshold	Output voltage is considered squelched below this threshold voltage.			300	mV_{PP}

Table 9. TRANSMITTER AC/DC CHARACTERISTICS Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Output differential voltage swing	50 Ω to V_{CC}, DE = Low −1 dB, EQ = Low 3 dB		1000		mV_{PP}
C_{TX}	TX input capacitance to GND	At 2.5 GHz		1.25		pF
$Z_{TX-DIFF}$	Differential output impedance (DC)	Present after an USB device is detected on TX+/TX−	80	100	120	Ω
Z_{TX-CM}	Common−mode output impedance (DC)	Present after an USB device is detected on TX+/TX−	20		30	Ω
I_{TX-SC}	TX short circuit current	TX+ or TX− shorted to GND		35		mA
V_{TX-CM}	Common−mode voltage bias in the transmitter (DC)			V_{CC}−0.6	V_{CC}	V
$V_{TX-CM-ACpp}$	AC common−mode peak−to−peak voltage swing in active mode	Within U0 and within LFPS			100	mV_{PP}
$V_{TX-IDLE-DIFF-ACpp}$	Differential voltage swing during electrical idle	Tested with a high−pass filter	0		10	mV_{PP}
$V_{TX-RXDET}$	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t_R, t_F	Output rise, fall time	20% − 80% of differential voltage measured 1 inch from the output pin		45		ps
t_{RF-MM}	Output rise, Fall time mismatch	20% − 80% of differential voltage measured 1 inch from the output pin			5	ps
$t_{diff-LH}$, $t_{diff-HL}$	Differential propagation delay	De−emphasis = −4.5 dB propagation delay between 50% level at input and output		150		ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times			30		ns

Table 10. TIMING AND JITTER CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
TIMING						
t_{READY}	Time from power applied until RX termination is enabled	Apply 0 V to V_{CC}, connect USB termination to TX±, apply 1.8 V to V_{CC}, and measure when $Z_{RX-DIFF}$ is enabled		10		ms
JITTER FOR 5 Gbps						
$T_{JTX-EYE}$	Total jitter (Notes 6, 7)	EQ = Low 3 dB, DE = Low −1 dB		0.045		UI (Note 8)
D_{JTX}	Deterministic jitter (Note 7)			0.011		UI (Note 8)
R_{JTX}	Random jitter (Note 7)			0.005		UI (Note 8)
JITTER FOR 10 Gbps						
$T_{JTX-EYE}$	Total jitter (Notes 6, 7)	EQ = Low 3 dB, DE = Low −1 dB		0.118		UI (Note 8)
D_{JTX}	Deterministic jitter (Note 7)			0.053		UI (Note 8)
R_{JTX}	Random jitter (Note 7)			0.010		UI (Note 8)

6. Includes RJ at 10^{-12}.
7. Measured at the ends of reference channel with a K28.5 pattern, VID = 1000 mVpp, −3.5 dB de−emphasis from source.
8. 5 Gbps, UI = 200 ps for 10 Gbps, UI = 100 ps

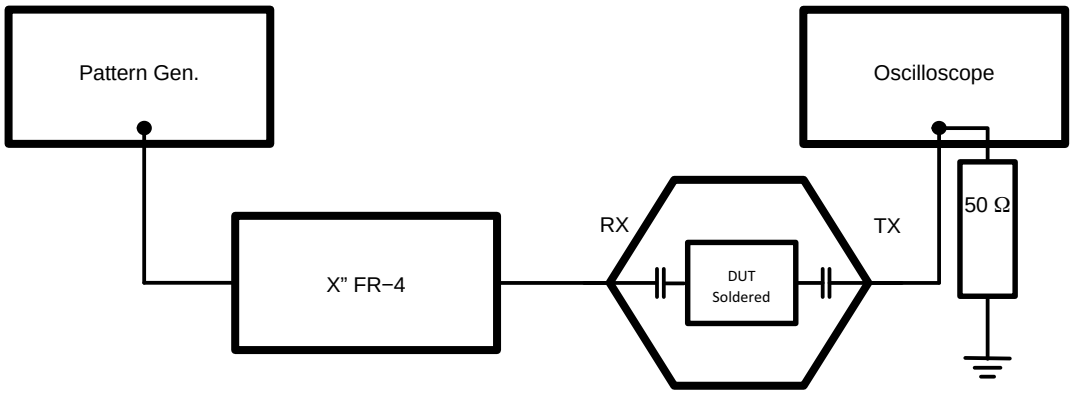


Figure 3. Equalization Measurement Setup

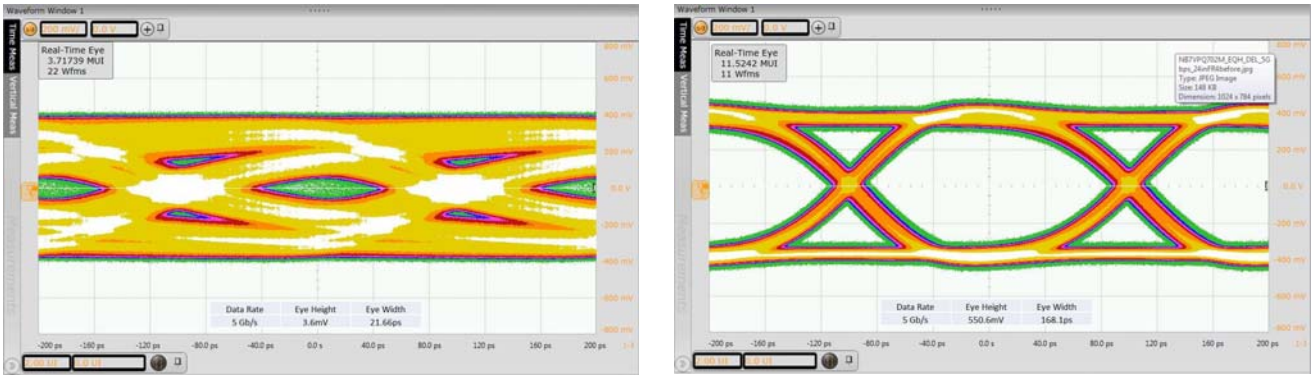


Figure 4. 5 Gbps Signal with 24 inches of FR4 Before Input to NB7VPQ702M and After Using High EQ Setting

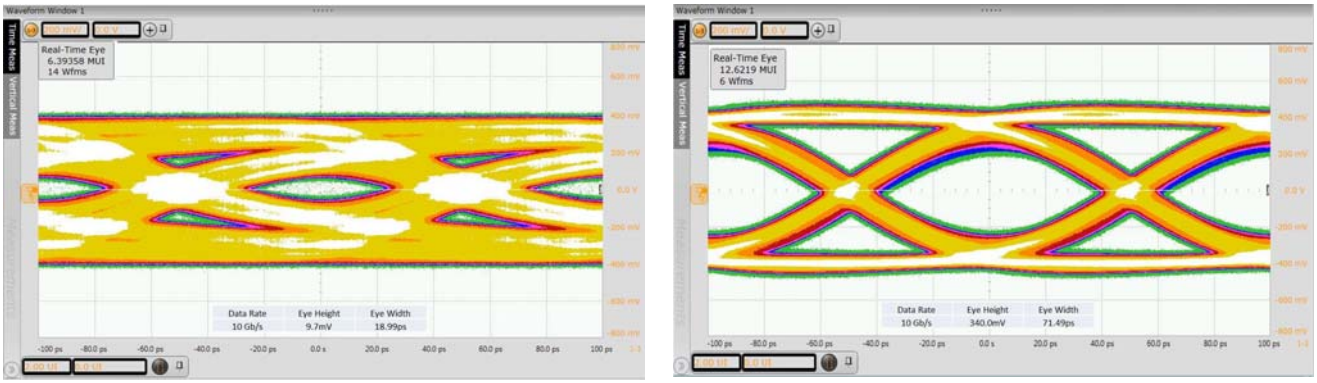


Figure 5. 10 Gbps Signal with 12 inches of FR4 Before Input to NB7VPQ702M and After with EQ Floating (Mid)

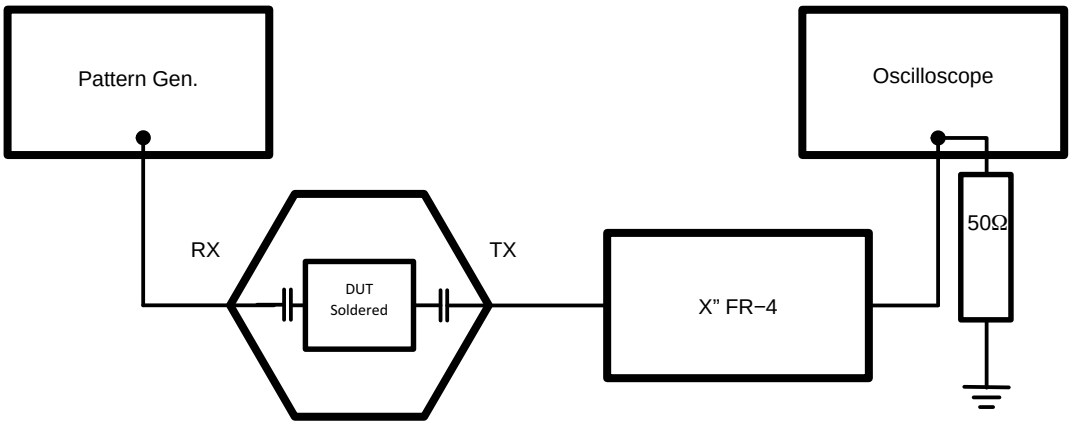


Figure 6. De−Emphasis Measurement Setup

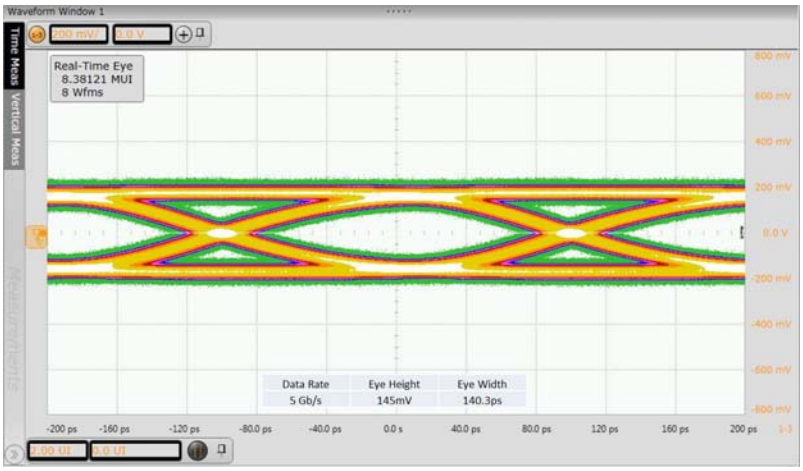


Figure 7. 5 Gbps Signal After 24 inches of FR4 at Output with High DE Setting to NB7VPQ702M

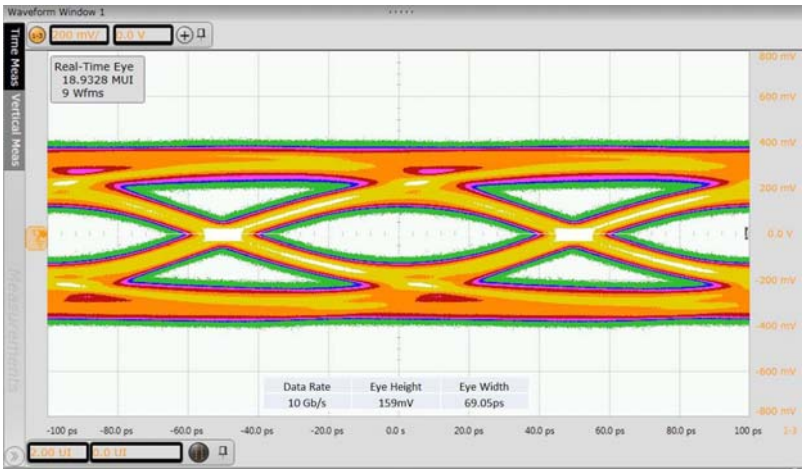


Figure 8. 10 Gbps Signal After 9 inches of FR4 at Output with Low DE Setting to NB7VPQ702M

PARAMETER MEASUREMENT DIAGRAMS

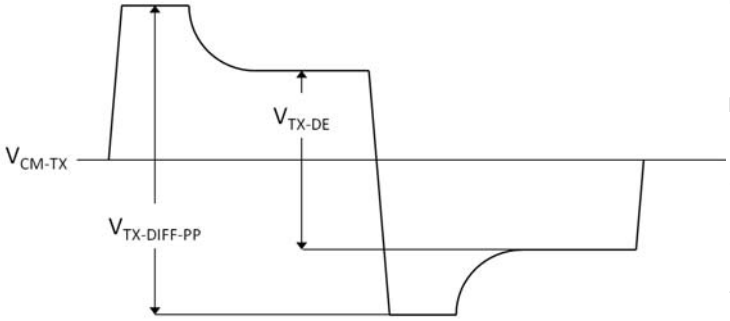


Figure 9. Transmitter Differential Voltage
dB Decrease = 20 log * (V_{TX-DE} / $V_{TX-DIFF-PP}$)

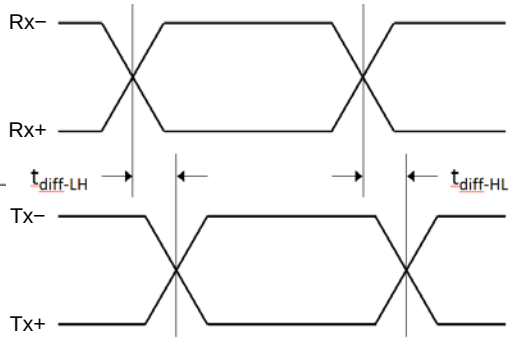


Figure 10. Propagation Delay

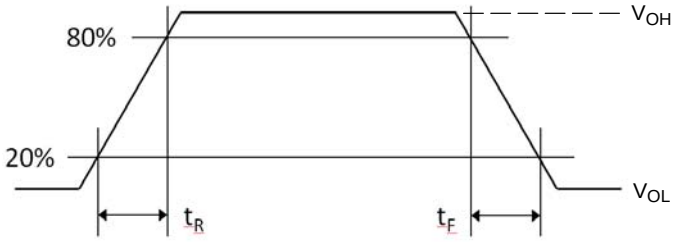


Figure 11. Output Rise and Fall Times

APPLICATION GUIDELINES

LFPS Compliance Testing

As part of USB 3.1 compliance test, the host or peripheral must transmit a LFPS signal that adheres to the spec parameters. When using a real−time oscilloscope to capture this data, *the scope's trigger must be below 0 V when making single−ended measurements*. Although the differential signal is identical to that which is expected by the USB 3.1 system, the AC common mode voltage for LFPS may fall below 0 V during short bursts of switching signal, which is still within the spec's limit.

LFPS Functionality

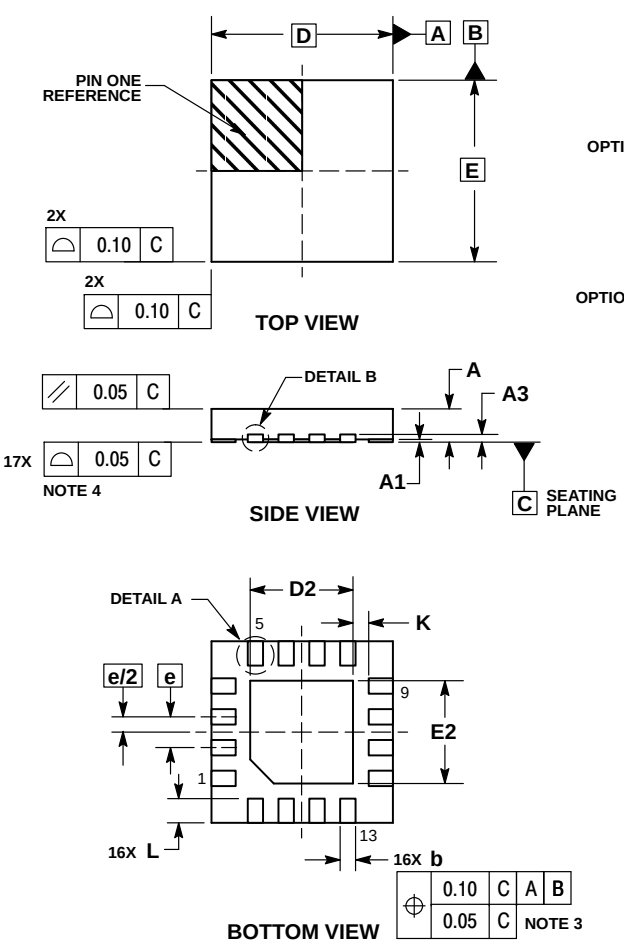
USB 3.1 links use Low Frequency Periodic Signaling (LFPS) to implement functions like exiting low−power modes, performing warm resets and providing link training between host and peripheral devices. LFPS signaling consists of bursts of frequencies ranging between 10 to 50 MHz and can have specific burst lengths or repeat rates.

Ping.LFPS for TX Compliance

During the transmitter compliance, the system under test must transmit certain compliance patterns as defined by the USB−IF. In order to toggle through these patterns for various tests, the receiver must receive a ping. LFPS signal from either the test suite or a separate pattern generator. The standard signal comprises of a single burst period of 100ns at 20 MHz. In order to pass this signal through NB7VPQ702M, *the duration of the burst must be extended to at least 200 ns.*

PACKAGE DIMENSIONS

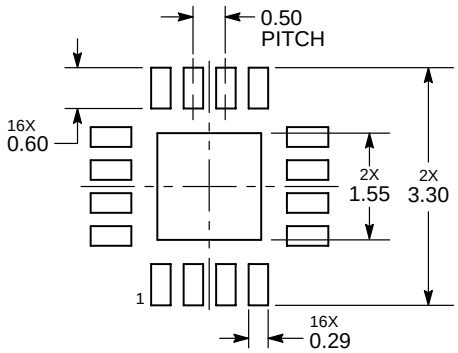
UQFN16 3x3, 0.5P
CASE 523AF
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	–––
L	0.30	0.50

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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