



July 2001
Revised April 2003

NC7NZ34 TinyLogic® UHS Triple Buffer

General Description

The NC7NZ34 is a triple buffer from Fairchild's Ultra High Speed Series of TinyLogic® in the space saving US8 package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

Features

- Space saving US8 surface mount package
- MicroPak™ leadless package
- Ultra High Speed: t_{PD} 2.4 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive: ± 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

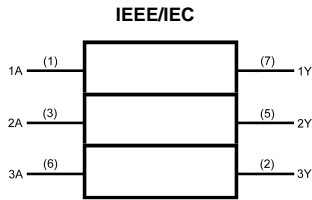
Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7NZ34K8X	MAB08A	7NZ34	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7NZ34L8X (Preliminary)	MAC08A	P9	8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

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MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

NC7NZ34 TinyLogic® UHS Triple Buffer

Logic Symbol



Pin Descriptions

Pin Names	Description
A ₁ , A ₂ , A ₃	Data Inputs
Y ₁ , Y ₂ , Y ₃	Output

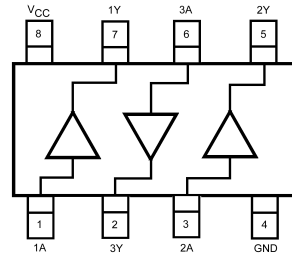
Function Table

$Y = A$

Input	Output
A	Y
L	L
H	H

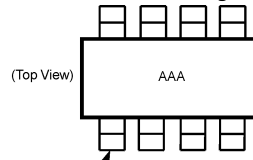
H = HIGH Logic Level
L = LOW Logic Level

Connection Diagrams



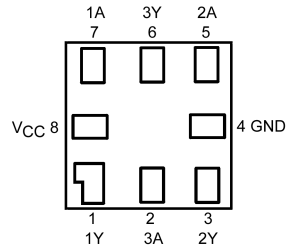
(Top View)

Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code
Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Thru View)

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 2)	
Supply Voltage (V_{CC})	-0.5V to +7.0V	Supply Voltage	1.65V to 5.5V
DC Input Voltage (V_{IN})	-0.5V to +7.0V	Operating (V_{CC})	1.5V to 5.5V
DC Output Voltage (V_{OUT})	-0.5V to +7.0V	Data Retention	1.5V to 5.5V
DC Input Diode Current (I_{IK})		Input Voltage (V_{IN})	0V to 5.5V
$V_{IN} < 0V$	-50 mA	Output Voltage (V_{OUT})	0V to V_{CC}
DC Output Diode Current (I_{OK})		Input Rise and Fall Time (t_r, t_f)	
$V_{OUT} < 0V$	-50 mA	$V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 to 20 ns/V
DC Output Source/Sink Current (I_{OUT})	± 50 mA	$V_{CC} = 3.3V \pm 0.3V$	0 to 10 ns/V
DC V_{CC}/GND Current (I_{CC}/I_{GND})	± 100 mA	$V_{CC} = 5.5V \pm 0.5V$	0 to 5 ns/V
Storage Temperature (T_{STG})	-65°C to +150°C	Operating Temperature (T_A)	-40°C to +85°C
Junction Temperature under Bias (T_J)	150°C	Thermal Resistance (θ_{JA})	250°C/W
Junction Lead Temperature (T_L)		Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.	
(Soldering, 10 seconds)	260°C	Note 2: Unused inputs must be held HIGH or LOW. They may not float.	
Power Dissipation (P_D) @ +85°C	250 mW		

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Control Input Voltage	1.8 ± 0.15	0.75 V_{CC}			0.75 V_{CC}		V		
		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Control Input Voltage	1.8 ± 0.15	0.25 V_{CC}			0.25 V_{CC}		V		
		2.3 to 5.5	0.3 V_{CC}			0.3 V_{CC}				
V_{OH}	HIGH Level Control Output Voltage	1.65	1.55	1.65	1.55		V	$V_{IN} = V_{IH}$	$I_{OH} = -100 \mu A$	
		2.3	2.2	2.3	2.2					
		3.0	2.9	3.0	2.9					
		4.5	4.4	4.5	4.4					
		1.65	1.29	1.52	1.29					
		2.3	1.9	2.14	1.9					
		3.0	2.4	2.75	2.4					
		3.0	2.3	2.62	2.3					
		4.5	3.8	4.13	3.8					
		V_{OL}	LOW Level Control Output Voltage	1.65	0.0				0.1	
2.3	0.0			0.1						
3.0	0.0			0.1						
4.5	0.0			0.1						
1.65	0.08			0.24						
2.3	0.10			0.3						
3.0	0.16			0.4						
3.0	0.24			0.55						
4.5	0.25			0.55						
I_{IN}	Input Leakage Current			0 to 5.5				± 0.1		μA
I_{OFF}	Power Off Leakage Current	0.0				1.0		μA	V_{IN} or $V_{OUT} = 5.5V$	
I_{CC}	Quiescent Supply Current	1.65 to 5.5				1.0		μA	$V_{IN} = 5.5V, GND$	

AC Electrical Characteristics

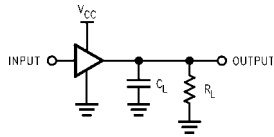
Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t _{PLH}	Propagation Delay	1.8 ± 0.15	1.8	4.6	8.0	1.8	8.8	ns	C _L = 15 pF, R _L = 1 MΩ	Figures 1, 3
t _{PHL}		2.5 ± 0.2	1.0	3.0	5.2	1.0	5.8			
		3.3 ± 0.3	0.8	2.3	3.6	0.8	4.0			
		5.0 ± 0.5	0.5	1.8	2.9	0.5	3.2			
t _{PLH}	Propagation Delay	3.3 ± 0.3	1.2	3.0	4.6	1.2	5.1	ns	C _L = 50 pF, R _L = 500Ω	Figures 1, 3
t _{PHL}		5.0 ± 0.5	0.8	2.4	3.8	0.8	4.2			
C _{IN}	Input Capacitance	0	2.5					pF		
C _{PD}	Power Dissipation	3.3	9					pF	(Note 3)	Figure 2
	Capacitance	5.0	11							

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static).

Dynamic Switching Characteristics

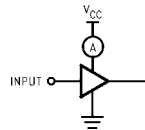
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Unit
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50pF, V _{IH} = 5.0V, V _{IL} = 0V	5.0	0.8	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50pF, V _{IH} = 5.0V, V _{IL} = 0V	5.0	-0.8	V

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; t_r = t_f = 1.8 ns;
PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

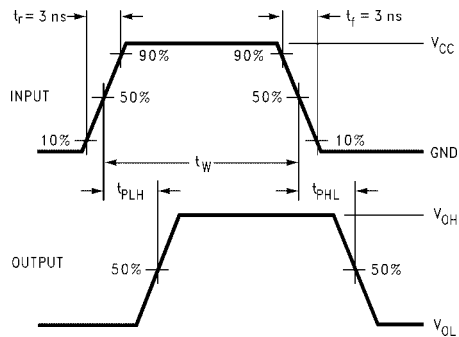


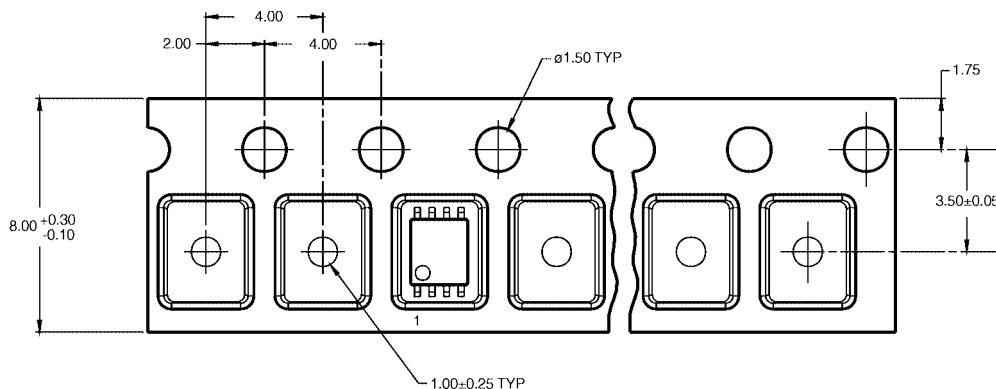
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

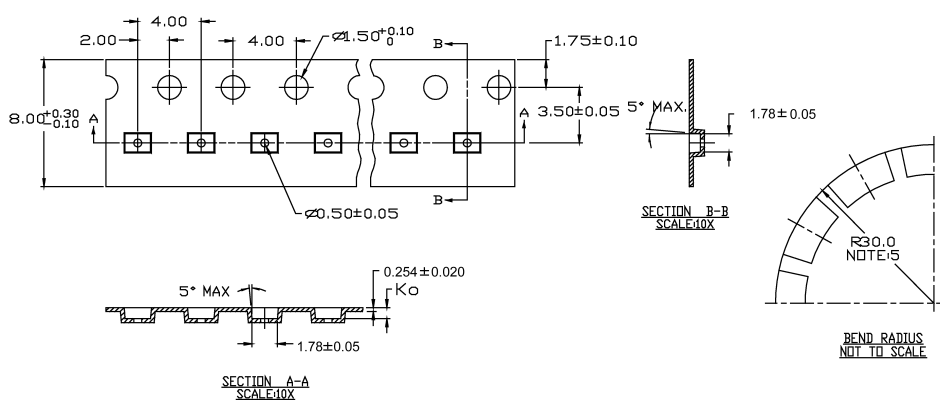
TAPE DIMENSIONS inches (millimeters)



TAPE FORMAT for MicroPak

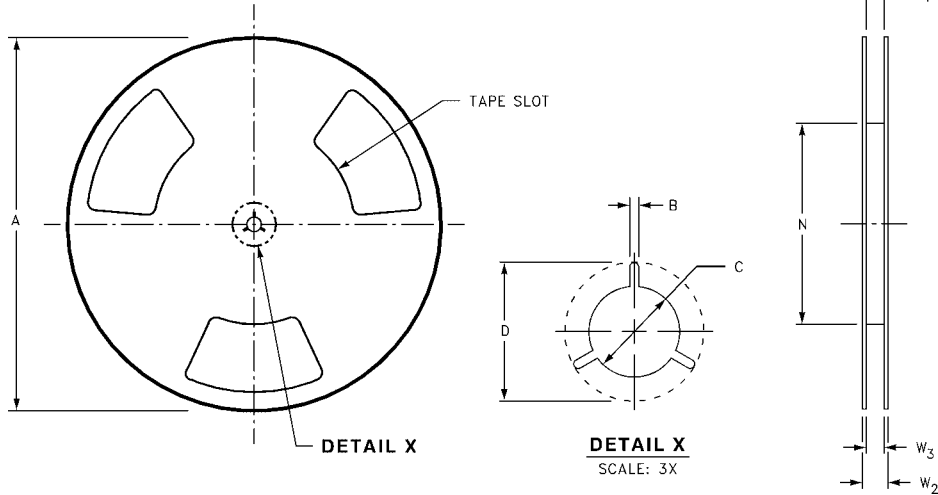
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



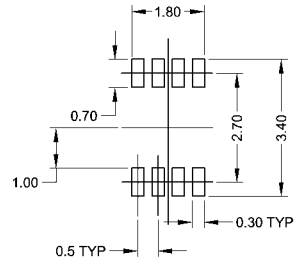
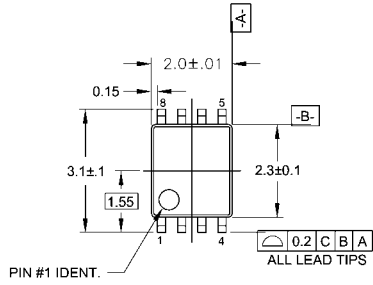
NC7NZ34

Tape and Reel Specification (Continued)
REEL DIMENSIONS inches (millimeters)

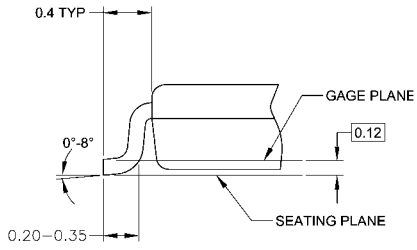
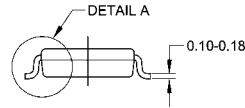
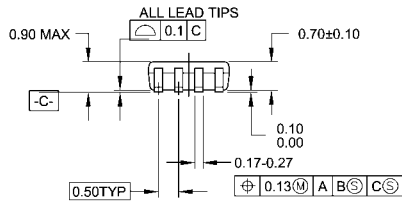


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	$0.331 + 0.059/-0.000$ ($8.40 + 1.50/-0.00$)	0.567 (14.40)	$W1 + 0.078/-0.039$ ($W1 + 2.00/-1.00$)

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



DETAIL A

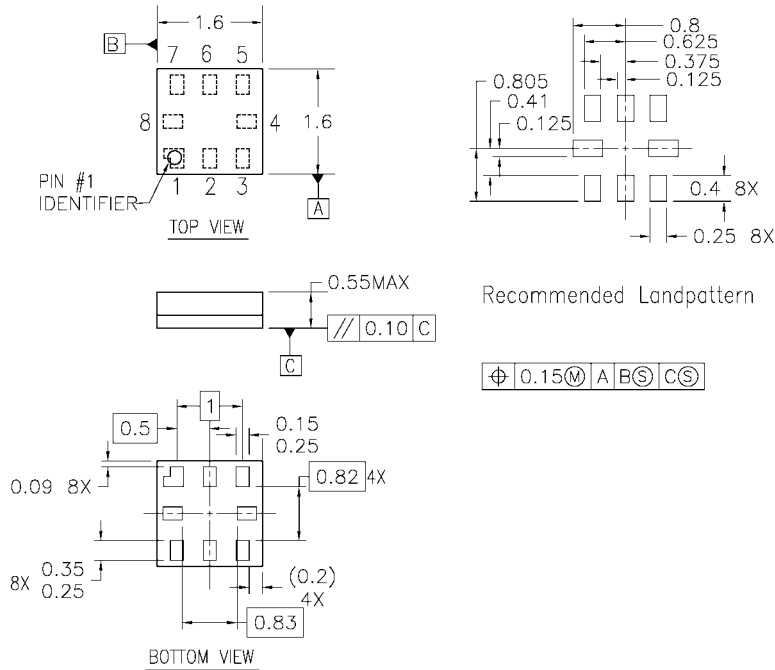
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. PACKAGE REGISTRATION WITH JEDEC IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994

MAC08AREVB

**8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A
(Preliminary)**

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