# TinyLogic HS 2-Input NAND Gate

# NC7S00

## Description

The NC7S00 is a single 2−Input high performance CMOS NAND Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad $V_{CC}$ range. ESD protection diodes inherently guard both inputs and output with respect to the $V_{CC}$ and GND rails. Three stages of gain between inputs and output assures high noise immunity and reduced sensitivity to input edge rate.

## Features

- Space Saving SOT23−5, SC−74A and SC−88A 5−Lead Packages
- Ultra Small MicroPak™ Leadless Package
- High Speed: $t_{PD}$ = 3.5 ns Typ
- Low Quiescent Power: $I_{CC}$ < 1 μA
- Balanced Output Drive: 2 mA $I_{OL}$, −2 mA $I_{OH}$
- Broad $V_{CC}$ Operating Range: 2 V – 6 V
- Balanced Propagation Delays
- Specified for 3 V Operation
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

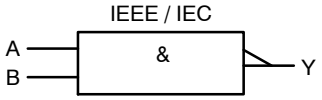
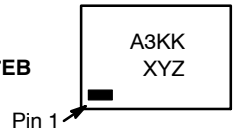
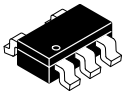



**Figure 1. Logic Symbol**

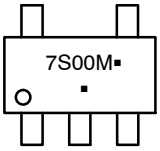
## MARKING DIAGRAMS

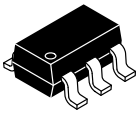
**SIP6**
**CASE 127EB**



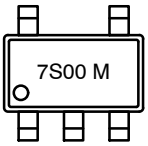



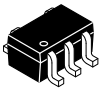
**SC−74A**
**CASE 318BQ**



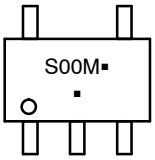



**SOT23−5**
**CASE 527AH**



**SC−88A**
**CASE 419A−02**




| | |
|---|---|
| A3, 7S00, S00 | = Specific Device Code |
| KK | = 2−Digit Lot Run Traceability Code |
| XY | = 2−Digit Date Code Format |
| Z | = Assembly Plant Code |
| M | = Date Code* |

*Date Code orientation and/or position may vary depending upon manufacturing location.

## ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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## Pin Configurations

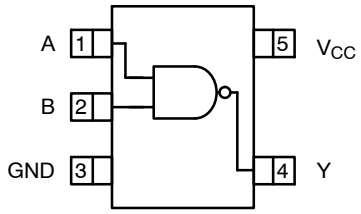



**Figure 2. SOT23−5, SC−88A and SC−74A (Top View)**

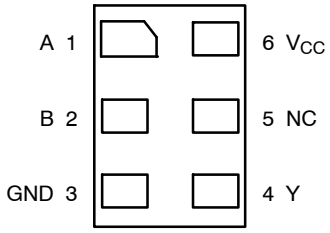



**Figure 3. MicroPak (Top Through View)**

### PIN DESCRIPTIONS

| Pin Names | Description |
|---|---|
| A, B | Inputs |
| Y | Output |
| NC | No Connect |

### FUNCTION TABLE ($Y = \overline{AB}$)

| Inputs | | Output |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH Logic Level
L = LOW Logic Level

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | −0.5 | 6.5 | V |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < 0 V | − | −20 | mA |
| | | $V_{IN}$ > $V_{CC}$ | − | +20 | |
| $V_{IN}$ | DC Input Voltage | | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < 0 V | − | −20 | mA |
| | | $V_{OUT}$ > $V_{CC}$ | − | +20 | |
| $V_{OUT}$ | DC Output Voltage | | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{OUT}$ | DC Output Source or Sink Current | | − | ±12.5 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current per Output Pin | | − | ±25 | mA |
| $T_{STG}$ | Storage Temperature | | −65 | +150 | °C |
| $T_J$ | Junction Temperature | | − | +150 | °C |
| $T_L$ | Lead Temperature (Soldering, 10 Seconds) | | − | +260 | °C |
| $P_D$ | Power Dissipation in Still Air | SC−74A / SOT23−5 | − | 390 | mW |
| | | SC−88A | − | 332 | |
| | | MicroPak−6 | − | 812 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 2.0 | 6.0 | V |
| $V_{IN}$ | Input Voltage | | 0 | $V_{CC}$ | V |
| $V_{OUT}$ | Output Voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature | | −40 | +85 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Times | $V_{CC}$ at 2.0 V | 0 | 20 | ns/V |
| | | $V_{CC}$ at 3.0 V | 0 | 20 | |
| | | $V_{CC}$ at 4.5 V | 0 | 10 | |
| | | $V_{CC}$ at 6.0 V | 0 | 5 | |
| $\theta_{JA}$ | Thermal Resistance | SC−74A / SOT23−5 | – | 320 | °C/W |
| | | SC−88A | – | 377 | |
| | | MicroPak−6 | – | 154 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC ELECTICAL CHARACTERISTICS

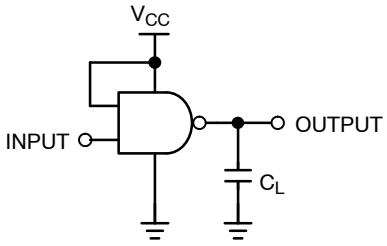
| Symbol | Parameter | $V_{CC}$ (V) | Conditions | | $T_A$ = +25°C | | | $T_A$ = −40 to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | 2.0 | | | 1.50 | – | – | 1.50 | – | V |
| | | 3.0 – 6.0 | | | 0.7 x $V_{CC}$ | – | – | 0.7 x $V_{CC}$ | – | |
| $V_{IL}$ | LOW Level Input Voltage | 2.0 | | | – | – | 0.50 | – | 0.50 | V |
| | | 3.0 – 6.0 | | | – | – | 0.3 x $V_{CC}$ | – | 0.3 x $V_{CC}$ | |
| $V_{OH}$ | HIGH Level Output Voltage | 2.0 | $I_{OH}$ = −20 μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 1.90 | 2.0 | – | 1.90 | – | V |
| | | 3.0 | | | 2.90 | 3.0 | – | 2.90 | – | |
| | | 4.5 | | | 4.40 | 4.5 | – | 4.40 | – | |
| | | 6.0 | | | 5.90 | 6.0 | – | 5.90 | – | |
| | | 3.0 | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −1.3 mA | 2.68 | 2.85 | – | 2.63 | – | |
| | | 4.5 | | $I_{OH}$ = −2 mA | 4.18 | 4.35 | – | 4.13 | – | |
| | | 6.0 | | $I_{OH}$ = −2.6 mA | 5.68 | 5.85 | – | 5.63 | – | |
| $V_{OL}$ | LOW Level Output Voltage | 2.0 | $I_{OL}$ = 20 μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | – | 0.0 | 0.10 | – | 0.10 | V |
| | | 3.0 | | | – | 0.0 | 0.10 | – | 0.10 | |
| | | 4.5 | | | – | 0.0 | 0.10 | – | 0.10 | |
| | | 6.0 | | | – | 0.0 | 0.10 | – | 0.10 | |
| | | 3.0 | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = 1.3 mA | – | 0.1 | 0.26 | – | 0.33 | |
| | | 4.5 | | $I_{OL}$ = 2 mA | – | 0.1 | 0.26 | – | 0.33 | |
| | | 6.0 | | $I_{OL}$ = 2.6 mA | – | 0.1 | 0.26 | – | 0.33 | |
| $I_{IN}$ | Input Leakage Current | 6.0 | $V_{IN}$ = $V_{CC}$, GND | | – | – | ±0.1 | – | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | 6.0 | $V_{IN}$ = $V_{CC}$, GND | | – | – | 1.0 | – | 10.0 | μA |

## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = +25°C | | | $T_A$ = −40 to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay (Figure 4, 6) | 5.0 | $C_L$ = 15 pF | – | 3.5 | 15 | – | – | ns |
| | | 2.0 | $C_L$ = 50 pF | – | 19 | 100 | – | 125 | |
| | | 3.0 | | – | 10.5 | 27 | – | 35 | |
| | | 4.5 | | – | 7.5 | 20 | – | 25 | |
| | | 6.0 | | – | 6.5 | 17 | – | 21 | |
| $t_{TLH}$, $t_{THL}$ | Output Transition Time (Figure 4, 6) | 5.0 | $C_L$ = 15 pF | – | 3.0 | 10 | – | – | ns |
| | | 2.0 | $C_L$ = 50 pF | – | 25 | 125 | – | 155 | |
| | | 3.0 | | – | 16 | 35 | – | 45 | |
| | | 4.5 | | – | 11 | 25 | – | 31 | |
| | | 6.0 | | – | 9 | 21 | – | 26 | |
| $C_{IN}$ | Input Capacitance | Open | | – | 2 | 10 | – | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Figure 5) | 5.0 | (Note 2) | – | 6 | – | – | – | pF |

2. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading and operating at 50% duty cycle. $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

### AC Loading and Waveforms




$C_L$ includes load and stray capacitance
Input PRR = 1.0 MHz, $t_W$ = 500 ns

**Figure 4. AC Test Circuit**

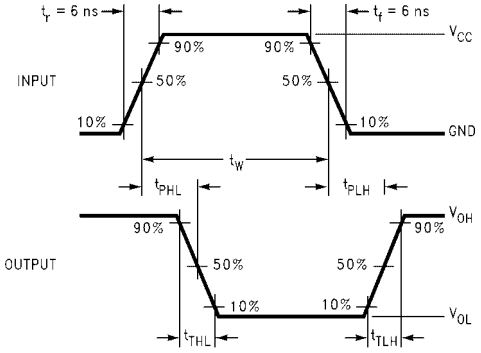
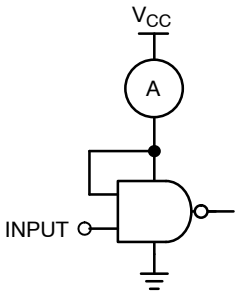



**Figure 6. AC Waveforms**




Input = AC Waveform;
PRR = Variable; Duty Cycle = 50%.

**Figure 5. $I_{CCD}$ Test Circuit**

## DEVICE ORDERING INFORMATION

| Device | Top Mark | Packages | Shipping† |
|---|---|---|---|
| NC7S00M5X | 7S00 | SC−74A | 3000 / Tape & Reel |
| NC7S00M5X−L22090 | 7S00 | SOT23−5 | 3000 / Tape & Reel |
| NC7S00P5X | S00 | SC−88A | 3000 / Tape & Reel |
| NC7S00P5X−L22057 | S00 | SC−88A | 3000 / Tape & Reel |
| NC7S00L6X | A3 | SIP6, MicroPak | 5000 / Tape & Reel |
| NC7S00L6X−L22175 | A3 | SIP6, MicroPak | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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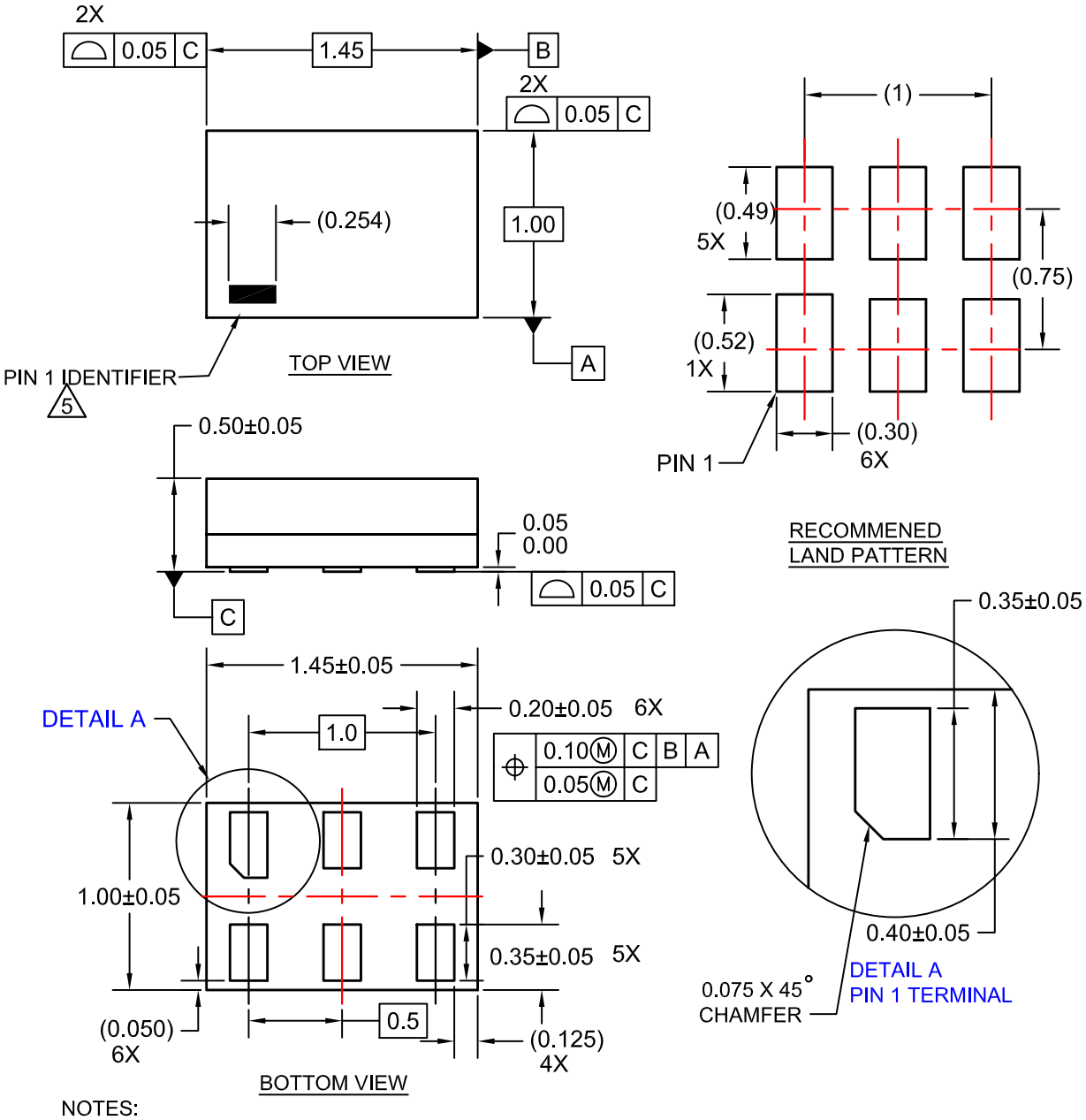
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

**SIP6 1.45X1.0**
CASE 127EB
ISSUE O

DATE 31 AUG 2016




NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON13590G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SIP6 1.45X1.0** | **PAGE 1 OF 1** |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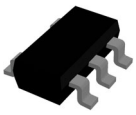
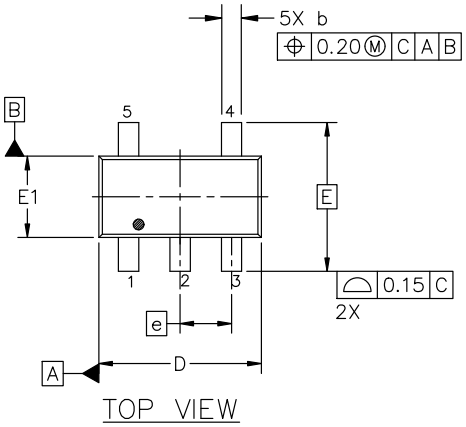
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

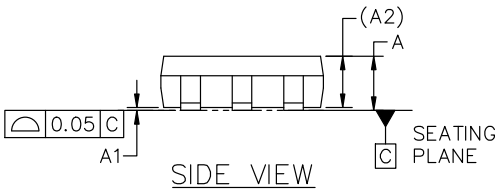


**SC−74A−5 3.00x1.50x0.95, 0.95P**
CASE 318BQ
ISSUE C

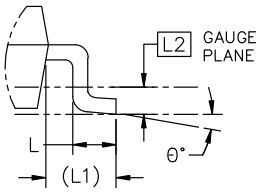
DATE 26 FEB 2024



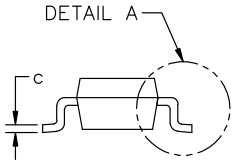

TOP VIEW




SIDE VIEW




DETAIL "A"
SCALE 2:1

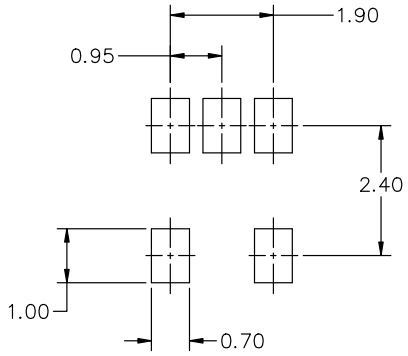



END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

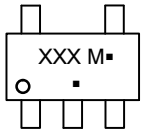
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.01 | 0.18 | 0.10 |
| A2 | | 0.95 REF. | |
| b | 0.25 | 0.37 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.85 | 3.00 | 3.15 |
| E | | 2.75 BSC | |
| E1 | 1.35 | 1.50 | 1.65 |
| e | | 0.95 BSC | |
| L | 0.20 | 0.40 | 0.60 |
| L1 | | 0.62 REF. | |
| L2 | | 0.25 BSC | |
| θ | 0° | 5° | 10° |




RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

| DOCUMENT NUMBER: | 98AON66279G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | SC−74A−5 3.00x1.50x0.95, 0.95P | PAGE 1 OF 1 |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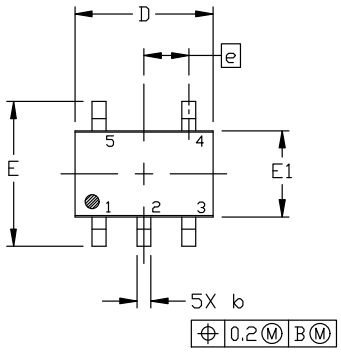
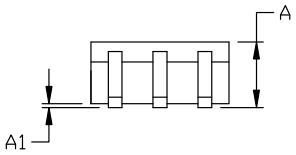
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

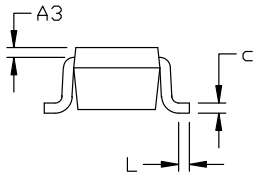
**SCALE 2:1**

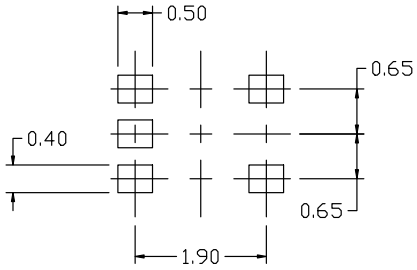
**SC−88A (SC−70−5/SOT−353)**
CASE 419A−02
ISSUE M

DATE 11 APR 2023




RECOMMENDED
MOUNTING FOOTPRINT

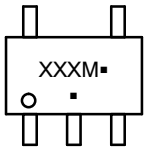
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.95 | 1.10 |
| A1 | --- | --- | 0.10 |
| A3 | 0.20 REF | | |
| b | 0.10 | 0.20 | 0.30 |
| c | 0.10 | --- | 0.25 |
| D | 1.80 | 2.00 | 2.20 |
| E | 2.00 | 2.10 | 2.20 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.10 | 0.15 | 0.30 |

### GENERIC MARKING DIAGRAM*




*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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| DESCRIPTION: | SC−88A (SC−70−5/SOT−353) | PAGE 1 OF 1 |

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# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

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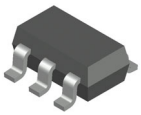
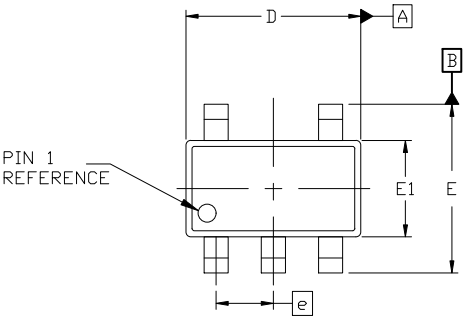
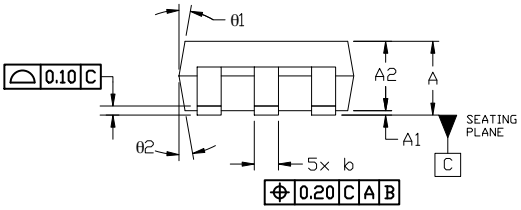


**SOT−23, 5 Lead**
CASE 527AH
ISSUE A

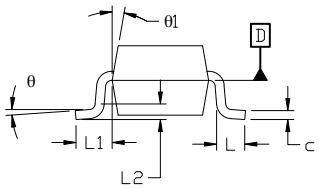
DATE 09 JUN 2021




TOP VIEW



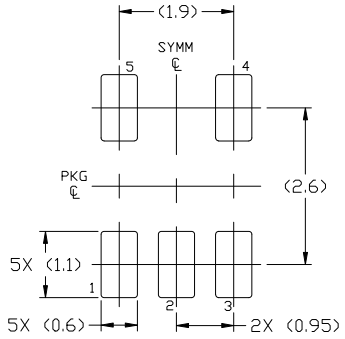

SIDE VIEW




END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

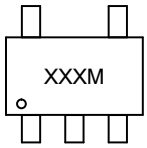
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 0.90 | — | 1.45 |
| A1 | 0.00 | — | 0.15 |
| A2 | 0.90 | 1.15 | 1.30 |
| b | 0.30 | — | 0.50 |
| c | 0.08 | — | 0.22 |
| D | 2.90 BSC | | |
| E | 2.80 BSC | | |
| E1 | 1.60 BSC | | |
| e | 0.95 BSC | | |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.60 REF | | |
| L2 | 0.25 REF | | |
| θ | 0° | 4° | 8° |
| θ1 | 0° | 10° | 15° |
| θ2 | 0° | 10° | 15° |




**RECOMMENDED MOUNTING FOOTPRINT**

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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