NCA1021S

LIN transceiver with multiple modes

Datasheet (EN) 1.1

Product Overview

The NCA1021S is a LIN (Local Interconnect Network) transceiver with a low-power mode and multiple wake-up methods. It supports up to 20 kbps for sending and receiving communication and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602 and ISO 17987-4: 2016 (12V LIN systems).

In sleep mode, the power consumption of NCA1021S is extremely low. Support remote wake-up and local wake-up via LIN bus, pin WAKE_N and pin SLP_N. The device can also use the INH output pin as a sign to control the working state of other devices in the local system, such as the voltage regulator, to achieve low power operation of the system.

The NCA1021S converts the signal received by TXD into a LIN bus signal through waveform shaping and slew rate adjustment to reduce electromagnetic emission (EME). TXD has a fault time-out protection function to prevent the LIN bus from being occupied.

Key Features

- Compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602 and ISO 17987–4 standard
- Very low electromagnetic emission (EME)
- High electromagnetic immunity (EMI)
- Support for 12 V applications
- Input levels compatible with 3.3 V and 5 V devices
- Bus fault protection of -40 V to +40 V
- Wake-up source recognition (local or remote)
- Integrated LIN pull-up resistor
- Transmit data (TXD) dominant time-out function
- K-line compatible
- AEC-Q100 qualified for automotive applications (Grade 1)
- Over temperature protection
- Date rate: up to 20 kbps
- Operation temperature range: -40 ℃~125 ℃
- RoHS compliance
- Available packages:

  SOP8

  DFN8

Applications

- Body sensor and module control
- Car steering wheel and instrument cluster
- Powertrain system and electric engine

Device Information

Part Number	*Package*	*Body Size*
NCA1021S-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1021S-Q1DNR	DFN8	3.00mm × 3.00mm

Function Block Diagram

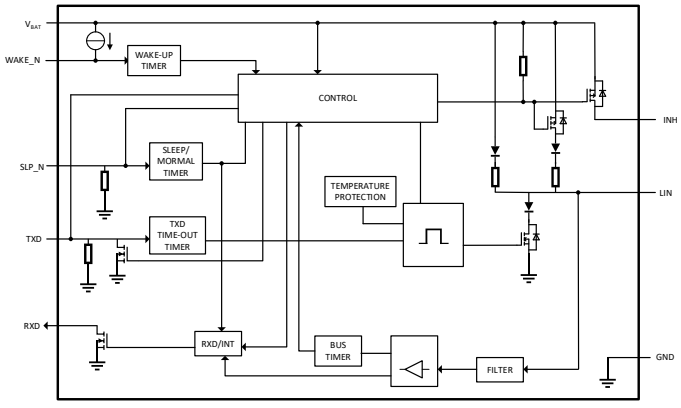

Figure 1. NCA1021S block diagram

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1. Pin Configuration and Functions

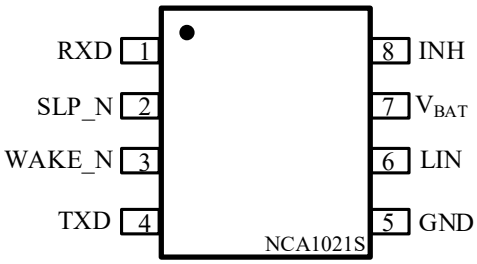


Figure 1.1 NCA1021S SOP8 Package

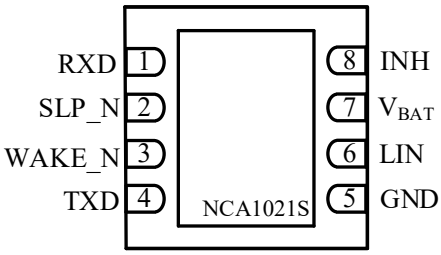


Figure 1.2 NCA1021S DFN8 Package

Table1.1 NCA1021S Pin Configuration and Description

NCA1021S PIN NO.	*SYMBOL*	*FUNCTION*
1	RXD	Receive data output (open-drain). In standby mode, the RXD pin is driven low to indicate a wake-up request.
2	SLP_N	Sleep control input (active low) integrated pull down. When SLP_N is high the device is in normal mode, When SLP_N is low the device is in sleep mode.
3	WAKE_N	Local wake-up input (active low), negative edge triggered, high voltage.
4	TXD	Transmit data input, integrated pull down, active low output after a local wake-up event.
5	GND	Ground
6	LIN	LIN bus line, input/output
7	V_{BAT}	Battery supply voltage, high voltage.
8	INH	Battery related inhibit output for controlling an external voltage regulator, high voltage. Only floating in sleep mode, the rest is high.

2. Absolute Maximum Ratings

Current into device pins is defined as positive. Current out of device pins is defined as negative.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Battery supply voltage	V_{BAT}	-0.3		40	V	With respect to GND
Voltage on pin TXD	V_{TXD}	-0.3		6	V	I_{TXD} no limitation
		-0.3		7	V	I_{TXD} < 500 μA
Voltage on pin RXD	V_{RXD}	-0.3		6	V	I_{RXD} no limitation
		-0.3		7	V	I_{RXD} < 500 μA
Voltage on pin SLP_N	V_{SLP_N}	-0.3		6	V	I_{SLP_N} no limitation
		-0.3		7	V	I_{SLP_N} < 500 μA
Voltage on pin LIN	V_{LIN}	-40		40	V	Limiting value with respect to GND, V_{BAT} and V_{WAKE_N}
Voltage on pin WAKE_N	V_{WAKE_N}	-0.3		40	V	
Current on pin WAKE_N	I_{WAKE_N}	-15			mA	Only relevant if $V_{WAKE\_N} < V_{GND}$-0.3 current will flow into pin GND
Voltage on pin INH	V_{INH}	-0.3		V_{BAT} + 0.3	V	
Output current on pin INH	$I_{O(INH)}$	-50		15	mA	
Operation ambient temperature	T_a	-40		125	℃	
Virtual junction temperature	T_{vj}	-40		150		
Storage temperature	T_{stg}	-55		150		

3. ESD ratings

Symbol	Ratings	Value	Unit
$V_{ESD-HBM1}$ $V_{ESD-HBM2}$	Human body model (JESD22/A114) - 100pF, 1.5kΩ ● Pins LIN and V_{BAT} ● Other pins	±8.0 ±7.0	kV
$V_{ESD-CDM1}$	Charged device model (JESD22/C101): ● All pins	±1.5	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Battery supply voltage	V_{BAT}	5.5		27	V
LIN Bus input voltage	V_{LIN}	0		27	V
TXD high-level input voltage	V_{IH}	2		7	V
TXD low-level input voltage	V_{IL}	-0.3		0.8	V

5. Thermal Characteristics

Parameters	Symbol	SOP8	DFN8	Unit
Junction-to-air thermal resistance	θ_{JA}	125.3	53.3	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	65.4	60	℃/W
Junction-to-board thermal resistance	θ_{JB}	68.7	25.6	℃/W

6. Specifications

6.1. Electrical Characteristics

(V_{BAT} = 5.5 V to 27 V, T_{vj} = -40 ℃ to 150 ℃. Unless otherwise noted, typical values are at V_{BAT} =12 V, T_a = 25℃).

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Battery supply current	I_{BAT}			20	μA	Sleep mode, V_{LIN} = V_{BAT} = V_{WAKE_N}, V_{TXD} = V_{SLP_N} = 0 V
				150	μA	Standby mode, bus recessive V_{INH} = V_{LIN} = V_{WAKE_N} = V_{BAT}, V_{TXD} = V_{SLP_N} = 0 V
				1200	μA	Standby mode, bus dominant V_{BAT} = V_{INH} = V_{WAKE_N} = 12 V, V_{LIN} = 0 V V_{TXD} = 0 V, V_{SLP_N} = 0 V
				1600	μA	Normal mode, bus recessive V_{INH} = V_{LIN} = V_{WAKE_N} = V_{BAT} V_{TXD} = 5 V, V_{SLP_N} = 5 V
				4	mA	Normal mode, bus dominant V_{BAT} = V_{INH} = V_{WAKE_N} = 12 V V_{TXD} = 0V, V_{SLP_N} = 5 V
Power on reset	$V_{th(POR)L}$	1.6	3.1	3.9	V	Low-level power-on reset threshold voltage
	$V_{th(POR)H}$	2.3	3.4	4.3	V	High-level power-on reset threshold voltage

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	$V_{hys(POR)}$	0.01	0.3	1	V	Power-on reset hysteresis voltage
	$V_{th(VBATL)L}$	3.9	4.4	4.7	V	Low-level V_{BAT} LOW threshold voltage
	$V_{th(VBATL)H}$	4.2	4.7	4.9	V	High-level V_{BAT} LOW threshold voltage
	$V_{hys(VBATL)}$	0.01	0.3	1	V	V_{BAT} LOW hysteresis voltage
TXD						
High-level input voltage	V_{IH}	2		7	V	
Low-level input voltage	V_{IL}	-0.3		0.8	V	
Hysteresis voltage	V_{hys}		160		mV	Guaranteed by design
Low-level input current	I_{IL}	-5		5	μA	
Output low current	I_{OL}	1.5			mA	Local wake-up request, standby mode, V_{WAKE_N} = 0 V, V_{LIN} = V_{BAT}, V_{TXD} = 0.4 V
Pull-down resistance on pin TXD	$R_{PD(TXD)}$	140		1200	kΩ	
SLP_N						
High-level input voltage	V_{IH}	2		7	V	
Low-level input voltage	V_{IL}	-0.3		0.8	V	
Hysteresis Voltage	V_{hys}		120		mV	Guaranteed by design
Low-Level Input Current	I_{IL}	-5		5	μA	V_{SLP_N} = 0 V
Pull-down resistance on pin SLP_N	$R_{PD(SLP\_N)}$	140		1200	kΩ	V_{SLP_N} = 5 V
RXD (Open-Drain)						
High-level leakage current	I_{LH}	-5		5	μA	Normal mode, V_{LIN} = V_{BAT}, V_{RXD} = 5 V
Low-level output current	I_{OL}	1.5			mA	Normal mode, V_{LIN} = 0 V, V_{RXD} = 0.4 V
WAKE_N						
High-level input voltage	V_{IH}	V_{BAT}-1		V_{BAT} + 0.3	V	Guaranteed by design
Low-level input voltage	V_{IL}	-0.3		V_{BAT} - 3.3	V	
High-level input current	I_{IH}	-5		5	μA	V_{WAKE_N} = 27 V, V_{BAT} = 27 V
Low-level input current	I_{IL}	-30		-1	μA	V_{WAKE_N} = 0 V
INH						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Switch-on resistance Between pins V_{BAT} and INH	$R_{sw(VBAT-INH)}$		20	50	Ω	Switch-on resistance between pins V_{BAT} and INH. Standby, normal, and power-on modes, I_{INH} = -15 mA, V_{BAT} = 12 V
High-level leakage current	I_{LH}	-5		5	μA	Sleep mode, V_{INH} = 27 V, V_{BAT} = 27 V
LIN						
Current limitation for transmitter dominant state	I_{BUS_LIM}	40		110	mA	V_{BAT} = 18 V, V_{LIN} = 18 V, V_{TXD} =0 V
Pull-up resistance	R_{pu}	50		250	kΩ	Sleep mode, V_{SLP_N} = 0 V
Receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$			15	μA	V_{LIN} = 18 V, V_{BAT} = 5.5 V, V_{TXD} =5 V
Receiver dominant input Leakage current including pull-up resistor	$I_{BUS\_PAS\_dom}$	-600			μA	Normal mode, V_{TXD} =5 V V_{LIN} = 0 V, V_{BAT} = 12 V
Voltage drop at the serial diode	$V_{SerDiode}$	0.4		1	V	Guaranteed by design
Loss-of-ground bus current	$I_{BUS\_NO\_GND}$	-1000		10	μA	V_{BAT} = 12 V, V_{LIN} =0 V
Loss-of-battery bus current	$I_{BUS\_NO\_BAT}$			15	μA	V_{BAT} = 0 V, V_{LIN} = 18 V
Receiver dominant state	V_{BUSdom}			0.4V_{BAT}	V	
Receiver recessive state	V_{BUSrec}	0.6V_{BAT}			V	
Receiver center voltage	V_{BUS_CNT}	0.475V_{BAT}		0.525V_{BAT}	V	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom}) / 2 V_{BAT} = 7 V to 27 V
Receiver hysteresis voltage	V_{HYS}			0.175V_{BAT}	V	V_{HYS} = V_{BUSrec} - V_{BUSdom}
Slave Resistance	R_{slave}	20		47	kΩ	Connected between pins LIN and V_{BAT}, V_{LIN} = 0 V, V_{BAT} = 12 V
Capacitance on pin LIN	C_{LIN}			30	pF	Guaranteed by design
Dominant output voltage	$V_{o(dom)}$			1.4	V	Normal mode, V_{TXD} = 0 V, V_{BAT} = 7 V
				2.0	V	Normal mode, V_{TXD} = 0 V, V_{BAT} = 18 V

6.2. Switching Characteristics

(V_{BAT} = 5.5 V to 18 V, T_{vj} = -40 ℃ to 150 ℃. Unless otherwise noted, typical values are at V_{BAT} =12 V, T_a = 25 ℃).

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Duty cycles (bus load conditions (C_{BUS} / R_{BUS}): 1 nF / 1 kΩ, 6,8 nF / 660 Ω, 10 nF / 500 Ω), see Figure 6. 1						
Duty Cycle 1	D1[1]	0.396				$V_{th(rec)(max)}$ = 0.744 × V_{BAT} $V_{th(dom)(max)}$ = 0.581 × V_{BAT} V_{BAT} = 7 V to 18 V, t_{bit} = 50 µs[2] ISO 17987 Param 27
		0.396				$V_{th(rec)(max)}$ = 0.76 × V_{BAT} $V_{th(dom)(max)}$ = 0.593 × V_{BAT} V_{BAT} = 5.5 V to 7 V, t_{bit} = 50 µs
Duty Cycle 2	D2[1]			0.581		$V_{th(rec)(min)}$ = 0.422 × V_{BAT} $V_{th(dom)(min)}$ = 0.284 × V_{BAT} V_{BAT} = 7.6 V to 18 V, t_{bit} = 50 µs ISO 17987 Param 28
				0.581		$V_{th(rec)(min)}$ = 0.41 × V_{BAT} $V_{th(dom)(min)}$ = 0.275 × V_{BAT} V_{BAT} = 6.1 V to 7 V, t_{bit} = 50 µs
Duty Cycle 3	D3[1]	0.417				$V_{th(rec)(max)}$ = 0.778 × V_{BAT} $V_{th(dom)(max)}$ = 0.616 × V_{BAT} V_{BAT} = 7 V to 18 V, t_{bit} = 96 µs ISO 17987 Param 29
		0.417				$V_{th(rec)(max)}$ = 0.797 × V_{BAT} $V_{th(dom)(max)}$ = 0.63 × V_{BAT} V_{BAT} = 5.5 V to 7 V, t_{bit} = 96 µs
Duty Cycle 4	D4[1]			0.59		$V_{th(rec)(min)}$ = 0.389 × V_{BAT} $V_{th(dom)(min)}$ = 0.251 × V_{BAT} V_{BAT} = 7.6 V to 18 V, t_{bit} = 96 µs ISO 17987 Param 30
				0.59		$V_{th(rec)(min)}$ = 0.378 × V_{BAT} $V_{th(dom)(min)}$ = 0.242 × V_{BAT} V_{BAT} = 6.1 V to 7 V, t_{bit} = 96 µs
Timing characteristics						
Fall Time	t_f			22.5	µs	20 % - 80 %, see Figure 6. 3 C_{BUS} = 1 nF and R_{BUS} = 1 kΩ C_{BUS} = 6.8 nF and R_{BUS} = 660 Ω C_{BUS} = 10 nF and R_{BUS} = 500 Ω
Rise Time	t_r			22.5	µs	
Difference between rise and fall time	$t_{(r-f)}$	-6		8	µs	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Transmitter propagation delay of failing edge	t_{tx_pdf}			10	µs	See Figure 6. 3 R_{BUS} = 500 Ω
Transmitter propagation delay of rising edge	t_{tx_pdr}			10	µs	
Transmitter propagation delay symmetry	t_{tx_sym}	-4		4.6	µs	$t_{tx\_sym} = t_{tx\_pdr} - t_{tx\_pdf}$
Receiver propagation delay of failing edge	t_{rx_pdf}			6	µs	See Figure 6. 4 C_{RXD} = 20 pF[3] and R_{RXD} = 2.4 kΩ
Receiver propagation delay of rising edge	t_{rx_pdr}			6	µs	
Receiver propagation delay Symmetry	t_{rx_sym}	-2		2	µs	$t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$
LIN dominant wake-up time	$t_{wake(dom)LIN}$	30		150	µs	Sleep mode
Dominant wake-up time on pin WAKE_N	$t_{wake(dom)WAKE\_N}$	7		85	µs	Sleep mode
Go to normal time	$t_{gotonorm}$	2		20	µs	Time period for mode change from sleep, power-on or standby mode into normal mode
Normal mode initialization time	$t_{init(norm)}$			25	µs	Normal mode, initialization time
Go to sleep time	$t_{gotosleep}$	2		30	µs	Time period for mode change from normal mode into sleep mode
TXD dominant time-out time	$t_{to(dom)TXD}$	27		90	ms	Timer started at falling edge on TXD with V_{TXD} = 0 V

[1] D1, D3= $t_{bus(rec)(min)}$ / (2*t_{bit}), D2, D4= $t_{bus(rec)(max)}$ / (2*t_{bit}), as illustrated in Figure 6. *2*.

[2] t_{bit}=50 µs (20 kbps), t_{bit}=96 µs (10.4 kbps).

[3] C_{RXD} includes load and jig capacitance.

6.3. Parameter Measurement Information

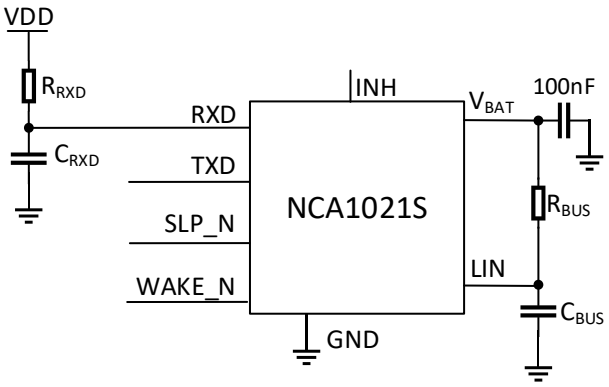


Figure 6. 1 Timing test circuit for LIN transceiver

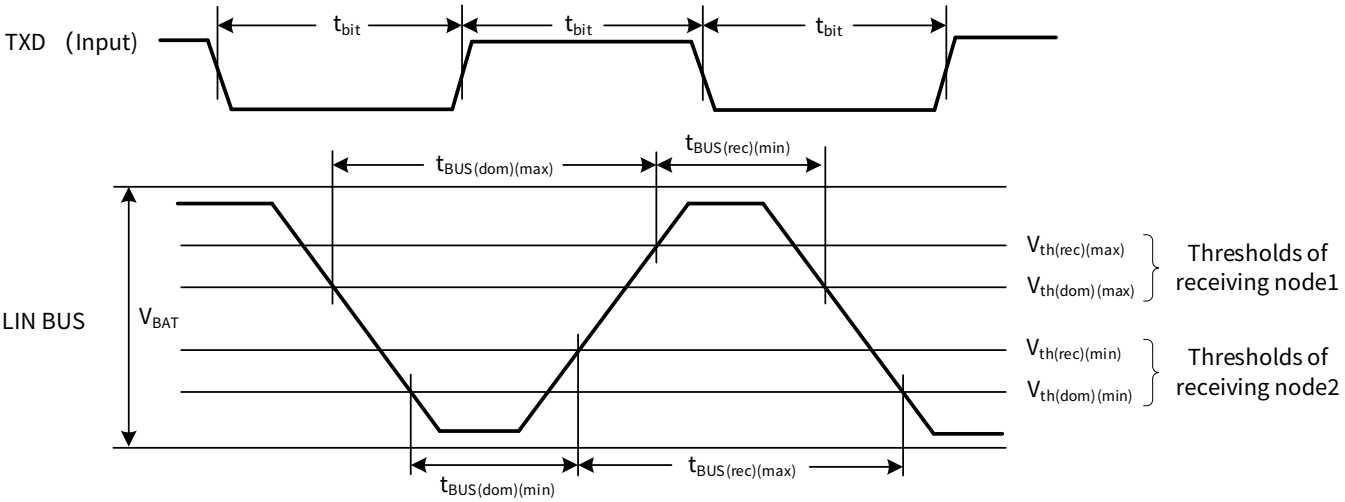


Figure 6. 2 Timing diagram of LIN transceiver

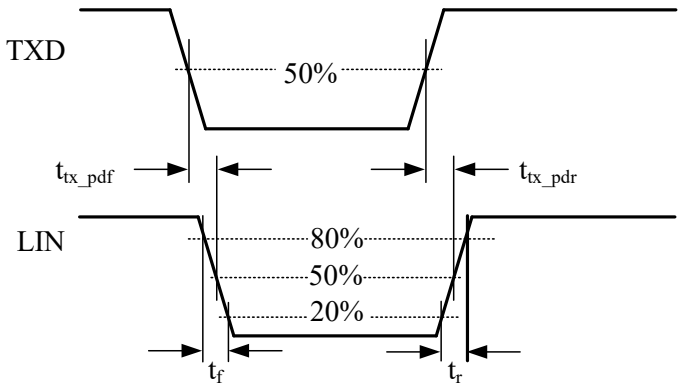


Figure 6. 3 Propagation delay and transition times from TXD to LIN

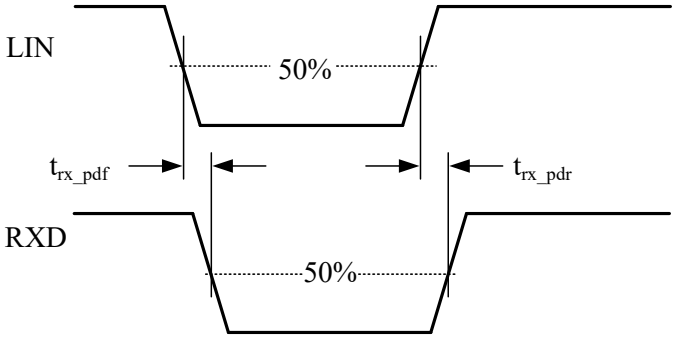


Figure 6. 4 Propagation delay and transition times from LIN to RXD

7. Function Description

7.1. Overview

The NCA1021S is a LIN transceiver with a low-power mode and multiple wake-up methods. The NCA1021S is fully compatible with the ISO 17987-4 standard. The NCA1021S controls the state of the LIN bus via the TXD pin and reports the state of the bus via its open-drain RXD output pin. An optimized electromagnetic emissions and wave-shaping transmitter is applied in NCA1021S. Therefore, the NCA1021S is providing high electromagnetic immunity and low emissions.

The data rate of the NCA1021S is up to 20 kbps. No external pull-up components are required for slave applications. For master applications, a resistor in the range of 1 kΩ and a reverse diode must be connected between the LIN bus and the power supply V_{BAT} or the INH pin.

The NCA1021S supports three methods for wake-up from sleep mode, by LIN bus, WAKE_N pin or SLP_N.

The NCA1021S allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a node through the NCA1021S INH output pin.

The NCA1021S provides thermal protection, undervoltage detection, TXD dominant time-out function and loss of power protection. Digital I/O levels compatible for 3.3 V and 5 V microcontrollers.

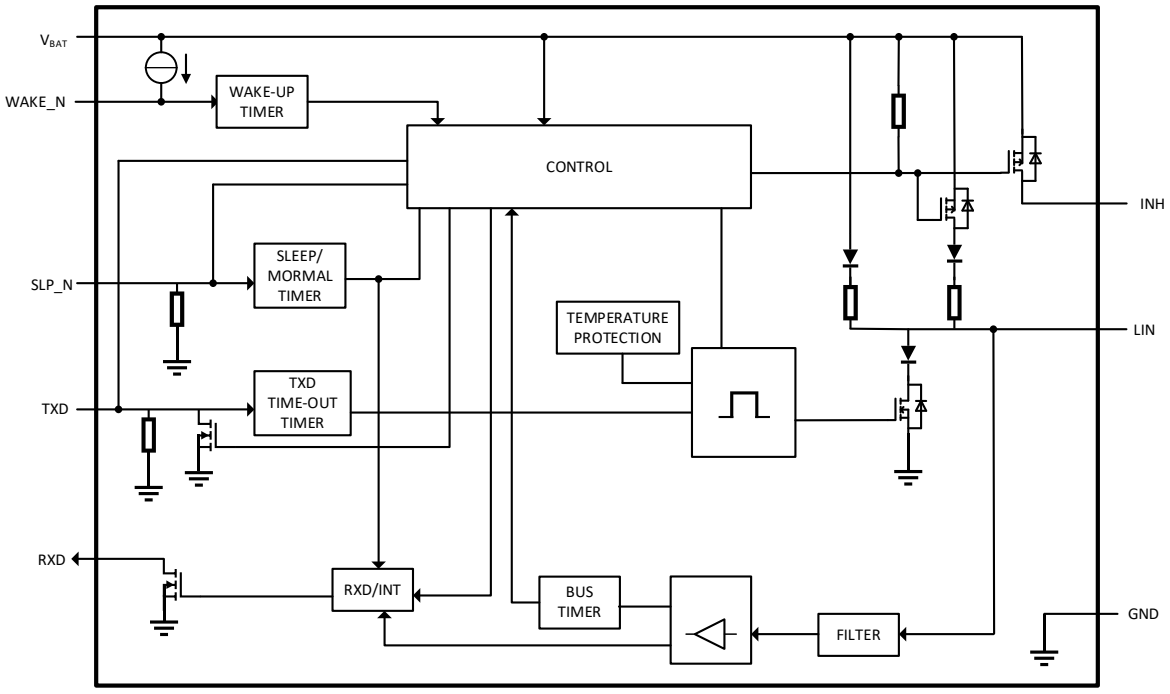


Figure 7. 1 Block diagram of NCA1021S

7.2. Device Functional Modes

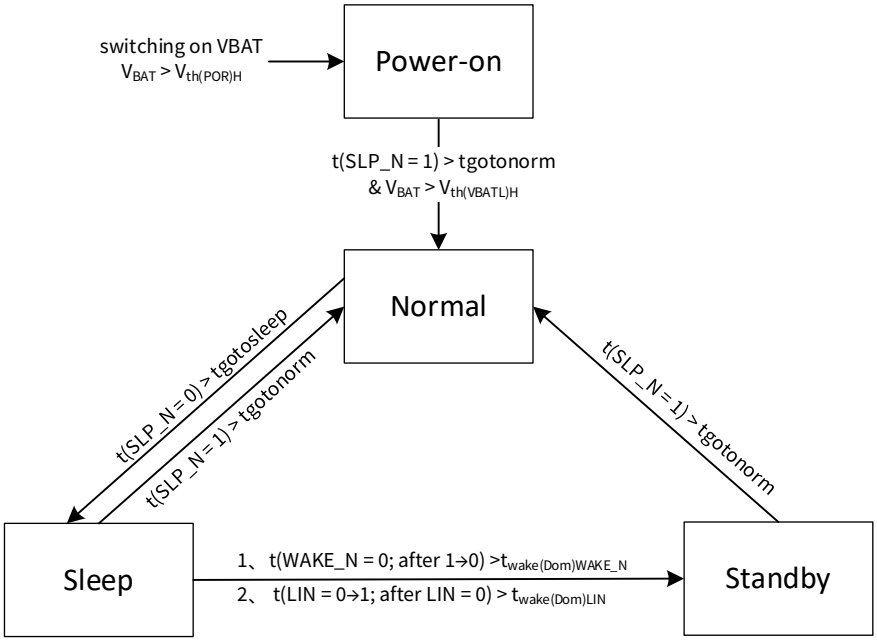


Figure 7. 2 State diagram of NCA1021S

Table 7. 1 Function table

Mode	*SLP_N*	*LIN*	*TXD (output)*	*RXD*	*INH*	*Transmitter*
Power-on[1]	low	pull up by 30 kΩ	weak pull-down	floating	high	OFF
Normal[2]	high	pull up by 30 kΩ	HIGH: recessive state LOW: dominant state	HIGH: recessive state LOW: dominant state	high	ON
Sleep	low	weak pull up	weak pull-down	floating	floating	OFF
Standby	low	pull up by 30 kΩ	weak pull-down if remote wake-up, strong pull-down if local wake-up[3]	LOW[4]	high	OFF

[1] Power-on mode is entered after switching on V_{BAT}.

[2] Normal mode is entered after a positive edge on SLP_N. If TXD is low, the transmitter is OFF. In the event of a short circuit to ground on pin TXD, the transmitter will be disabled.

[3] The internal wake-up source flag on TXD will be reset after a positive edge on pin SLP_N.

[4] The wake-up interrupt on pin RXD is released after a positive edge on pin SLP_N.

7.2.1 Power-on mode

When V_{BAT} exceeds the power-on-reset threshold voltage $V_{th(POR)H}$, the NCA1021S enters power-on mode. Though the NCA1021S is powered-up and INH is high, both the transmitter and receiver are still inactive. If $t_{(SLP\_N=1)} > t_{gotonorm}$, and V_{BAT} exceeds the $V_{th(VBATL)H}$, the NCA1021S will enter normal mode.

7.2.2 Normal mode

Under the normal mode of NCA1021S, it can receive and send normally on the LIN bus. In the normal mode, In normal mode the transmitter and receiver fully operational. The transmitter receives the signal from the MCU via the TXD, and first determines the dominant timeout, and then converts it into an optimized bus signal slew rate and waveform shaping to minimize EME. The receiver detects the signal on the LIN bus input and transmits it to the microcontroller through the RXD.

The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). No external pull-up components are required for slave applications. For a Master application, an external 1kΩ resistor in series with a diode should be connected between pin INH or V_{BAT} and pin LIN, as shown in Figure 8. 1.

7.2.3 Sleep mode

Sleep mode is the lowest power consumption mode of NCA1021S. In sleep mode the transmitter is disabled, releasing the INH to floating state. LIN bus is weakly pulled up, which can prevent false remote wake-up events.

The INH pin is switched to a floating output in sleep mode causing any system power elements controlled by the INH pin to be switched off thus reducing the system power consumption.

The only way to enter sleep mode is to make $t_{(SLP\_N=0)} > t_{gotosleep}$ in normal mode.

The NCA1021S in sleep mode supports three methods to wake up. They are wake-up remotely via LIN bus, and wake-up locally via pin SLP_N or pin WAKE_N.

7.2.4 Standby mode

When NCA1021S is in sleep mode, it will enter standby mode by local or remote wake-up by LIN bus or pin WAKE_N. When a wake-up event occurs and the NCA1021S enters standby mode, the pin RXD is driven low signaling the wake-up event to the controller.

In standby mode, the INH changes from floating to high, which can be used as a control flag for other devices. In standby mode, the LIN bus slave termination resistance, R_{slave}, is on.

In Standby mode, the condition of pin TXD indicates the wake-up source when pin SLP_N is still low. After being remotely awakened by the LIN bus, pin TXD will be in a weak pull-down state. After being woken up locally by the pin WAKE_N, pin TXD will be in a strong pull-down state.

The NCA1021S exits standby mode and enters normal mode when the pin SLP_N is set high for longer than $t_{gotonorm}$.

In standby mode, set the pin SLP_N high ($t_{(SLP\_N=1)} > t_{gotonorm}$) to enter the normal mode. Once the device enters normal mode, the wake-up event is cleared, and the RXD output is released. The RXD output is fully operation and reflects the receiver output from the LIN bus.

7.3. Pin characteristics

7.3.1 RXD

The receiver detects the data stream at the LIN bus input pin and transfers it via pin RXD to the microcontroller. The pin RXD output structure is an open-drain output structure which allows the device to be used with 3.3 V and 5 V microcontrollers. LIN recessive is represented by a high level on the pin RXD and LIN dominant is represented by a low level on the pin RXD. In standby mode, the pin RXD is driven low which can be used as an interrupt for microcontroller. The wake-up interrupt on pin RXD is released after a positive edge on pin SLP_N. If the microcontrollers RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontrollers IO supply voltage is required.

7.3.2 SLP_N

Pin SLP_N pin controls the functional modes of NCA1021S. When pin SLP_N is high, NCA1021S operates in normal mode. When SLP_N is low, NCA1021S operates in sleep mode. Pin SLP_N has an internal pull-down resistor to ensure the device remains in low power mode even if SLP_N floats.

7.3.3 WAKE_N

The NCA1021S can be woken up locally via pin WAKE_N. Filter at the input of pin WAKE_N prevents unwanted wake-up events due to automotive transients or EMI.

A falling edge at pin WAKE_N followed by $t_{(WAKE\_N=0)} > t_{wake(dom)WAKE\_N}$ results in a local wake-up. The pin WAKE_N internally pulls up to V_{BAT}.

7.3.4 TXD

TXD is the interface to the MCU LIN protocol controller that is used to control the state of the LIN output. When TXD is high, the LIN output is recessive. When the TXD is low, the LIN output is dominant. Pin TXD provides a pull-down to GND to force a predefined level on input pin TXD in case the pin TXD is unsupplied. In Standby mode, the status of pin TXD indicates the wake-up source: weak pull-down for a remote wake-up request and strong pull-down for a local wake-up request.

After switching to normal mode, the NCA1021S will detect the status of TXD. The LIN driver will be enabled only if a high TXD level is detected.

7.3.5 LIN

LIN has two internal pull-up resistors to V_{BAT}. In sleep mode, the internal slave termination between pins LIN and V_{BAT} is disabled to minimize the power dissipation. Only a weak pull-up between pins LIN and V_{BAT} is present. There is an internal slave termination resistor between pin LIN and pin V_{BAT}. For master applications, an external 1 kΩ pull-up resistor with series blocking diode can be used.

A falling edge at pin LIN followed by a low level maintained for a certain time ($t_{wake(dom)LIN}$) and a rising edge at pin LIN respectively results in a remote wake-up.

7.3.6 V_{BAT}

V_{BAT} pin is responsible for the input of the power supply. Even if there is a loss of power, the NCA1021S has extremely low leakage form the pin LIN, which will not pull the LIN bus down. The recommended voltage range for V_{BAT} is 5.5 V to 27 V. If V_{BAT} < 5.5 V or V_{BAT} > 27 V, the NCA1021S may remain operational, but parameter values cannot be guaranteed.

7.3.7 INH

Pin INH is battery related inhibit output for controlling an external voltage regulator. Only in sleep mode INH is floating, the rest is high. As a result of the high condition on pin INH the voltage regulator and the microcontroller can be activated.

7.4. TXD dominant time-out function

During normal mode, a TXD dominant time-out timer circuit in NCA1021S prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period $t_{to(dom)TXD}$. The timer is triggered by a negative edge on pin TXD. If the duration of the low-level on pin TXD exceeds the internal timer value ($t_{to(dom)TXD}$), the transmitter is disabled, driving the bus line into a recessive state. The timer is reset by a positive edge on pin TXD.

7.5. Fail-safe features

The current of the transmitter output stage is limited to protect the transmitter against short circuit to pins V_{BAT} or GND.

In automotive applications, some LIN transceivers in a system can be unpowered or ignition supplied, while others in the network remains powered by the battery. A loss of power (pins V_{BAT} and GND) has no impact on the LIN bus line and the microcontroller. There are no reverse currents from the bus.

The transmitter at pin LIN is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the thermal protection circuit disables the transmitter. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled.

If V_{BAT} drops below $V_{th(VBATL)L}$, a protection circuit disables the transmitter. The transmitter is enabled again when $V_{BAT} > V_{th(VBATL)H}$.

8. Application Note

8.1. Typical Application

The Figure 8. 1 is the basic schematic of NCA1021S. The NCA1021S requires a 0.1 μF bypass capacitors between V_{BAT} and GND. The bypass capacitance value can also be determined according to the actual situation of the system. The capacitor should be placed as close as possible to the package.

For a Master application, an external 1kΩ resistor in series with a diode should be connected between pin INH or V_{BAT} and pin LIN. If RXD on the MCU does not have an internal pull-up, an external pull-up resistor is required.

The LIN external capacitance value is selected according to the actual situation (refer to ISO 17987-4:2016 5.3.6 Line characteristics), generally 220 pF for the slave or 1nF for the master. To alleviate EMI problems, EMI filtering of LIN bus is strongly recommended, which is also a necessary measure. In addition to LIN message itself will radiate noise through rising edge, falling edge and asymmetric waveform, noise from other parts of the car may also penetrate LIN bus. Usually, a ferrite bead or inductor can be connected in series on the LIN bus.

Transient pulse suppression is also important for LIN buses, so it is recommended to add bidirectional TVS tubes.

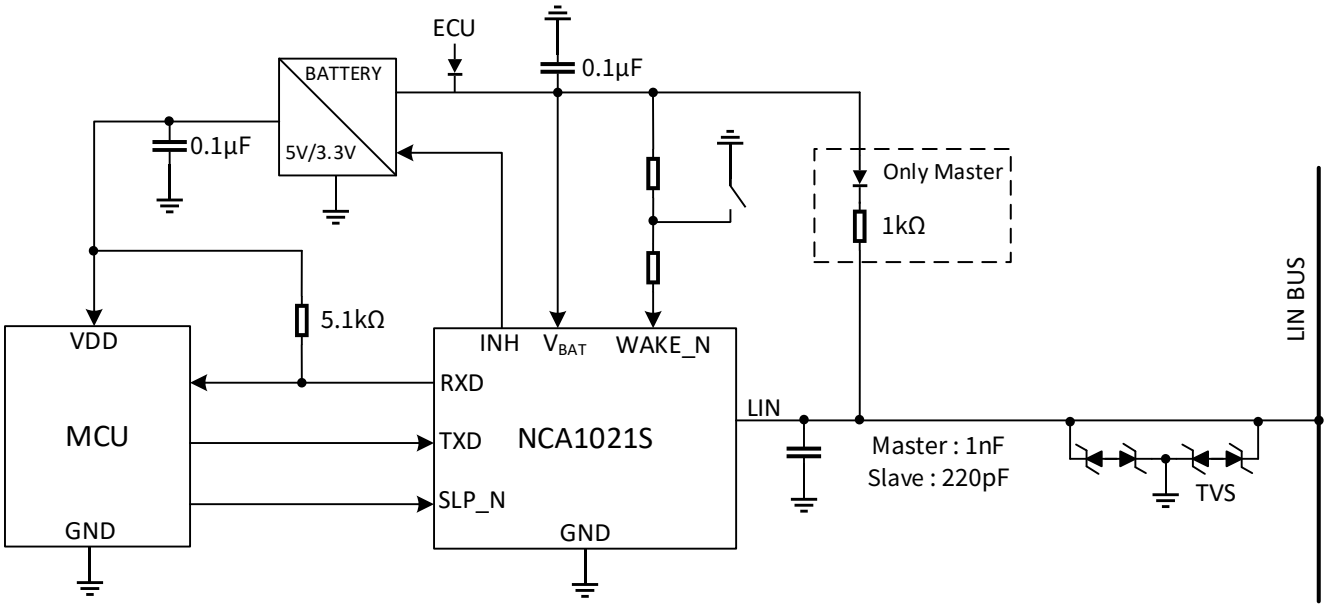
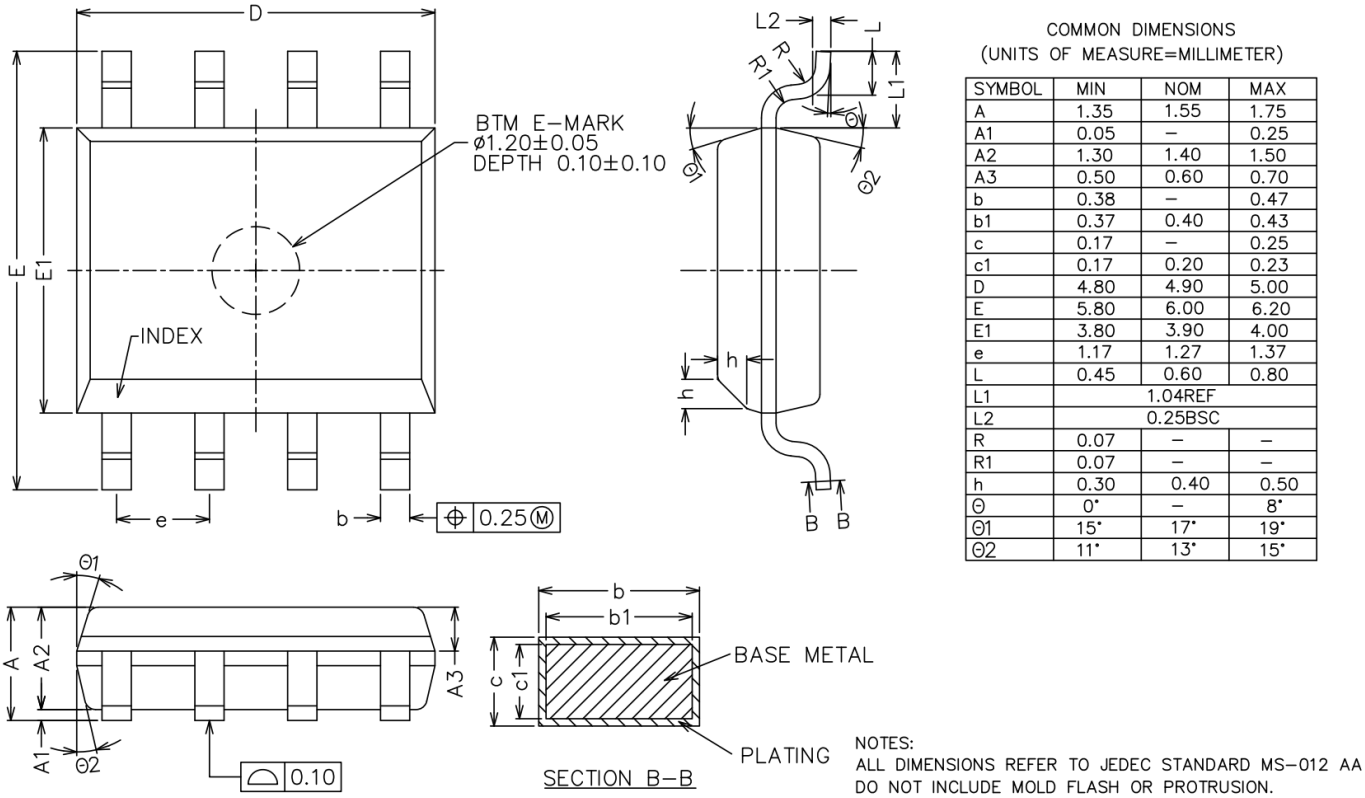


Figure 8. 1 Basic schematic of NCA1021S

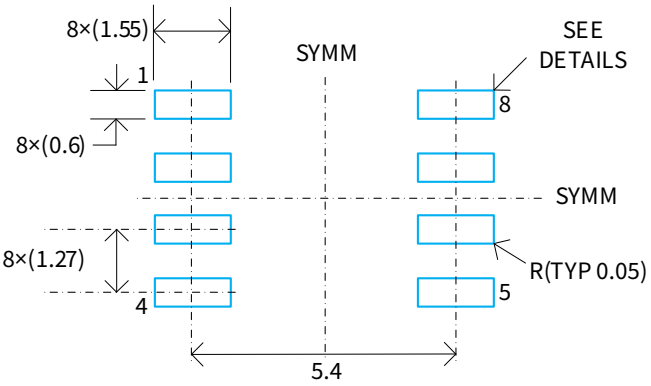
9. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
Θ	0°	–	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°

Figure 9. 1 SOP8 package shape and dimension in millimeters



LAND PATTERN EXAMPLE(mm)

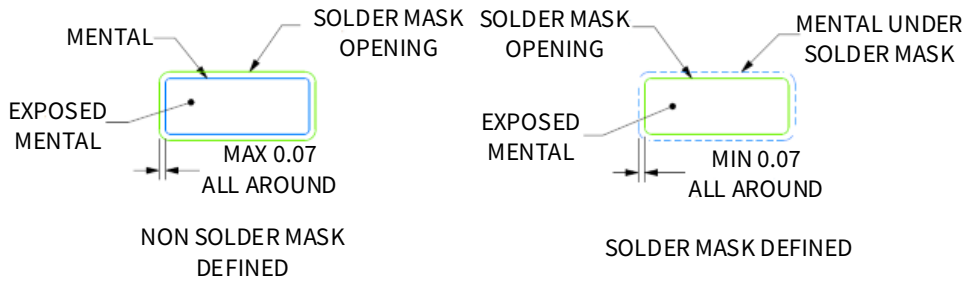
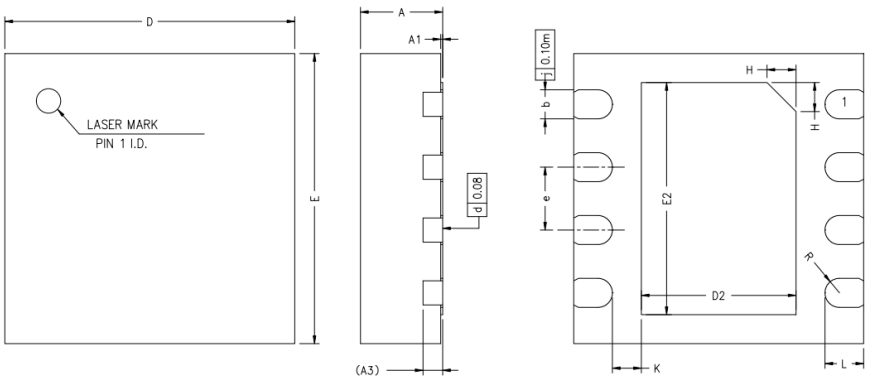


Figure 9. 2 SOP8 package board layout example



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.25	0.30	0.35
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.50	1.60	1.70
E2	2.30	2.40	2.50
e	0.55	0.65	0.75
H		0.30REF	
K	0.20	0.30	0.40
L	0.35	0.40	0.45
R		0.15REF	

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 9. 3 DFN8 package shape and dimension in millimeters

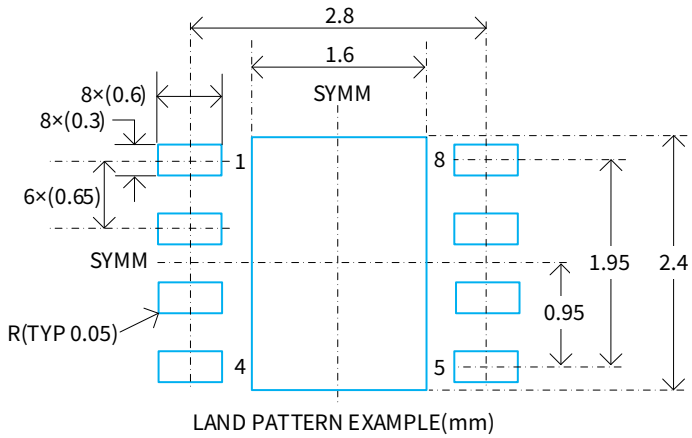
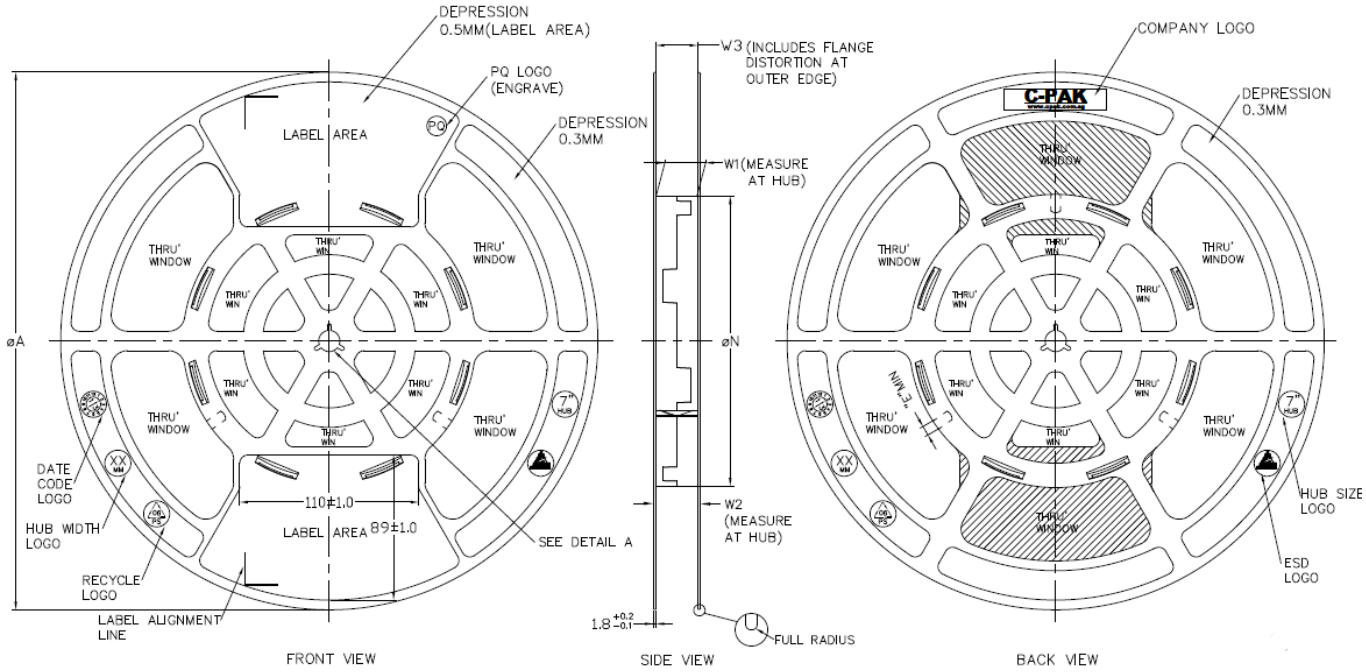


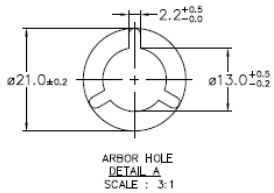
Figure 9. 4 DFN8 package board layout example

10. Order Information

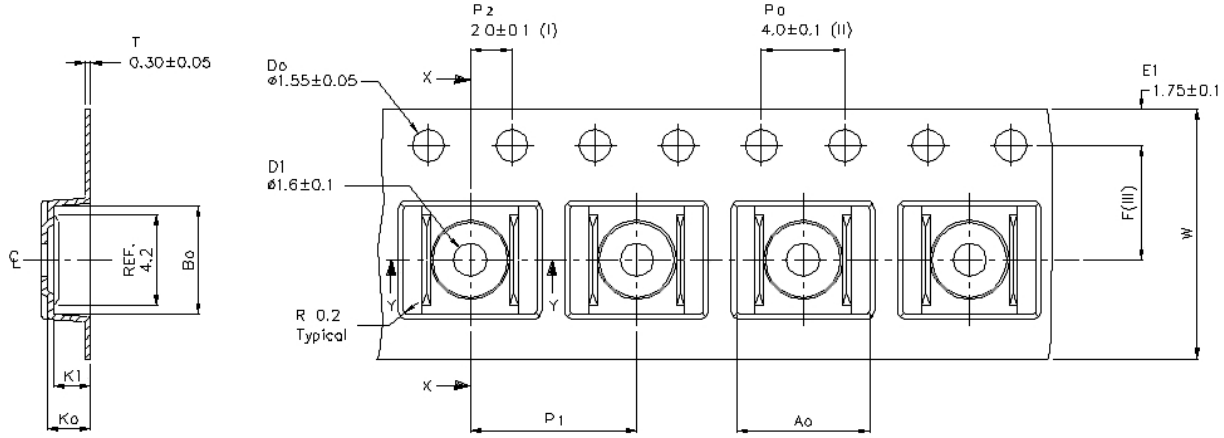
Part Number	*Max Data Rate (kbps)*	*Junction Temperature*	*MSL*	*Package*	*SPQ*
NCA1021S-Q1SPR	20	-40 ℃ to 150 ℃	1	SOP8	2500
NCA1021S-Q1DNR	20	-40 ℃ to 150 ℃	1	DFN8	5000

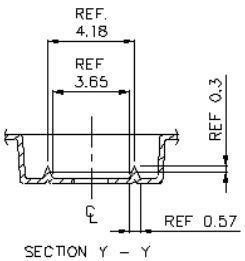
11. Tape and Reel Information





PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5





Ao	6.50	+/–	0.1
Bo	5.30	+/–	0.1
Ko	2.20	+/–	0.1
K1	1.90	+/–	0.1
F	5.50	+/–	0.1
P1	8.00	+/–	0.1
W	12.00	+/–	0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

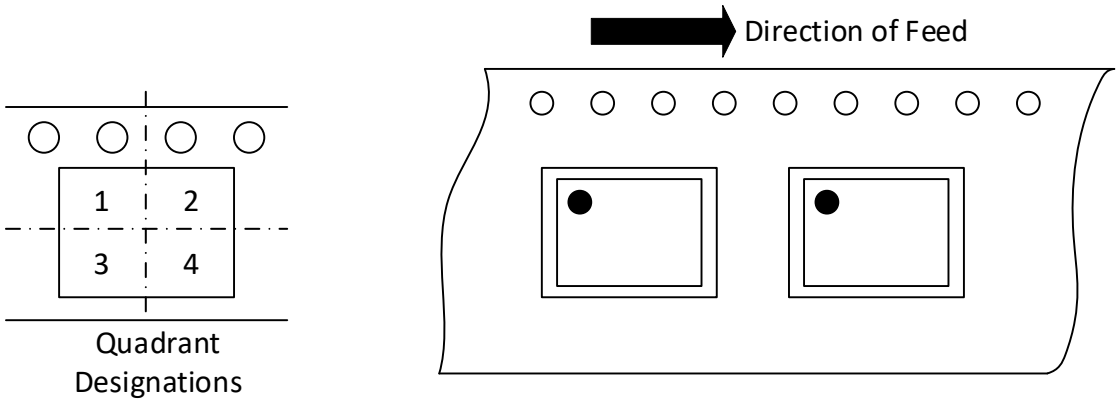
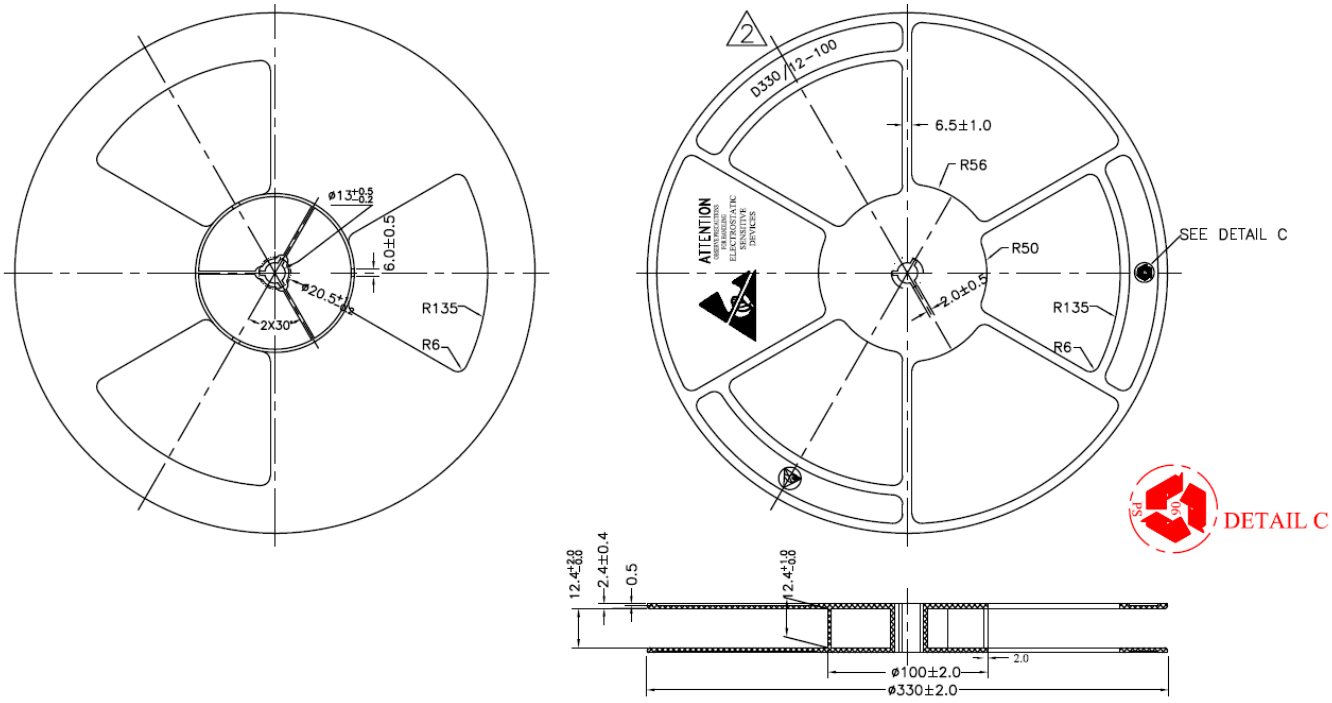
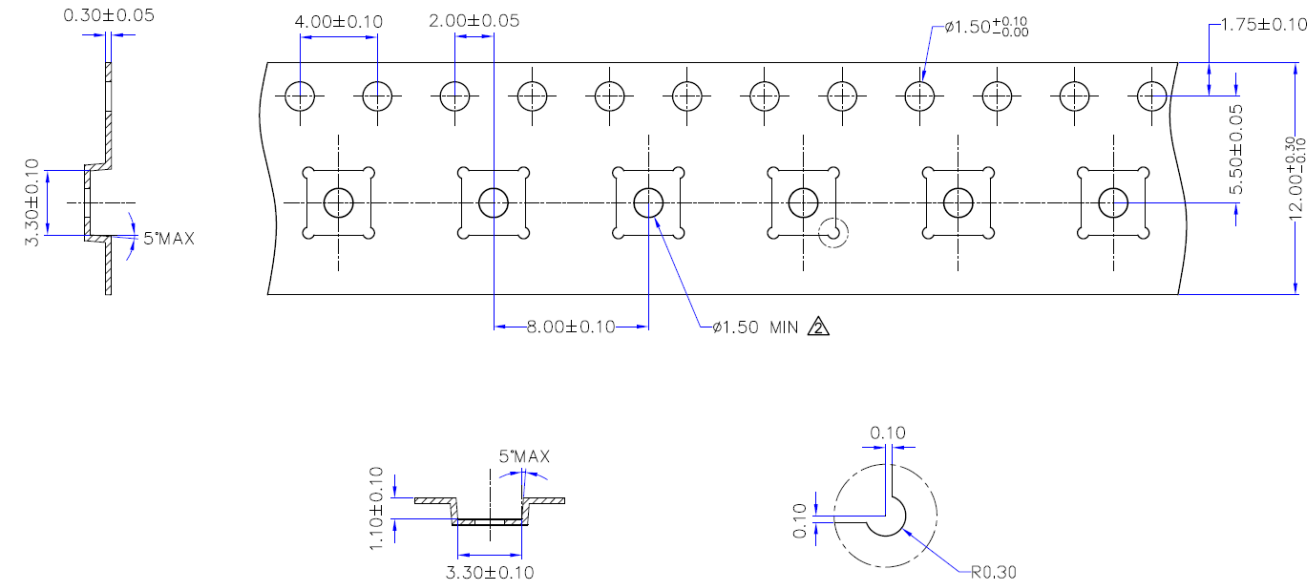


Figure 11. 1 Tape and Reel Information of SOP8 in millimeters





NOTES:
1. ALL DIMS IN MM
2. MATERIAL: BLACK CONDUCTIVE POLYSTYRENE
3. 10 sprocket hole pitch cumulative tolerance ±0.20mm
4. Carrier camber is within 1mm in 250mm
5. There must not be foreign body adhesion and the state of the surface must be excellent
6. Surface resistance 1X10E5≤Rs≤1X10E9 OHMS/SQ
7. 17" PLASTIC-Reel, 60625 pockets (485m)
QFN3×3

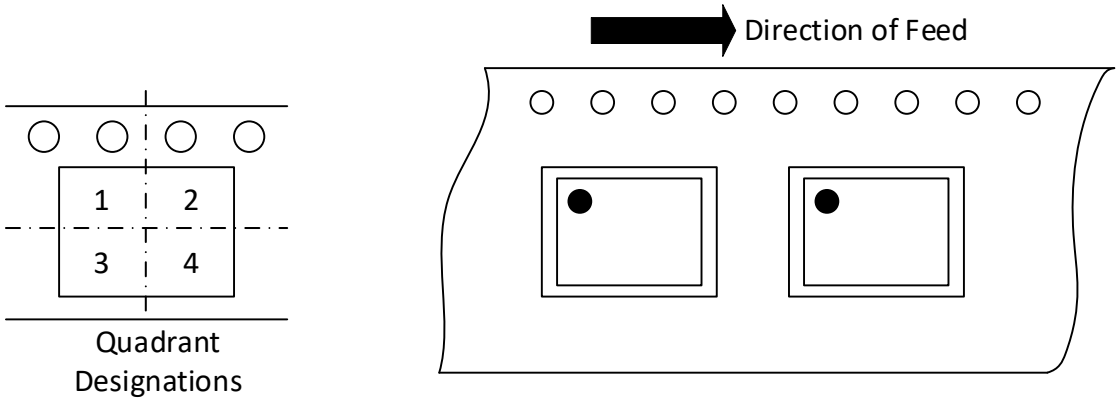


Figure 11. 2 Tape and reel information of DFN8 in millimeters

12. Revision History

Revision	Description	Date
1.0	Initial version	2023/12/11
1.1	Added restriction for V_{BUS_CNT}. Corrected condition for $t_{wake(dom)WAKE\_N}$. Replace commander and responder with master and slave. Updated the description of the master node in section 8.1. Updated Figure 8. 1. Updated SOP8 package board layout example. Added DFN8 package board layout example.	2024/4/19

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