NOVOSENSE

NCA1145B
High-speed CAN Transceiver for Partial Networking
Datasheet (EN) 1.0

Product Overview

NCA1145B is a high-speed CAN transceiver providing an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver consumes very low power in Standby and Sleep modes. Meanwhile, NCA1145B supports CAN Partial Networking compliant to ISO11898-2:2024 by selective wake-up function. NCA1145B supports 'FD-passive' to ignore CAN FD frames while waiting for a valid wake-up frame in low power mode. It allows the CAN controllers that do not need CAN FD function to remain in Standby/Sleep mode during CAN FD communication in the network without generating bus errors.

The CAN signal improvements significantly reduce signal ringing on the network, allowing reliable CAN FD communication at 5 Mbit/s in larger topologies.

NCA1145B supplies an SPI interface to control the transceiver and to retrieve the status information. The I/O level of the transceiver is adjusted to the I/O level of microcontrollers as required, including 1.8V, 3.3V and 5V.

Key Features

- AEC-Q100 Qualified for automotive applications, Grade 1
- Fully compatible with the ISO11898-2:2024 standard
- I/O voltage range supports 1.8V,3.3V and 5V MCU
- Power supply voltage: V_{CC}: 4.5V to 5.5V
  V_{IO}: 1.7V to 5.5V
  V_{BAT}:4.5V to 40V
- Very low-current Standby and Sleep modes
- Autonomous bus biasing
- Remote wake-up via standard CAN wake-up pattern or via ISO 11898-2:2024 compliant selective wake-up frame detection and local wake-up via the WAKE pin
- Bus fault protection: -58V to 58V
- Overtemperature warning and shut-down
- 16- or 24- or 32-bit SPI for configuration, control and diagnosis
- Data rate: up to 5Mbps
- Advanced system and transceiver interrupt handling
- Operation temperature: -40℃~125℃
- RoHS & REACH compliant packages: SOP14, DFN14

Applications

- Automotive infotainment and cluster
- Hybrid, electric and powertrain systems
- Body electronics and lighting

Device Information

Part Number	*Package*	*Body Size*
NCA1145B-Q1SPKR	SOP14	8.63mm × 3.90mm
NCA1145B-Q1DNKR	DFN14	4.50mm × 3.00mm

Functional Block Diagrams

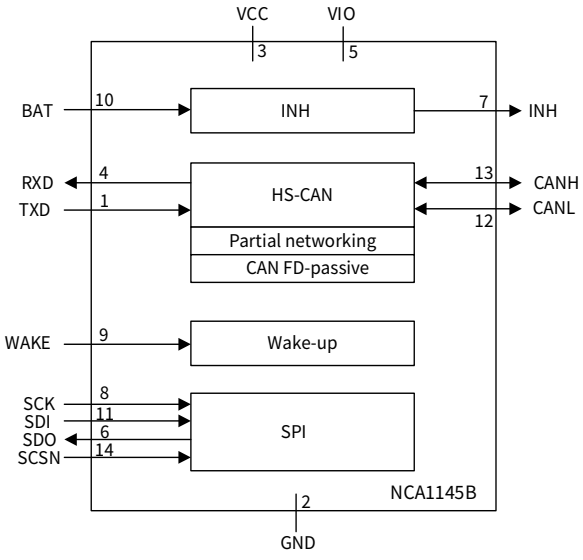

Figure 1 NCA1145B Block Diagram

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1. Pin Configuration and Functions

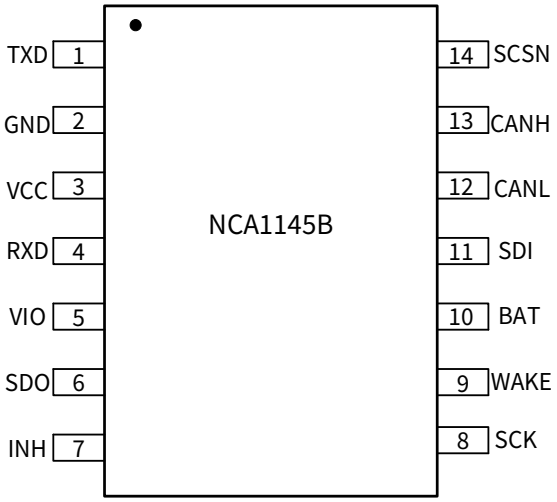


Figure 1.1 NCA1145B (SOP14) Package

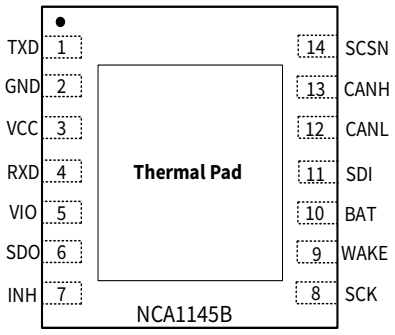


Figure 1.2 NCA1145B (DFN14) Package

Table 1.1 NCA1145B Pin Configuration and Description

NSI8266W PIN NO.	*SYMBOL*	*FUNCTION*
1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	Ground(1)
3	V_{CC}	5V CAN transceiver supply voltage
4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	V_{IO}	Logic I/O supply voltage
6	SDO	SPI data output
7	INH	Inhibit output for switching external voltage regulators
8	SCK	SPI clock input
9	WAKE	Local wake-up input
10	BAT	Battery supply voltage
11	SDI	SPI data input
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	SCSN	SPI chip select input

(1) The thermal pad is recommended to be soldered to board ground.

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	V_{CC}, V_{IO}	-0.2		6	V	
	BAT	-0.2		58	V	
Input Voltage	TXD , SDI, SCSN, SCK	-0.2		V_{IO}+0.2	V	The maximum voltage must not exceed 6V
	INH	-0.2		V_{BAT}+0.2	V	
	WAKE	-58		58	V	
Output Voltage	RXD, SDO	-0.2		V_{IO}+0.2	V	The maximum voltage must not exceed 6 V
Bus Pin Voltage	V_{CANH}、V_{CANL}	-58		58	V	
Voltage between pin CANH and CANL	$V_{(CANH-CANL)}$	-58		58	V	
Transient voltage	V_{trt}	on pins CANL, CANH, WAKE, BAT				
		-100			V	pulse 1
				75	V	pulse 2a
		-150			V	pulse 3a
				100	V	pulse 3b
Output Current	I_O	-15		15	mA	Pin RXD, SDO
Junction Temperature	T_j	-40		150	°C	
Storage Temperature	T_{stg}	-55		150	°C	

3. ESD Ratings

	Ratings	*Value*	*Unit*
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● CANH,CANL to GND ● Other pins	 ±8.0 ±4.0	 kV kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±2.0	kV
	System， per IEC 61000-4-2 (150 pF, 330 Ω at pins CANH and CANL to GND	±7.0	kV
	Machine model (MM), per AEC-Q100-003-RevD on any pin	±200	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	unit
Power Supply Voltage	V_{BAT}	4.5		40	V
	V_{CC}	4.5		5.5	V
	V_{IO}	1.7		5.5	V
Operating Temperature	T_a	-40		125	℃

5. Thermal Information

Parameters	Symbol	SOP14	DFN14	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	77.6	34.8	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC（top）}$	32.6	37.3	℃/W
Junction-to-board thermal resistance	θ_{JB}	34.5	12.5	℃/W

6. Specifications

6.1. Static Characteristics

(V_{CC}=4.5V~5.5V, V_{IO}=1.7V~5.5V, V_{BAT}=4.5V~40V, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{CC}=5V, V_{IO}=3.3V, V_{BAT}=12V, T_a = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	V_{CC}	4.5	5	5.5	V	
	V_{IO}	1.7	3.3	5.5	V	
	V_{BAT}	4.5	12	40	V	
Power-on detection threshold voltage	$V_{th(det)pon}$	3.95		4.48	V	BAT pin
Power-off detection threshold voltage	$V_{th(det)poff}$	2.84		3.21	V	
CAN undervoltage recovery voltage	$V_{uvr(CAN)}$	3.95		4.48	V	
CAN undervoltage detection voltage	$V_{uvd(CAN)}$	3.86		4.37	V	
Undervoltage detection voltage on pin V_{CC}	$V_{uvd(VCC)}$	3.91		4.46	V	V_{CC} pin
Undervoltage detection voltage on pin V_{IO}	$V_{uvd(VIO)}$	1.4		1.65	V	V_{IO} pin

Battery supply current	I_{BAT}		1	1.5	mA	Normal mode
			48	140	µA	Sleep mode; CAN Offline mode; -40°C < T_a< 125°C; V_{BAT} = 4.5 V to 40V
			48	64	µA	Sleep mode; CAN Offline mode; -40°C < T_a< 85°C; V_{BAT} = 4.5 V to 40V
			56	150	µA	Standby mode; CAN Offline mode; -40°C < T_a< 125°C; V_{BAT} = 4.5 V to 40V
			56	73	µA	Standby mode; CAN Offline mode; -40°C < T_a< 85°C; V_{BAT} = 4.5 V to 40V
			46	70	µA	additional current in CAN Offline Bias mode; -40°C < T_a< 125°C
			0.4	0.65	mA	additional current in CAN Offline Bias mode with active partial networking decoder; Standby or Sleep mode; -40°C < T_a< 125°C
			1	3	µA	additional current from WAKE input; WPRE = WPFE = 1; -40°C < T_a < 125°C
Supply current	I_{CC}		4	6	mA	CAN Active mode; CAN recessive; V_{TXD} = V_{IO}
			45	60	mA	CAN Active mode; CAN dominant; V_{TXD} = 0 V
			4.7	6	µA	Standby/Normal mode; CAN inactive; -40°C < T_a < 125°C
			3.8	5	µA	Sleep mode; CAN inactive; -40°C < T_a < 125°C
			75	95	mA	short circuit on bus lines; CAN dominant; V_{TXD} = 0 V; -3 V < (V_{CANH} = V_{CANL}) < +18 V
Supply current on pin V_{IO}	I_{IO}		7.1	11	µA	Standby/Normal mode; -40°C < T_a < 125°C
			5	8	µA	Sleep mode; -40°C < T_a < 125°C
pins SDI, SCK and SCSN						
Switching threshold voltage	$V_{th(sw)}$	0.25V_{IO}		0.75V_{IO}	V	V_{IO} = 1.7 V to 5.5 V
Switching threshold voltage hysteresis	$V_{th(sw)hys}$		0.2		V	V_{IO} =1.7 V to 5.5 V

Pull-down resistance on pin SCK	$R_{pd(SCK)}$	40	60	80	kΩ	
Pull-up resistance on pin SCSN	$R_{pu(SCSN)}$	40	60	80	kΩ	
Pull-down resistance on pin SDI	$R_{pd(SDI)}$	40	60	80	kΩ	$V_{SDI} < V_{th(sw)}$
Pull-up resistance on pin SDI	$R_{pu(SDI)}$	40	60	80	kΩ	$V_{SDI} > V_{th(sw)}$， VIO=2.8-5.5V
pin SDO						
High-level output voltage	V_{OH}	V_{IO}-0.5			V	I_{OH}=-4mA(V_{IO}=2.8V-5.5V) or I_{OH}=-2mA(V_{IO}=1.7V-2.8V)
Low-level output voltage	V_{OL}			0.4	V	I_{OL}=-4mA(V_{IO}=2.8-5.5V) or I_{OL}=-2mA(V_{IO}=1.7-2.8V)
Off-state output leakage current	$I_{LO(off)}$	-5		5	μA	$V_{SCSN} = V_{IO}$; V_O = 0 V to V_{IO}
pin INH						
Output voltage	V_O	V_{BAT}-1		V_{BAT}	V	I_{INH} =-6mA
Pull-down resistance	R_{pd}	2.8	4	5	MΩ	Sleep mode
pin TXD						
Switching threshold voltage	$V_{th(sw)}$	0.3*V_{IO}		0.7*V_{IO}	V	V_{IO} = 1.7 V to 5.5 V
Switching threshold voltage Hysteresis	$V_{th(sw)hys}$		0.2		V	V_{IO} = 1.7 V to 5.5 V
Pull-up resistance	R_{pu}	40	60	90	kΩ	
pin RXD						
High-level output voltage	V_{OH}	V_{IO}-0.5			V	I_{OH}=-4mA(V_{IO}=2.8V-5.5V) or I_{OH}=-2mA(V_{IO}=1.7V-2.8V)
Low-level output voltage	V_{OL}			0.4	V	I_{OL}=-4mA(V_{IO}=2.8-5.5V) or I_{OL}=-2mA(V_{IO}=1.7-2.8V)
pin WAKE						
Rising switching threshold voltage	$V_{th(sw)r}$	2.8		4.1	V	
Falling switching threshold voltage	$V_{th(sw)f}$	2.4		3.75	V	
Input hysteresis voltage	$V_{hys(i)}$	250		800	mV	
Input current	I_i			1.5	μA	-40°C ≤T_a≤125°C
pins CANH and CANL						
Dominant output voltage	$V_{O(dom)}$	CAN Active mode; V_{TXD} = 0 V; t <$t_{to(dom)TXD}$				
		2.75	3.5	4.5	V	pin CANH; R_L = 50Ω to 65Ω

		0.5	1.5	2.25	V	pin CANL; R_L = 50Ω to 65Ω
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	-400		400	mV	$V_{dom(TX)sym} = V_{CC}-V_{CANH} -V_{CANL}$; V_{CC} = 5 V
Transmitter voltage symmetry	V_{TXsym}	$0.9V_{CC}$		$1.1V_{CC}$		$V_{TXsym} = V_{CANH} + V_{CANL}$; f_{TXD} = 250 kHz, 1MHz or 2.5MHz;(1)V_{CC} = 4.75V to 5.25V ;C_{SPLIT} = 4.7nF, guaranteed by design.
common mode voltage step	$V_{cm(step)}$	-150		150	mv	guaranteed by design.
peak-to-peak common mode voltage	$V_{cm(p-p)}$	-300		300	mv	guaranteed by design.
Differential output voltage	$V_{O(dif)}$	CAN Active mode (dominant); V_{TXD} = 0 V; V_{CC} = 4.5 V to 5.5 V; t <$t_{to(dom)TXD}$				
		1.5		3	V	R_L = 45Ω to 70Ω
		1.5		5	V	R_L = 2240Ω
		recessive; R_L = no load				
		-50		50	mV	CAN Active/Listen-only/Offline Bias mode; $V_{TXD} = V_{IO}$
		-0.2		0.2	V	CAN Offline mode
Recessive output voltage	$V_{O(rec)}$	2	0.5*VCC	3	V	CAN Active mode; $V_{TXD} = V_{IO}$; R_L = no load
		-0.1		0.1	V	CAN Offline mode; R_L = no load
		2	2.5	3	V	CAN Offline Bias/Listen-only modes; R_L = no load; V_{CC} = 0 V
Dominant short-circuit output current	$I_{O(sc)dom}$	CAN Active mode; V_{TXD} = 0 V; V_{CC} = 5 V				
		-115			mA	pin CANH; V_{CANH} = -15 V to 40 V
				115	mA	pin CANL; V_{CANL} = -15 V to 40 V
Recessive short-circuit output current	$I_{O(sc)rec}$	-3		3	mA	$V_{CANL} = V_{CANH}$ = -27 V to 32 V; $V_{TXD} = V_{IO}$
Differential receiver threshold voltage	$V_{th(RX)dif}$	-12 V≤V_{CANL} -≤+12 V; -12 V ≤ V_{CANH}≤ +12 V				
		0.5	0.7	0.9	V	CAN Active/Listen-only modes
		0.4	0.7	1.15	V	CAN Offline mode
Receiver recessive voltage	$V_{rec(RX)}$	-12 V≤V_{CANL} ≤+12 V; -12 V ≤ V_{CANH} ≤ +12 V				
		-4		0.5	V	CAN Active/Listen-only modes, guaranteed by design.
		-4		0.4	V	CAN Offline mode, guaranteed by design.

Receiver dominant voltage	$V_{dom(RX)}$	-12 V≤V_{CANL} ≤+12 V; -12 V ≤ V_{CANH} ≤ +12 V				
		0.9		9	V	CAN Active/Listen-only modes, guaranteed by design.
		1.15		9	V	CAN Offline mode, guaranteed by design.
Differential receiver hysteresis voltage	$V_{hys(RX)dif}$	1	30	60	mV	CAN Active/Listen-only modes; -12 V≤V_{CANL} ≤+12 V; -12 V ≤ V_{CANH} ≤ +12 V
Input resistance	R_i	25	40	50	kΩ	-2V≤V_{CANL} ≤+7V; -2 V ≤ V_{CANH} ≤ +7V
Input resistance deviation	ΔR_i	-1		1	%	0V≤V_{CANL} ≤+5V; 0V ≤ V_{CANH} ≤ +5V
Differential input resistance	$R_{i(dif)}$	50	80	100	kΩ	-2V≤V_{CANL} ≤+7V; -2 V ≤ V_{CANH} ≤ +7V
Common-mode input capacitance	$C_{i(cm)}$			36	pF	guaranteed by design.
Differential input capacitance	$C_{i(dif)}$			18	pF	guaranteed by design.
Leakage current	I_L	-10		10	μA	V_{BAT} = V_{CC} = 0 V or V_{BAT} = V_{CC} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V
Temperature protection						
overtemperature protection activation threshold temperature	$T_{th(act)otp}$	167	177	187	°C	
overtemperature protection release threshold temperature	$T_{th(rel)otp}$	127	137	147	°C	
overtemperature protection warning threshold temperature	$T_{th(warn)otp}$	127	137	147	°C	

(1) The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 6.5.

6.2. Dynamic Characteristics

(V_{CC}=4.5V~5.5V, V_{IO}=1.7V~5.5V, V_{BAT}=4.5V~40V, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{CC}=5V, V_{IO}=3.3V, V_{BAT}=12V, T_a = 25°C)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
pins BAT, VCC, VIO						
Start-up time	$t_{startup}$		2.8	4.7	ms	from V_{BAT} exceeding the power-on detection threshold until INH active
Undervoltage detection delay time	$t_{d(uvd)}$	6		54	μs	guaranteed by design.

Delay time from undervoltage detection to sleep mode	$t_{d(uvd-sleep)}$	200	310	400	ms	from undervoltage detection on V_{CC} and/or V_{IO} until NCA1145B forced to Sleep mode
pins SCSN, SCK, SDI, SDO; see Figure 7.3						
Clock cycle time	$t_{cy(clk)}$	250			ns	Normal/Standby modes
		1			µs	Sleep mode
SPI enable lead time	$t_{SPILEAD}$	50			ns	Normal/Standby modes
		200			ns	Sleep mode
SPI enable lag time	t_{SPILAG}	50			ns	Normal/Standby modes
		200			ns	Sleep mode
Clock high time	$t_{clk(H)}$	100			ns	Normal/Standby modes
		475			ns	Sleep mode
Clock low time	$t_{clk(L)}$	100			ns	Normal/Standby modes
		475			ns	Sleep mode
Data input set-up time	$t_{su(D)}$	50			ns	Normal/Standby modes
		200			ns	Sleep mode
Data input hold time	$t_{h(D)}$	50			ns	Normal/Standby modes
		200			ns	Sleep mode
Data output valid time	$t_{v(Q)}$			60	ns	pin SDO; C_L = 20pF; VIO=2.8-5.5V
				100	ns	pin SDO; C_L = 20pF; VIO=1.7-2.8V
SDI to SDO delay time	$t_{d(SDI-SDO)}$			60	ns	pin SDO; C_L = 20pF; VIO=2.8-5.5V
				100	ns	pin SDO; C_L = 20pF; VIO=1.7-2.8V
Chip select pulse width HIGH	$t_{WH(S)}$	250			ns	pin SCSN; Normal/Standby modes
		1			µs	pin SCSN; Sleep mode
Delay time from SCK LOW to SCSN LOW	$t_{d(SCKL-SCSNL)}$	50			ns	
pins CANH, CANL, TXD and RXD ,V_{CC} = 4.5 V to 5.5 V						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$		80		ns	R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF

Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$		80		ns	R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$		105		ns	R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$		120		ns	R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
Delay time from TXD LOW to RXD LOW	$t_{d(TXDL-RXDL)}$			255	ns	$t_{bit(TXD)}$ = 200 ns, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
Delay time from TXD HIGH to RXD HIGH	$t_{d(TXDH-RXDH)}$			255	ns	$t_{bit(TXD)}$ = 200 ns, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
Transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)}$ = 500 ns, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
		155		210	ns	$t_{bit(TXD)}$ = 200 ns, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
Bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)}$ = 500 ns, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
		120		220	ns	$t_{bit(TXD)}$ = 200 ns, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
Receiver timing symmetry	Δt_{rec}	-65		40	ns	$t_{bit(TXD)}$ = 500 ns, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
		-45		15		$t_{bit(TXD)}$ = 200 ns, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF
Bus dominant wake-up time	$t_{wake(busdom)}$	0.5		1.8	µs	first pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode
		0.5		1.8	µs	second pulse for wake-up on pins CANH and CANL
Bus recessive wake-up time	$t_{wake(busrec)}$	0.5		1.8	µs	first pulse for wake-up on pins CANH and CANL; CAN Offline mode
		0.5		1.8	µs	second pulse (after first dominant) for wake-up on pins CANH and CANL

Bus wake-up time-out time	$t_{to(wake)bus}$	0.8		10	ms	between first and second dominant pulses; CAN Offline mode
TXD dominant time-out time	$t_{to(dom)TXD}$	2	3	4	ms	CAN Active mode; V_{TXD} = 0 V
Bus silence time-out time	$t_{to(silence)}$	0.8	1	1.3	s	recessive time measurement started in all CAN modes, guaranteed by design.
Delay time from bus active to bias	$t_{d(busact-bias)}$			200	µs	
CAN start-up time	$t_{startup(CAN)}$			220	µs	when switching to Active mode (CTS = 1)
CAN partial networking						
Number of idle bits	$N_{bit(idle)}$	6		10		before a new SOF is accepted; CFDC = 1, guaranteed by design.
Dominant bit filter time	$t_{fltr(bit)dom}$	5		17.5	%	arbitration data rate ≤ 500 kbit/s; CFDC = 1, guaranteed by design.
Pin RXD: interrupt/wake-up event timing (valid in CAN Offline mode only)						
Event capture delay time	$t_{d(event)}$	0.7	1	1.4	ms	CAN Offline mode
Blanking time	t_{blank}			25	µs	when switching from Offline to Active/Listen-only mode, guaranteed by design.
Pin WAKE						
Wake-up time	t_{wake}	50			µs	
Pin INH						
Delay time from bus wake-up to INH HIGH	$t_{d(buswake-INHH)}$			100	µs	

6.3. Parameter Measurement Information

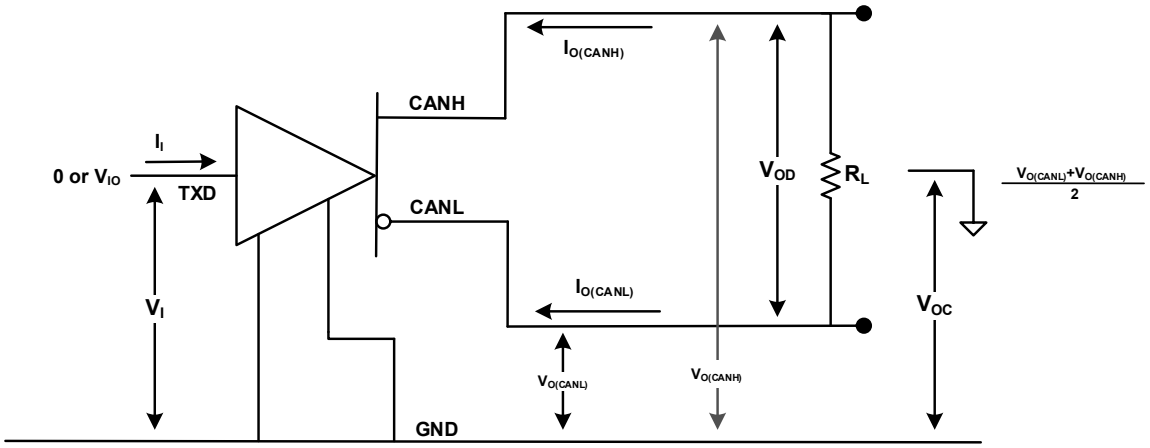


Figure 6.1 Driver Voltage, Current and Test Definitions

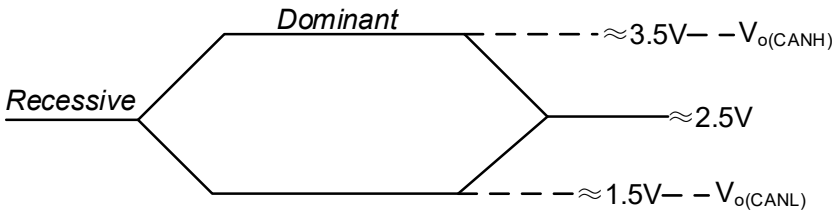


Figure 6.2 Bus Logic State Voltage Definitions

$$V_{IC} = \frac{V_{I\ (CANH)} + V_{I(CANL)}}{2}$$

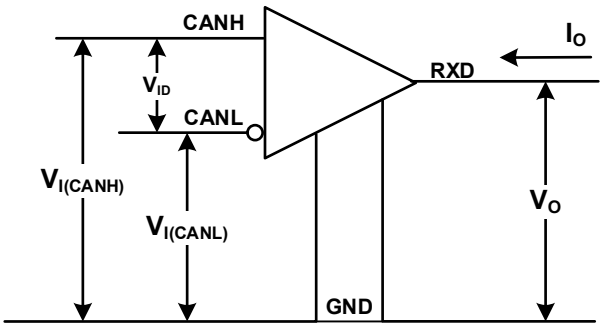


Figure 6.3 Receiver Voltage and Current Definitions

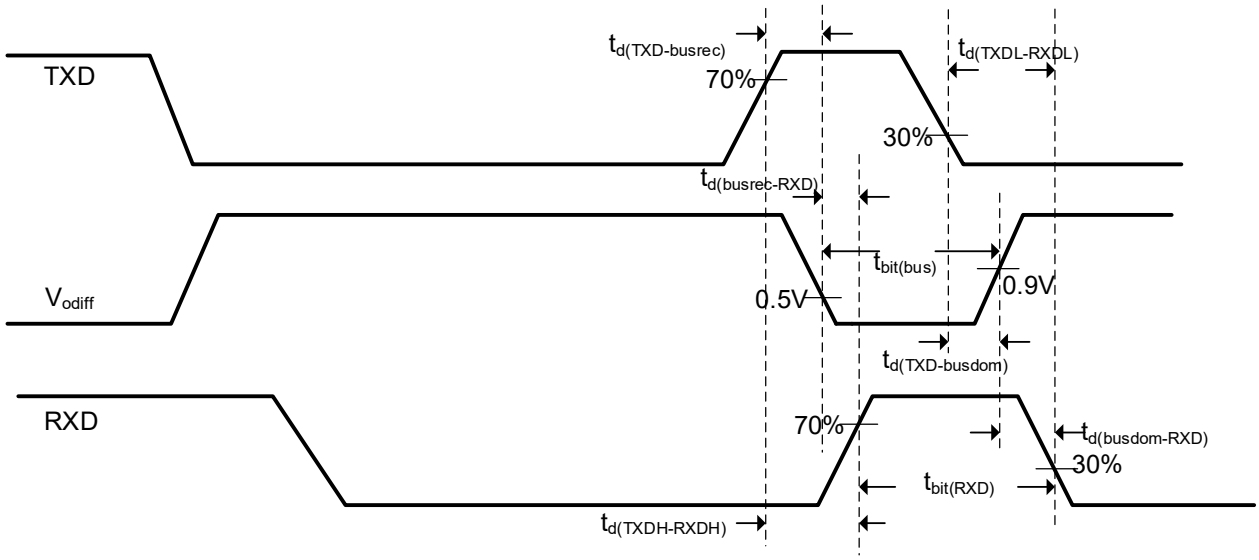


Figure 6.4 CAN timing definitions

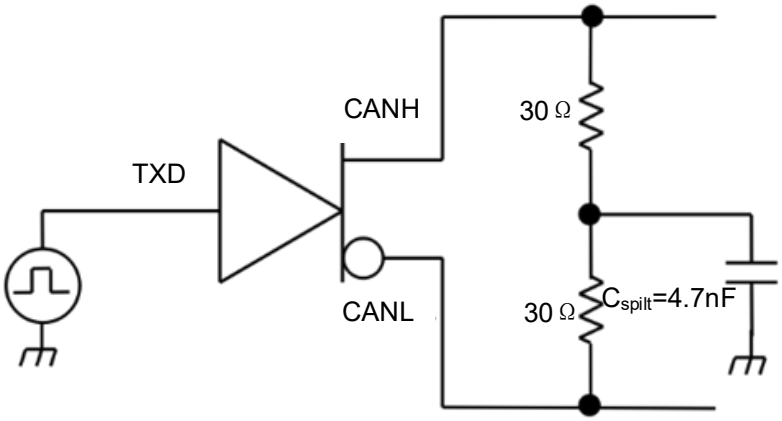


Figure 6.5 Transceiver Driver Symmetry Test Circuit

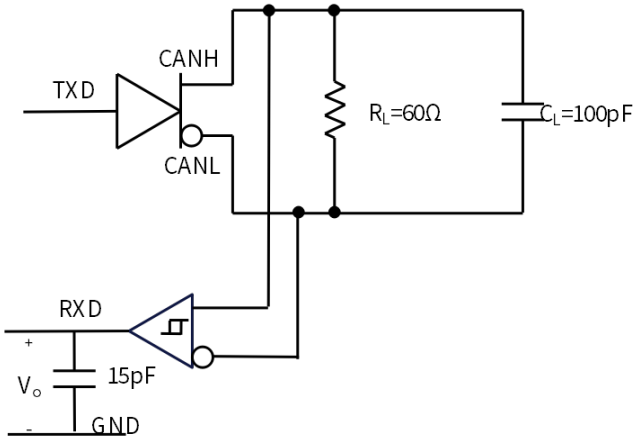


Figure 6.6 Timing test circuit

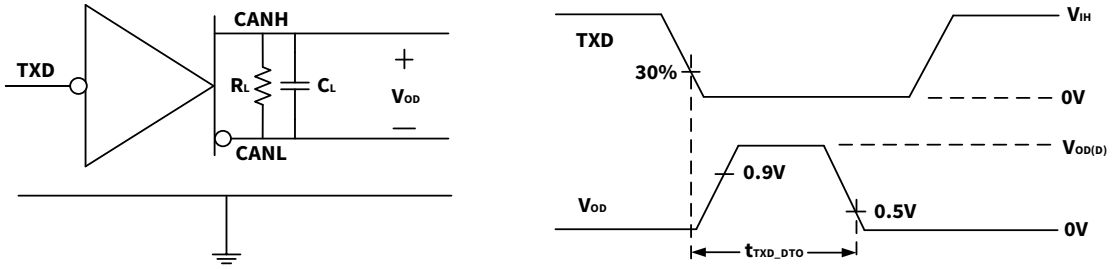


Figure 6.7 TXD Dominant Time Out Test Circuit and Measurement

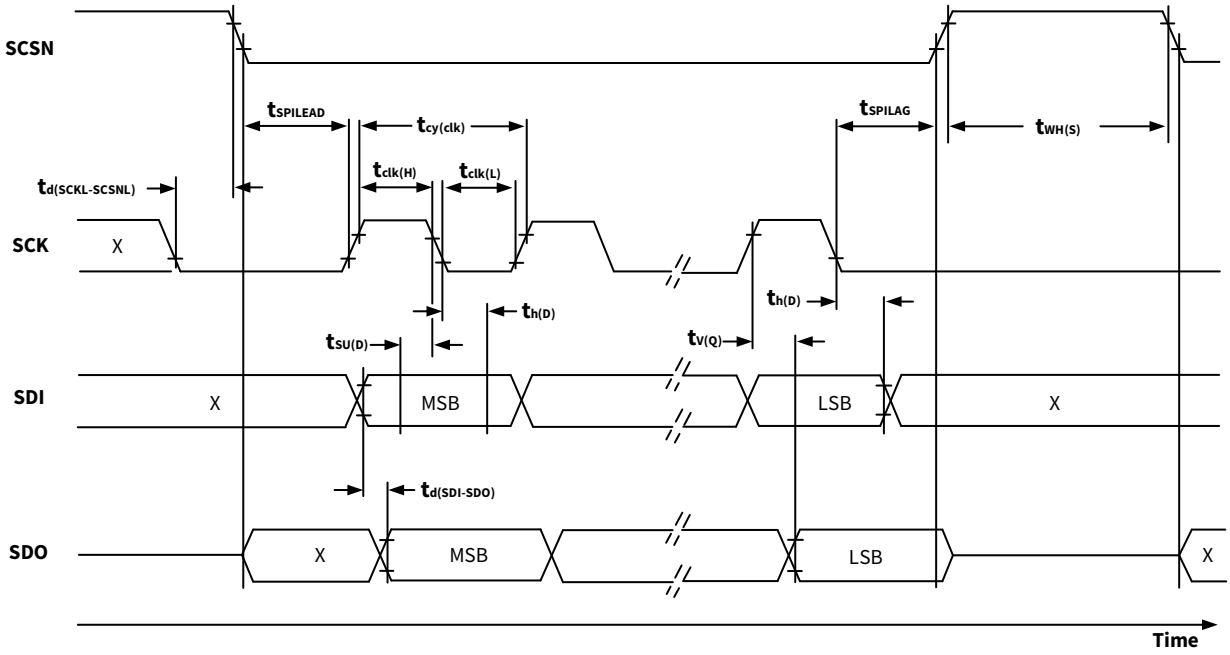


Figure 6.8 SPI timing diagram

7. Function Description

7.1. Overview

NCA1145B is a high-speed CAN transceiver providing an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver consumes very low power in Standby and Sleep modes. Meanwhile, NCA1145B supports CAN Partial Networking compliant to ISO11898-2:2024 by selective wake-up function. NCA1145 supports 'FD-passive' to ignore CAN FD frames while waiting for a valid wake-up frame in low power mode. It allows the CAN controllers that do not need CAN FD function to remain in Standby/Sleep mode during CAN FD communication in the network without generating bus errors.

The CAN signal improvements significantly reduce signal ringing on the network, allowing reliable CAN FD communication at 5 Mbit/s in larger topologies.

NCA1145B supplies an SPI interface to control the transceiver and to retrieve the status information. The I/O level of the transceiver is adjusted to the I/O level of microcontrollers as required, including 1.8V, 3.3V and 5V.

7.2. Detail description

7.2.1. BAT Pin

The BAT Pin connects to the battery supply and supplies for NCA1145B internal regulators that support the digital core and low power CAN receiver.

7.2.2. V_{IO} Pin

The V_{IO} Pin supplies SPI pins and its supply voltage ranges from 1.7V to 5.5V thus matching the microprocessor IO voltage of 1.8V, 3.3V and 5V.

7.2.3. V_{CC} Pin

The V_{CC} Pin supplies for the NCA1145B internal CAN transceiver.

7.2.4. GND Pin

The thermal pad should be connected to the GND plane for heat dissipation.

7.2.5. INH Pin

The INH pin is a high voltage output pin that provides voltage from the V_{BAT} to enable an external high voltage regulator. The INH function is on in all modes except for CAN sleep mode and NCA1145B off mode. In sleep mode, the INH pin is turned off, going into a high Z state. This allows the node to be placed into the lowest power state while in sleep mode.

7.2.6. Wake Pin

The WAKE pin is used for a local wake up. The pin is defaulted to bi-directional edge trigger, meaning it recognizes a local wake up on either a rising or falling edge of WAKE pin transition. This default value can be change via a SPI command that either configures it as a rising edge only, a falling edge only, a pulse of specific width and timing or a filtered rising or falling edge.

7.2.7. Operating modes

The system controller contains a state machine that supports five operating modes: Normal, Standby, Sleep, Overtemperature and Off. The state transitions are illustrated in Figure 7.1.

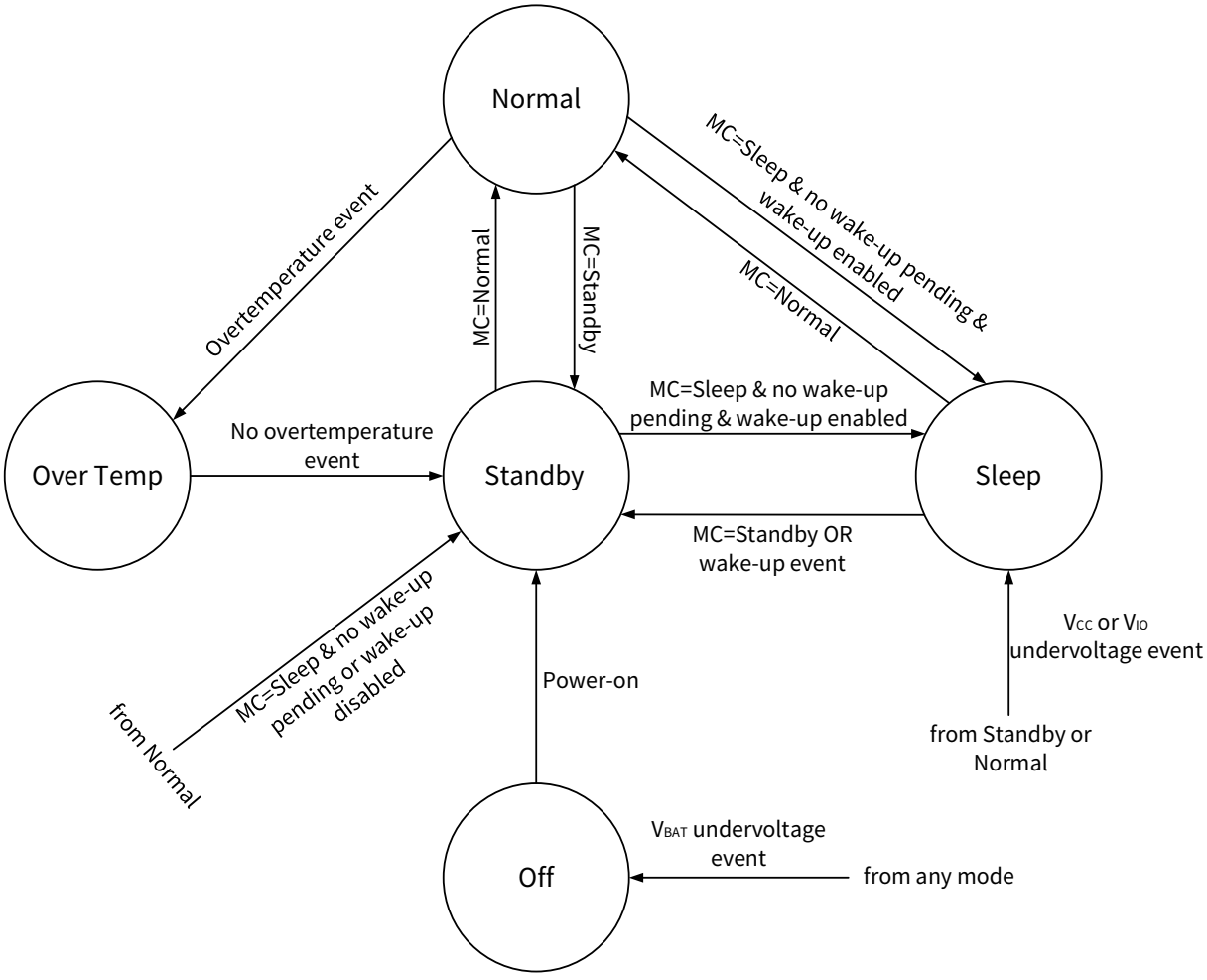


Figure 7.1 NCA1145B system controller state diagram

7.2.7.1. Normal mode

Normal mode is the active operating mode. In this mode, NCA1145B is fully operational. All device hardware is available and can be activated (see Table 7.2.1). Normal mode can be selected from Standby or Sleep mode via an SPI command (MC = 111).

7.2.7.2. Standby mode

Standby mode is one of the power-saving mode of NCA1145B. The transceiver doesn't work in Standby mode, but the INH pin remains active so voltage regulators controlled by this pin will be active. If remote CAN wake-up is enabled (CWE = 1), the receiver monitors bus activity for a wake-up request. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up can occur via a standard wake-up pattern or via a selective wake-up frame. Pin RXD is forced LOW when any enabled wake-up or interrupt event is detected (see Section 7.2.16).

7.2.7.3. Sleep mode

Sleep mode is another power saving mode of the NCA1145B. In Sleep mode, the transceiver behaves as in Standby Mode with the exception that pin INH is set to high-ohmic state. Voltage regulators controlled by this pin will be switched off, and the current into pin BAT will be reduced to a minimum.

Any enabled wake-up or interrupt event (except SPIF), or an SPI command, will wake up the transceiver from Sleep mode. Sleep mode can be selected from Normal or Standby mode via an SPI command (MC = 001). The NCA1145B will switch to Sleep mode on receipt of this command, provided there are no pending wake-up events and at least one regular wake-up source (CAN bus or WAKE pin) is enabled. Any attempt to enter Sleep mode while one of these conditions has not been met will cause the NCA1145B to switch to Standby mode.

The NCA1145B will also be forced to switch to Sleep mode after $t_{d(uvd\text{-}sleep)}$ if a V_{CC} or V_{IO} undervoltage event is detected ($V_{CC}/V_{IO} < V_{uvd(VCC)}/V_{uvd(VIO)}$ for longer than $t_{d(uvd)}$). In this event, all pending wake-up events will be cleared. CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE = WPRE = 1) are enabled in order to avoid a system deadlock and selective wake-up is disabled (CPNC = 0).

Status bit FSMS in the Main status register (Table 7.2.3) indicates whether a transition to Sleep mode was selected via an SPI command (FSMS = 0) or was forced by an undervoltage event on VCC or VIO (FSMS = 1). This bit can be read after the NCA1145B wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).

7.2.7.4. Off mode

The NCA1145B will be in Off mode when the battery voltage is too low. This is the default mode when the battery is first connected. The NCA1145B will switch to Off mode from any mode if the battery voltage drops below the power-off threshold ($V_{th(det)poff}$). In Off mode, Bus pins and pin INH are in a high-ohmic state. When the battery supply voltage rises above the power-on threshold ($V_{th(det)pon}$), the NCA1145B starts to boot up, triggering an initialization procedure. The NCA1145B will switch to Standby mode after $t_{start\ up}$.

7.2.7.5. Overtemp mode

Overtemp mode is provided to prevent NCA1145B being damaged by excessive temperatures. The NCA1145B switches immediately to Overtemp mode from Normal mode when the global chip temperature rises above the overtemperature protection activation threshold ($T_{th(act)otp}$). To help prevent the loss of data due to overheating, the NCA1145B issues a warning when the chip temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$). When this happens, status bit OTWS is set and an overtemperature interrupt is generated (OTW = 1), if enabled (OTWE = 1). In Overtemp mode, the CAN transceiver is disabled and the bus pins are in high-ohmic state. Wake-up events will not be detected, but a pending wake-up will still be noticed by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared.

7.2.7.6. Hardware characterization for the NCA1145B operating modes

Table 7.2.1 Hardware characterization by functional block

Pins	*Off*	*Standby*	*Normal*	*Sleep*	*Overtemp*
SPI	disabled	active	active	active (V_{IO} supplied)	disabled
INH	high-ohmic	V_{BAT} level	V_{BAT} level	high-ohmic	V_{BAT} level
CAN	off	offline	determined by CMC	offline	off
RXD	V_{IO} level	V_{IO} level/Low if wake-up or interrupt event detected	CAN bit stream if CMC = 01/10/11; otherwise same as Standby/Sleep	V_{IO} level/Low if wake-up or interrupt event detected	V_{IO} level/Low if wake-up pending

7.2.7.7. System control registers

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01.

Table 7.2.2 Mode control register(address 01h)

Bit	*Symbol*	*Access*	*Value*	*Description*
7:3	reserved	R		
2:0	MC	R/W		mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the NCA1145B has entered Normal mode after initial power-up. Bit FSMS indicates whether the most recent transition to Sleep mode was triggered by an undervoltage event or by an SPI command.

Table 7.2.3 Main status register (address 03h)

Bit	*Symbol*	*Access*	*Value*	*Description*
7	FSMS	R		Sleep mode transition status:
			0	transition to Sleep mode triggered by an SPI command
			1	an undervoltage on V_{CC} and/or V_{IO} forced a transition to Sleep mode
6	OTWS	R		overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	NCA1145B has entered Normal mode (after power-up)
			1	NCA1145B has powered up but has not yet switched to Normal mode
4:0	reserved	R		

7.2.8. CAN operating modes

The integrated CAN transceiver supports four operating modes: Active, Listen-only, Offline and Offline Bias (see Figure 7.2). The CAN transceiver operating mode depends on the NCA1145B operating mode and on the setting of bits CMC in the CAN control register (Table 7.2.4).

When the NCA1145B is in Normal mode, the CAN transceiver operating mode (Offline, Active or Listen-only) can be selected via bits CMC in the CAN control register (Table 7.2.4). When the NCA1145B is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).

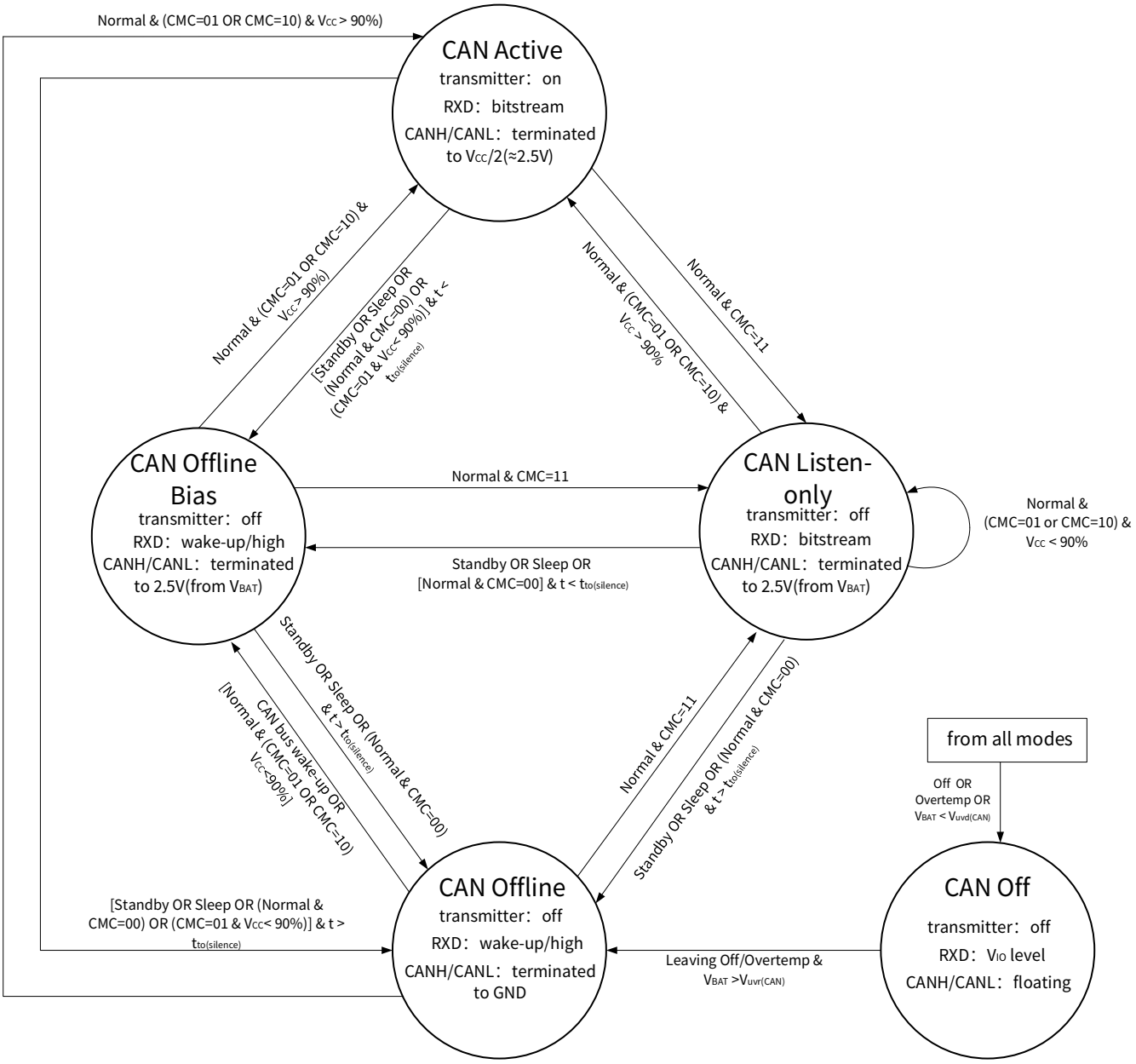


Figure 7.2 NCA1145B CAN transceiver state machine

7.2.8.1. CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines. CAN Active mode is selected when CMC = 01 or 10. When CMC = 01, VCC undervoltage detection is enabled and the transceiver switches to CAN Offline or CAN Offline Bias mode when the voltage on VCC drops below $V_{uvd(VCC)}$. When CMC = 10, VCC undervoltage detection is disabled. The transmitter will remain active until the NCA1145B is forced into Sleep mode by the VCC undervoltage event; the transceiver will then switch to CAN Offline or CAN Offline Bias mode. In CAN Active mode, the CAN bias voltage is derived from VCC.

If pin TXD is held Low (e.g. by a short-circuit to GND) when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXD goes high in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

7.2.8.2. CAN Listen-only mode

CAN Listen-only mode allows the NCA1145B to monitor bus activity while the transceiver is inactive, without influencing bus levels. This facility could be used by development tools that need to listen to the bus but do not need to transmit or receive data or for

software-driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low-power CAN engine designed to monitor the bus for potential wake-up events.

In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active. This enables the host microcontroller to switch to a low-power mode in which an embedded CAN protocol controller remains active, waiting for a signal to wake up the microcontroller.

The CAN transceiver will not leave Listen-only mode while TXD is Low or CAN Active mode is selected with CMC = 01 or 10 while the voltage on VCC is below the undervoltage threshold, $V_{uvd(VCC)}$.

7.2.8.3. CAN Offline and Offline Bias mode

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event, provided CAN wake-up detection is enabled (CWE = 1). CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

7.2.8.4. CAN Off mode

The CAN transceiver is switched off completely with the bus lines floating when:

- the NCA1145B switches to Off or Overtemp mode or
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when VBAT rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$) and the CAN transceiver is no longer in Off/Overtemp mode. CAN Off mode prevents reverse currents flowing from the bus when the battery supply to the CAN transceiver is lost.

7.2.9. CAN standard wake-up(partial networking not enabled)

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the NCA1145B will monitor the bus for a standard wake-up pattern. A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The NCA1145B wakes up from Standby or Sleep mode when a dedicated wake-up pattern (specified in ISO 11898-2:2024) is detected on the bus.

The wake-up pattern consists of the following phases, dominant or recessive bits between the phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 7.3). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains high until the wake-up event has been triggered. When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the transceiver event status register is set and pin RXD is driven Low. If the NCA1145B was in Sleep mode when the wake-up pattern was detected, it will switch pin INH to V_{BAT} to activate external voltage regulators (e.g. for supplying V_{CC} and V_{IO}) and enter Standby mode.

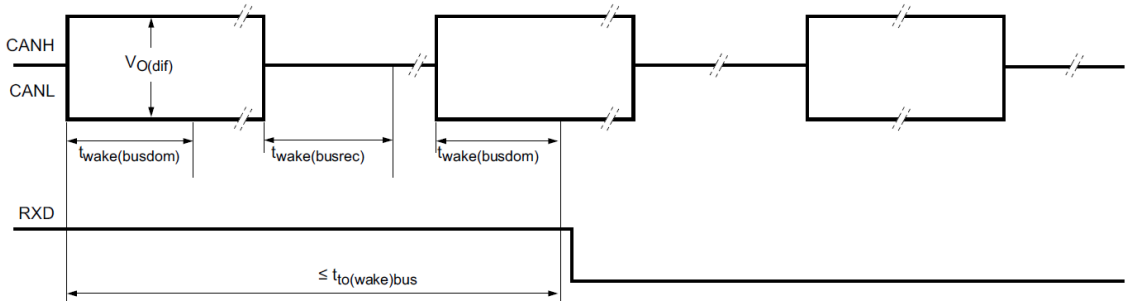


Figure 7.3 NCA1145B CAN wake-up timing

7.2.10. CAN control and Transceiver status registers

Table 7.2.4 CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	reserved	R		
6	CFDC	R/W		
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK	R/W		CAN partial networking configuration:
			0	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking registers configured successfully
4	CPNC	R/W		CAN selective wake-up; when enabled, node is part of a partial network:
			0	disable CAN selective wake-up
			1	enable CAN selective wake-up
3:2	reserved	R		
1:0	CMC	R/W		CAN transceiver operating mode selection:
			00	Offline mode
			01	Active mode (while NCA1145B is in Normal mode); V_{CC} undervoltage detection active; transition to Active mode, and remaining in Active mode, requires V_{CC} above undervoltage threshold
			10	Active mode (while NCA1145B is in Normal mode); V_{CC} undervoltage detection inactive; transition to Active mode requires V_{CC} above undervoltage threshold
			11	Listen-only mode

Table 7.2.5 Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode
6	CPNERR	R		CAN partial networking error status:
			0	no CAN partial networking error detected (PNFDE = 0 AND PNCOK = 1)
			1	CAN partial networking error detected (PNFDE = 1 or PNCOK = 0); wake-up via standard wake-up pattern only
5	CPNS	R		CAN partial networking status:
			0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration OK (PNCOK = 1)
4	COSCS	R		CAN oscillator status:
			0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency

3	CBSS	R		CAN bus silence status:
			0	CAN bus active (communication detected on bus)
			1	CAN bus inactive (for longer than $t_{to(silence)}$
2	reserved	R		
1	VCS	R		V_{CC} supply voltage status:
			0	V_{CC} is above the undervoltage detection threshold ($V_{uvd(VCC)}$)
			1	V_{CC} is below the undervoltage detection threshold ($V_{uvd(VCC)}$)
0	CFS	R		CAN failure status:
			0	no TXD dominant time-out event detected
			1	CAN transmitter disabled due to a TXD dominant time-out event

7.2.11. CAN partial networking

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed. If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

7.2.11.1. CAN partial networking configuration registers

Dedicated registers are provided for configuring CAN partial networking.

Table 7.2.6 Data rate register (address 26h)

Bit	*Symbol*	*Access*	*Value*	*Description*
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection
			000	50 kbits
			001	100 kbits
			010	125 kbits
			011	250 kbits
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

Table 7.2.7 ID registers 0 to 3 (addresses 27h to 2Ah)

Addr.	*Bit*	*Symbol*	*Access*	*Value*	*Description*
27h	7:0	ID7:ID0	R/W	-	bits ID7 to ID0 of the extended frame format
28h	7:0	ID15:ID08	R/W	-	bits ID15 to ID8 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format
	1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format
2Ah	7:5	reserved	R	-	
	4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

Table 7.2.8 ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

Addr.	*Bit*	*Symbol*	*Access*	*Value*	*Description*
2Bh	7:0	M7:M0	R/W	-	ID mask bits 7 to 0 of extended frame format
2Ch	7:0	M15:M8	R/W	-	ID mask bits 15 to 8 of extended frame format
2Dh	7:2	ID23:ID18	R/W	-	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format

	1:0	ID17:ID16	R/W	-	ID mask bits 17 to 16 of extended frame format
2Eh	7:5	reserved	R	-	
	4:0	ID28:ID24	R/W	-	ID mask bits 28 to 24 of extended frame format ID mask bits 10 to 6 of standard frame format

Table 7.2.9 Frame control register (address 2Fh)

Bit	*Symbol*	*Access*	*Value*	*Description*
7	IDE	R/W	-	Identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are 'don't care' for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected

Table 7.2.10 Data mask registers (addresses 68h to 6Fh)

Addr.	*Bit*	*Symbol*	*Access*	*Value*	*Description*
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration

Table 7.2.11 Data mask register usage for different values of DLC

DLC value	*DM*
1	DM7
2	DM6~7
3	DM5~7
4	DM4~7
5	DM3~7
6	DM2~7
7	DM1~7
8	DM0~7
>8	DM0~7

7.2.12. Wake-up frame (WUF)

A wake-up frame is a CAN frame according to ISO 11898-1:2015, consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter. The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 7.2.9).

A valid WUF identifier is defined and stored in the ID registers (Table7.2.7). An ID mask can be defined to allow a group of identifiers to be recognized as valid by one node. The identifier mask is defined in the mask registers (Table 7.2.8) and '1' means 'don't Care'.

In the example illustrated in Figure 7.4, based on the standard frame format, the 11-bit identifier is defined as 0x141. The identifier is stored in ID registers 2 (0x29) and 3 (0x2A). The three least significant bits of the ID mask, bits 2 to 4 of Mask register 2 (0x2D) are set to 1, which means that the corresponding identifier bits are 'don't care'. This means that any of eight different identifiers will be recognized as valid in the received WUF (from 0x140 to 0x147).

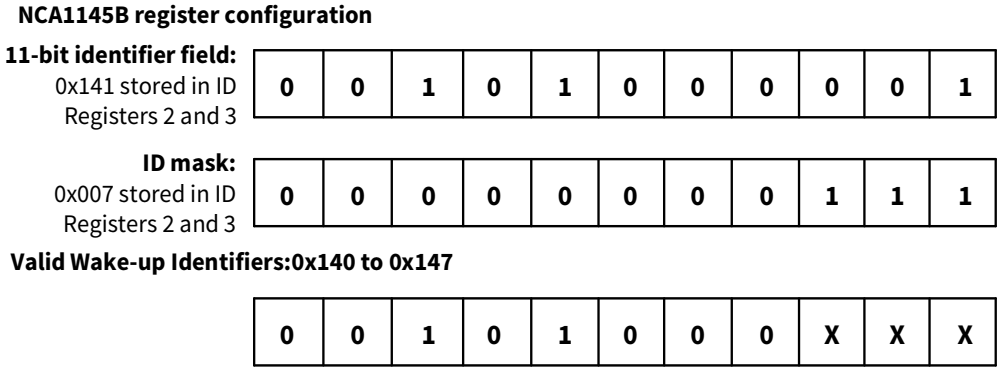


Figure 7.4 Evaluating the ID field in a selective wake-up frame

The data field indicates which nodes are to be woken up. Within the data field, groups of nodes can be pre-defined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

The data length code (bits DLC in the Frame control register; Table 7.2.9) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC≠0000), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 7.2.10) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined).

If DLC = 0000, a node will wake up if the WUF contains a valid identifier and the received data length code is 0000, regardless of the values stored in the data mask. If DLC≠0000 and all data mask bits are set to 0, the device cannot be woken up via the CAN bus (note that all data mask bits are set to 1 by default). If a WUF contains a valid ID but the DLCs (in the Frame control register and in the WUF) don't match, the data field is ignored and no nodes are woken up.

In the example illustrated in Figure7.5, the data field consists of a single byte (DLC = 1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see Table 7.2.10 and Table 7.2.11). Data mask 7 is defined as 10101010 in the example. This means that up to three groups of nodes could be woken up (group 1,3,5 and 7) if the respective bits in the data frame are also set to 1.

The received message shown in Figure 7.5 could, potentially, wake up four groups of nodes: groups 2, 3, 4, 5 and 7. Three matches are found (groups 3, 5 and 7) when the message data bits are compared with the configured data mask (DM7).

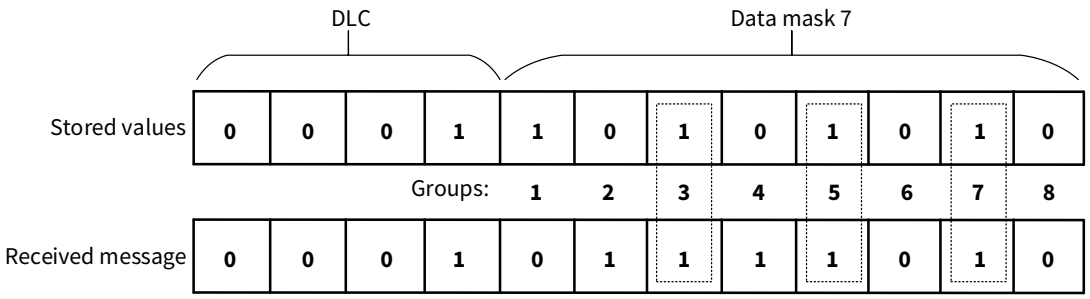


Figure 7.5 Evaluating the data field in a selective wake-up frame

Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included in the wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error.

When PNDM = 1, a valid wake-up message is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the frame is not a Remote frame AND
- the data length code in the received message matches the configured data length code (bits DLC) AND
- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error.

If the NCA1145B receives a CAN message containing errors (e.g. a 'stuffing' error) transmitted in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDE = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The NCA1145B clears PNCOK after a write access to any of the CAN partial networking configuration registers.

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWE = 1), then any valid wake-up pattern (according to ISO 11898-2:2024) will trigger a wake-up event. If the CAN transceiver is not in Offline mode (CMC≠00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus will be ignored.

CAN bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s are supported during selective wake-up. The bit rate is selected via bits CDR (see Table 7.2.5).

7.2.13. CAN FD passive

CAN FD stands for 'CAN with Flexible Data-Rate'. It is based on the CAN protocol as specified in ISO 11898-1:2015. In time, all CAN controllers will be required to comply with the new standard (enabling 'FD-active' nodes) or at least to tolerate CAN FD communication (enabling 'FD-passive' nodes).

CAN FD passive is supported up to a ratio of one-to-eight between arbitration and data bit rates, without unwanted wake-ups. The CAN FD filter parameter defined in ISO 11898-2:2024 and SAE J2284 is supported up to a ratio of one-to-four, with a maximum supported bit data bit rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s. CAN FD frames are interpreted as frames with errors by the partial networking module in the NCA1145B when CFDC=0. So the error counter is incremented when a CAN FD frame is received. If the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow, bit PNFDE is set to 1 and the device wakes up.

7.2.14. Fail-safe features

7.2.14.1. TXD dominant time-out

A TXD dominant time-out timer works when pin TXD is forced low while the transceiver is in Active Mode. If the low state on pin TXD stays longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes high. The TXD dominant time-out time also defines the minimum possible bit rate of 15 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure interrupt is generated (CF = 1), if enabled (CFE = 1). In addition, the status of the TXD dominant time-out can be read via the CFS bit in the transceiver status register and bit CTS is set to 0.

7.2.14.2. Pull-up on TXD pin

Pin TXD has an internal pull-up towards VIO to ensure a safe defined recessive driver state in case the pin is left floating.

7.2.14.3. VCC undervoltage event

When CMC = 01 and the supply to the CAN transceiver (V_{CC}) falls below $V_{uvd(VCC)}$, a CAN failure event is captured (CF = 1), assuming CAN failure detection is enabled (CFE = 1), and status bit VCS is set to 1.

7.2.14.4. Loss of power at pin BAT

A loss of power at pin BAT has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus.

7.2.15. Local wake-up via WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register. A wake-up event is triggered by a Low-to-High (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that don't make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND to ensure optimal EMI performance.

Table 7.2.12 WAKE status register (address 4Bh)

Bit	*Symbol*	*Access*	*Value*	*Description*
7:2	reserved	R	-	
1	WPVS	R		WAKE pin status:
			0	voltage on WAKE pin below switching threshold ($V_{th(sw)}$)
			1	voltage on WAKE pin above switching threshold ($V_{th(sw)}$)
0	reserved	R	-	

While the NCA1145B is in Normal mode, the status of the voltage on pin WAKE can always be read via bit WPVS. Otherwise, WPVS is only valid if local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

7.2.16. Wake-up and interrupt event diagnosis via pin RXD

Wake-up and interrupt event diagnosis in the NCA1145B is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers and is signaled on pin RXD pin, if enabled.

A distinction is made between regular wake-up events and interrupt events (at least one regular wake-up source must be enabled to allow the NCA1145B to switch to Sleep mode).

Table 7.2.13 Regular wake-up events

Symbol	*Event*	*Power-on*	*Description*
CW	CAN wake-up	disabled	a CAN wake-up event was detected while the transceiver was in CAN Offline mode.
WPR	rising edge on WAKE pin	disabled	a rising-edge wake-up was detected on pin WAKE
WPF	falling edge on WAKE pin	disabled	a falling-edge wake-up was detected on pin WAKE

Table 7.2.14 Interrupt events

Symbol	*Event*	*Power-on*	*Description*
PO	power-on	always enabled	the NCA1145B has exited Off mode (after battery power has been restored/connected)
OTW	Overtemperature warning	disabled	the chip temperature has exceeded the overtemperature

			warning threshold (only detected in Normal mode)
SPIF	SPI failure	disabled	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal MC code or attempted write access to locked register (an SPI failure event will not wake-up the NCA1145B from Sleep mode)
PNFDE	PN frame detection error	always enabled	partial networking frame detection error
CBS	CAN bus silence	disabled	no activity on CAN bus for $t_{to(silence)}$ (detected only when CBSE = 1 while bus active)
CF	CAN failure	disabled	one of the following CAN failure events detected (not is Sleep mode): - CAN transceiver deactivated due to a dominant clamped TXD - CAN transceiver deactivated due to a VCC undervoltage event (if CMC = 01)

PO and PNFDE interrupts are always captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers (Table 7.2.16 to Table 7.2.18). If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode, pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the NCA1145B is in Sleep mode when an event (other than a SPIF interrupt) occurs, pin INH is forced High and the NCA1145B switches to Standby mode. If the NCA1145B is in Standby mode when the event occurs, pin RXD is forced Low to flag an interrupt/wake-up event. The detection of any enabled wake-up or interrupt event will trigger a wake-up in Standby mode. The detection of any enabled wake-up or interrupt event other than a SPIF interrupt will trigger a wake-up in Sleep mode. The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register (Table 7.2.15), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, transceiver or WAKE) and then query the relevant table (Table 7.2.16, Table 7.2.17 or Table 7.2.18 respectively).

After the event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits. It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

7.2.16.1. Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven low, requiring a response from the microcontroller each time an interrupt/wake-up is generated). The NCA1145B has an interrupt/wake-up delay timer to limit the disturbance to the software. When one of the event capture status bits is cleared, pin RXD is released (high) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes low again to alert the microcontroller. In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events. If all active event capture bits have been cleared (by the microcontroller) when the timer expires after $t_{d(event)}$, pin RXD remains high (since there are no pending events). The event capture registers can be read at any time.

7.2.16.2. Sleep mode protection

It is very important that event detection is configured correctly when the NCA1145B switches to Sleep mode for responding to a wake-up event correctly. For this reason, and to avoid potential system deadlocks, at least one regular wake-up event must be enabled and all event status bits must be cleared before the NCA1145B switches to Sleep mode. Otherwise the NCA1145 will switch to Standby mode in response to a go-to-sleep command (MC = 001).

7.2.16.3. Event status and event capture registers

After an event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant status bit (writing 0 will have no effect).

Table 7.2.15 Global event status register (address 60h)

Bit	*Symbol*	*Access*	*Value*	*Description*
7:4	reserved	R	-	
3	WPE	R		WAKE pin event:
			0	no pending WAKE pin event

			1	WAKE pin event pending at address 0x64
2	TRXE	R		transceiver event:
			0	no pending transceiver event
			1	transceiver event pending at address 0x63
1	reserved	R	-	
0	SYSE	R	-	system event
			0	no pending system event
			1	system event pending at address 0x61

Table 7.2.16 System event status register (address 61h)

Bit	*Symbol*	*Access*	*Value*	*Description*
7:5	reserved	R	-	
4	PO[1]	R		WAKE pin event:
			0	no pending WAKE pin event
			1	WAKE pin event pending at address 0x64
3	reserved	R	-	
2	OTW	R/W		overtemperature warning:
			0	overtemperature not detected
			1	the global chip temperature has exceeded the overtemperature warning threshold ($T_{th(warn)otp}$)
1	SPIF	R/W	-	SPI failure
			0	no SPI failure detected
			1	SPI failure detected
0	reserved	R	-	

(1) PO is cleared when the NCA1145B is forced to Sleep mode due to an undervoltage event. The information stored in PO could be lost if the transition to Sleep mode was forced by an undervoltage event. Bit NMS，which is set to 0 when the NCA1145B switches to Normal mode after power-on, compensates for this.

Table 7.2.17 Transceiver event status register (address 63h)

Bit	*Symbol*	*Access*	*Value*	*Description*
7:6	reserved	R	-	
5	PNFDE	R/W		partial networking frame detection error:
			0	no partial networking frame detection error detected
			1	partial networking frame detection error detected
4	CBS	R/W		CAN-bus status:
			0	CAN-bus active
			1	no activity on CAN-bus for $t_{to(silence)}$
3:2	reserved	R		
1	CF[1]	R/W	-	CAN failure
			0	no CAN failure detected
			1	CAN failure event detected
0	CW	R/W	-	CAN wake-up:
			0	no CAN wake-up event detected
			1	CAN wake-up event detected

Table 7.2.18 WAKE pin event status register (address 64h)

Bit	*Symbol*	*Access*	*Value*	*Description*
7:2	reserved	R	-	
1	WPR	R/W		WAKE pin rising edge:
			0	no rising edge detected on WAKE pin
			1	rising edge detected on WAKE pin
0	WPF	R/W		WAKE pin falling edge:
			0	no falling edge detected on WAKE pin
			1	falling edge detected on WAKE pin

Table 7.2.19 System event capture enable register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	OTWE	R/W		overtemperature warning enable:
			0	overtemperature warning disabled
			1	overtemperature warning enabled
1	SPIFE	R/W		SPI failure enable:
			0	SPI failure detection disabled
			1	SPI failure detection enabled
0	reserved	R	-	

Table 7.2.20 Transceiver event capture enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	CBSE	R/W		CAN-bus silence enable:
			0	CAN-bus silence detection disabled
			1	CAN-bus silence detection enabled
3:2	reserved	R		
1	CFE	R/W		CAN failure enable:
			0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W	-	CAN wake-up enable:
			0	CAN wake-up detection disabled
			1	CAN wake-up detection enabled

(1) CF is only enabled in Normal mode while the transceiver is in CAN Active mode and is triggered if TXD is clamped dominant OR a Vcc undervoltage is detected (when CMC = 01).

Table 7.2.21 WAKE pin event capture enable register (address 4Ch)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPRE	R/W		WAKE pin rising edge enable:
			0	rising-edge detection on WAKE pin disabled
			1	rising-edge detection on WAKE pin enabled
0	WPEF	R/W		WAKE pin falling edge enable:
			0	falling-edge detection on WAKE pin disabled
			1	falling-edge detection on WAKE pin enabled

7.2.17. Lock control register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the NCA1145B updating status registers etc.

Table7.2.22 Lock control register (address 0Ah)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	cleared for future use
6	LK6C	R/W		lock control 6: address area 0x68 to 0x6F – partial networking data byte registers
			0	SPI write-access enabled
			1	SPI write-access disabled
5	LK5C	R/W		lock control 5: address area 0x50 to 0x5F
			0	SPI write-access enabled
			1	SPI write-access disabled
4	LK4C	R/W		lock control 4: address area 0x40 to 0x4F - WAKE pin configuration
			0	SPI write-access enabled
			1	SPI write-access disabled

3	LK3C	R/W		lock control 3: address area 0x30 to 0x3F
			0	SPI write-access enabled
			1	SPI write-access disabled
2	LK2C	R/W		lock control 2: address area 0x20 to 0x2F - transceiver control and partial networking
			0	SPI write-access enabled
			1	SPI write-access disabled
1	LK1C	R/W		lock control 1: address area 0x10 to 0x1F
			0	SPI write-access enabled
			1	SPI write-access disabled
0	LK0C	R/W		lock control 0: address area 0x06 to 0x09 – general purpose memory
			0	SPI write-access enabled
			1	SPI write-access disabled

7.2.18. General-purpose memory

NCA1145B allocates 4 bytes of memory for general-purpose registers used to store user information. The general purpose registers can be accessed via the SPI at address 0x06 to 0x09.

7.2.19. V_{CC}/V_{IO} undervoltage protection

If an undervoltage is detected on pins V_{CC} or V_{IO}, and it remains valid for longer than the undervoltage detection delay time, $t_{d(uvd)}$, the NCA1145B is forced to Sleep mode. A number of preventative measures are taken when the NCA1145B is forced to Sleep mode to avoid deadlock and unpredictable states:

All previously captured events (address range 0x61 to 0x64) are cleared before the NCA1145B switches to Sleep Mode to avoid repeated attempts to wake up while an undervoltage is present.

- Both CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE =WPRE = 1) are enabled in order to avoid a deadlock situation where the NCA1145 cannot be woken up after entering Sleep mode.
- Partial Networking is disabled (CPNC = 0) to ensure immediate wake-up in response to bus traffic after the NCA1145B has recovered from an undervoltage event.
- The Partial Networking Configuration bit is cleared (CPNOK = 0) to indicate that partial networking might not have been configured correctly when the NCA1145 switched to Sleep mode.

Status bit FSMS is set to 1 when a transition to Sleep mode is forced by an undervoltage event. This bit can be sampled after the NCA1145B wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).

7.2.20. SPI

7.2.20.1. Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active low; default level is high(pull-up)
- SCK: SPI clock; default level is LOW due to internal pull-down
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH (may need external pull-up or pull-down if not available in the host controller)

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Figure 8.6.

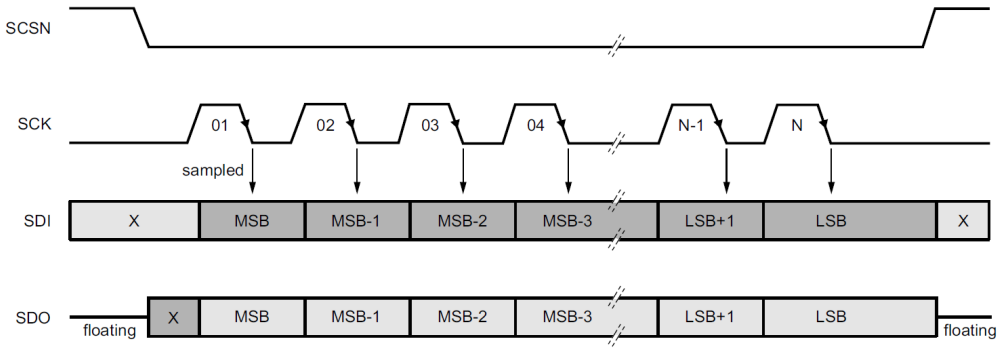


Figure 7.6 SPI timing protocol

The SPI data in the NCA1145B is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes (16 bits) must be transmitted to the NCA1145B for a single register read or write operation. The first byte contains the 7-bit address along with a 'read-only' bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The second byte contains the data to be written to the register.24-and 32-bit read and write operations are also supported. The register address is automatically incremented, once for a 24-bit operation and twice for a 32-bit operation, as illustrated in Figure 7.7.

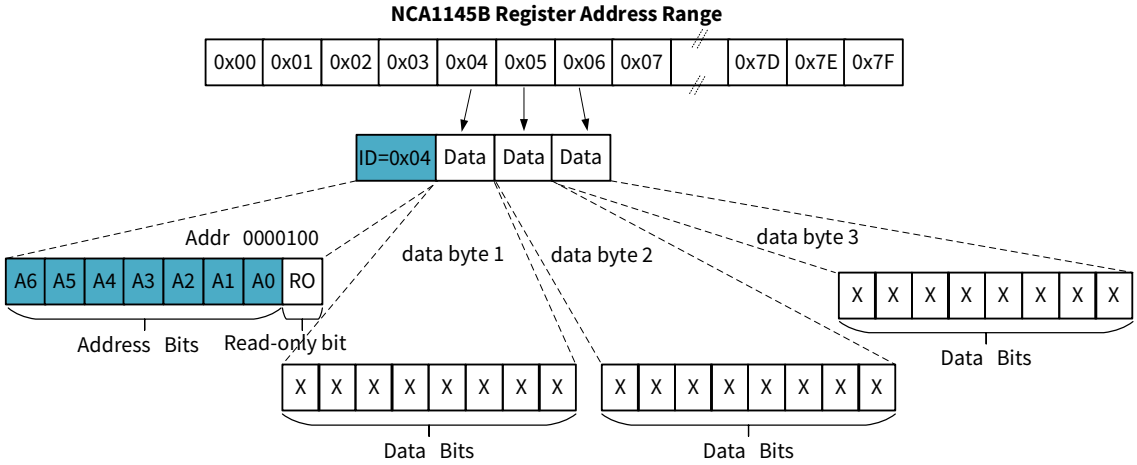


Figure 7.7 SPI data structure for a write operation (16-, 24- or 32-bit)

During an SPI data read or write operation, the contents of the addressed register(s) is returned via pin SDO. The NCA1145B tolerates attempts to write to registers that don't exist. If the available address space is exceeded during a write operation, the data above the valid address range is ignored (without generating an SPI failure event). During a write operation, the NCA1145B monitors the number of SPI bits transmitted. If the number recorded is not 16, 24 or 32, then the write operation is aborted and an SPI failure event is captured (SPIF = 1). If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDI is reflected on SDO from bit 33 onwards.

7.2.21. Register map

The addressable register space contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided in Table 7.2.23 to Table 7.2.27. The functionality of the individual bits is discussed in more detail in relevant sections of the data sheet.

Table 7.2.23 primary control registers

Address	*Register Name*	*Bit*							
		7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0x01	Mode control	reserved					MC		
0x03	Main status	FSMS	OTWS	NMS	reserved				
0x04	System event enable	reserved					OTWE	SPIFE	reserved
0x06	Memory 0	GPM [7:0]							
0x07	Memory 1	GPM [15:8]							

0x08	Memory 2	GPM [23:16]							
0x09	Memory 3	GPM [31:24]							
0x0A	Lock control	reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C

Table 7.2.24 Transceiver control and partial networking registers

Address	*Register Name*	*Bit*							
		7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0x20	CAN control	reserved	CFDC	PNCOK	CPNC	reserved		CMC	
0x22	Transceiver status	CTS	CPNERR	CPNS	COSCS	CBSS	reserved	VCS	CFS
0x23	Transceiver event enable	reserved			CBSE	reserved		CFE	CWE
0x26	Data rate	reserved						CDR	
0x27	Identifier 0	ID [7:0]							
0x28	Identifier 1	ID [15:8]							
0x29	Identifier 2	ID [23:16]							
0x2A	Identifier 3	reserved			ID [28:24]				
0x2B	Mask 0	M [7:0]							
0x2C	Mask 1	M [15:8]							
0x2D	Mask 2	M [23:16]							
0x2E	Mask 3	reserved			M [28:24]				
0x2F	Frame control	IDE	PNDM	reserved		DLC			
0x68	Data mask 0	DM0[7:0]							
0x69	Data mask 1	DM1[7:0]							
0x6A	Data mask 2	DM2[7:0]							
0x6B	Data mask 3	DM3[7:0]							
0x6C	Data mask 4	DM4[7:0]							
0x6D	Data mask 5	DM5[7:0]							
0x6E	Data mask 6	DM6[7:0]							
0x6F	Data mask 7	DM7[7:0]							

Table 7.2.25 WAKE pin control and status registers

Address	*Register Name*	*Bit*							
		7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0x4B	WAKE pin status	reserved						WPVS	reserved
0x4C	WAKE pin enable	reserved						WPRE	WPFE

Table 7.2.26 Event capture registers

Address	*Register Name*	*Bit*							
		7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0x60	Event capture status	reserved				WPE	TRXE	reserved	SYSE
0x61	System event status	reserved			PO	reserved	OTW	SPIF	reserved
0x63	Transceiver event status	reserved		PNFDE	CBS	reserved		CF	CW
0x64	WAKE pin event status	reserved						WPR	WPF

7.2.22. Register configuration in system operating modes

NCA1145B may change register bits state automatically when it switches from one operating mode to another. This is particularly evident when the NCA1145B switches to Off mode or when an undervoltage event forces a transition to Sleep mode.

These changes are summarized in Table 7.2.27. If an SPI transmission is in progress when the NCA1145B changes state, the transmission is ignored (automatic state changes have priority).

Table 7.2.27 Register bit settings in NCA1145B operating modes

Symbol	*Off(reset values)*	*Standby*	*Normal*	*Sleep*	*Overtemp*	*Forced Sleep(UV)*
CBS	0	no change	no change	no change	no change	0
CBSE	0	no change	no change	no change	no change	no change
CBSS	1	actual state	actual state	actual state	actual state	actual state
CDR	101	no change	no change	no change	no change	no change

CF	0	no change	no change	no change	no change	0
CFDC	0	no change	no change	no change	no change	no change
CFE	0	no change	no change	no change	no change	no change
CFS	0	actual state	actual state	actual state	actual state	actual state
CMC	01	no change	no change	no change	no change	no change
COSCS	0	actual state	actual state	actual state	actual state	actual state
CPNC	0	no change	no change	no change	no change	0
CPNERR	1	actual state	actual state	actual state	actual state	actual state
CPNS	0	actual state	actual state	actual state	actual state	actual state
CTS	0	0	actual state	0	0	0
CW	0	no change	no change	no change	no change	0
CWE	0	no change	no change	no change	no change	1
DMn	11111111	no change	no change	no change	no change	no change
DLC	0000	no change	no change	no change	no change	no change
FSMS	0	no change	no change	0	no change	1
GPMn	00000000	no change	no change	no change	no change	no change
IDn	00000000	no change	no change	no change	no change	no change
IDE	0	no change	no change	no change	no change	no change
LKnC	0	no change	no change	no change	no change	no change
Mn	00000000	no change	no change	no change	no change	no change
MC	100	100	111	001	don’t care	001
NMS	1	no change	0	no change	no change	no change
OTW	0	no change	no change	no change	no change	0
OTWE	0	no change	no change	no change	no change	no change
OTWS	0	actual state	actual state	actual state	actual state	actual state
PNCOK	0	no change	no change	no change	no change	0
PNDM	1	no change	no change	no change	no change	no change
PNFDE	0	no change	no change	no change	no change	0
PO	1	no change	no change	no change	no change	0
SPIF	0	no change	no change	no change	no change	0
SPIFE	0	no change	no change	no change	no change	no change
SYSE	1	no change	no change	no change	no change	0
TRXE	0	no change	no change	no change	no change	0
VCS	0	actual state	actual state	actual state	actual state	actual state
WPE	0	no change	no change	no change	no change	0
WPF	0	no change	no change	no change	no change	0
WPFE	0	no change	no change	no change	no change	1
WPR	0	no change	no change	no change	no change	0
WPRE	0	no change	no change	no change	no change	1
WPVS	0	no change	no change	no change	no change	no change

8. Application Note

8.1. Typical Application Circuit

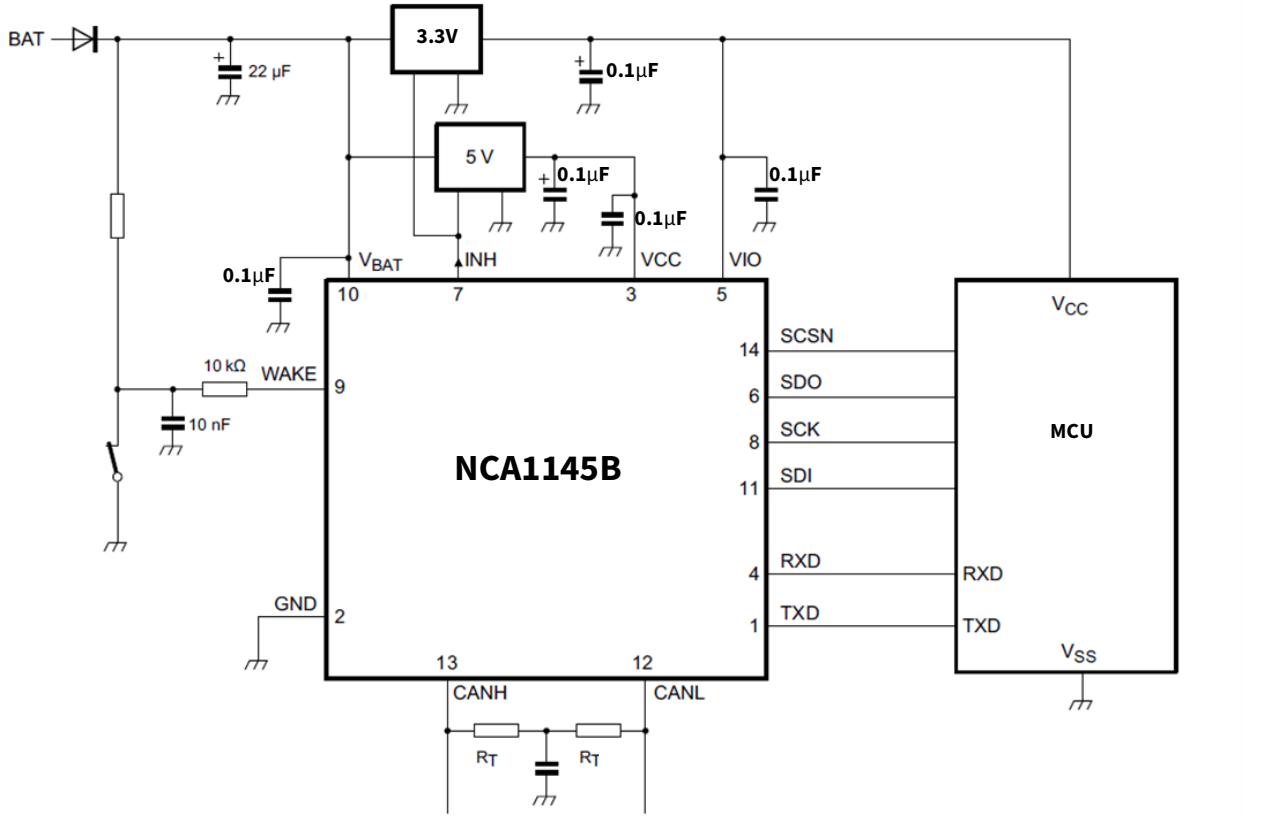
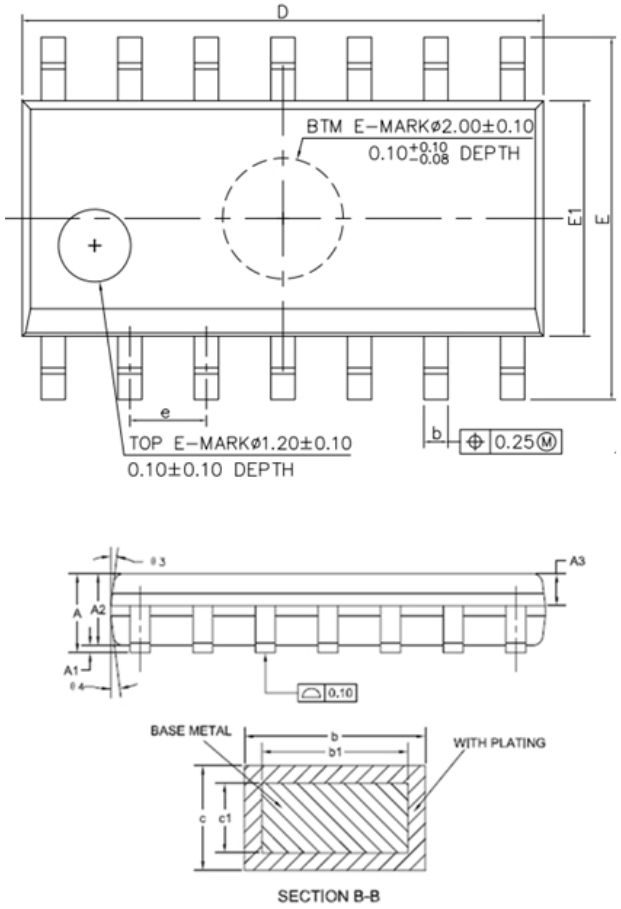


Figure 8.1 Typical application circuit for NCA1145B

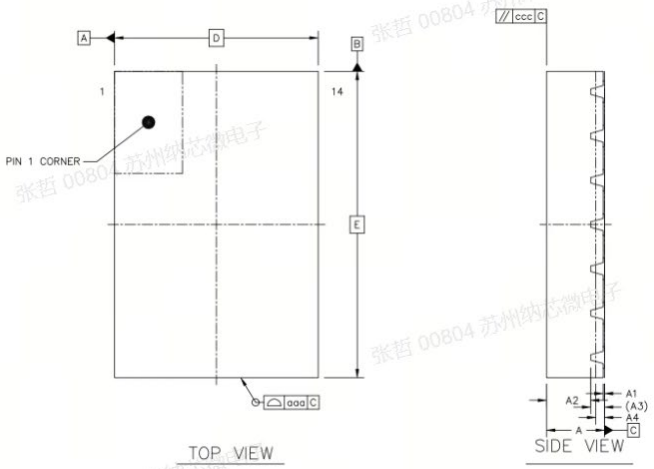
9. Package Information

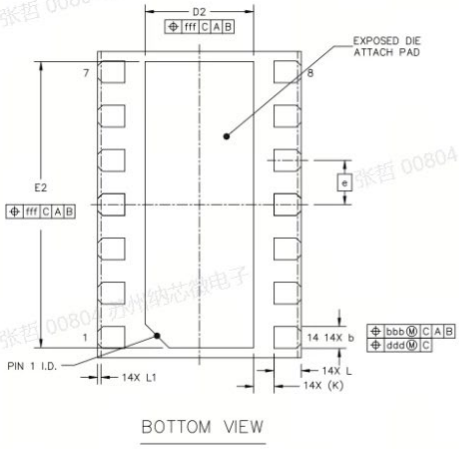


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
A3	0.55	0.65	0.75
b	0.36	–	0.51
b1	0.35	0.40	0.45
c	0.18	–	0.25
c1	0.17	0.20	0.23
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.22	1.27	1.32
H	0.30	0.40	0.50
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	10°	12°	14°
θ2	8°	10°	12°
θ3	10°	12°	14°
θ4	8°	10°	12°

Figure 9.1 SOP14 Package Shape and Dimension in millimeters





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.0500
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.1800
LEAD WIDTH		b	0.27	0.32	0.37
BODY SIZE	X	D		3 BSC	
	Y	E		4.5 BSC	
LEAD PITCH		e		0.65 BSC	
EP SIZE	X	D2	1.5	1.6	1.7
	Y	E2	4.10	4.20	4.30
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.0100	---	0.0900
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

Figure 9.2 DFN14 Package Shape and Dimension in millimeters

10. Ordering Information

Part Number	*Max Data Rate (Mbps)*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NCA1145B-Q1SPKR	5	-40 to 125℃	2	SOP14	SOP14	2500
NCA1145B-Q1DNKR	5	-40 to 125℃	2	DFN14	DFN14	6000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.						

11. Tape and Reel Information

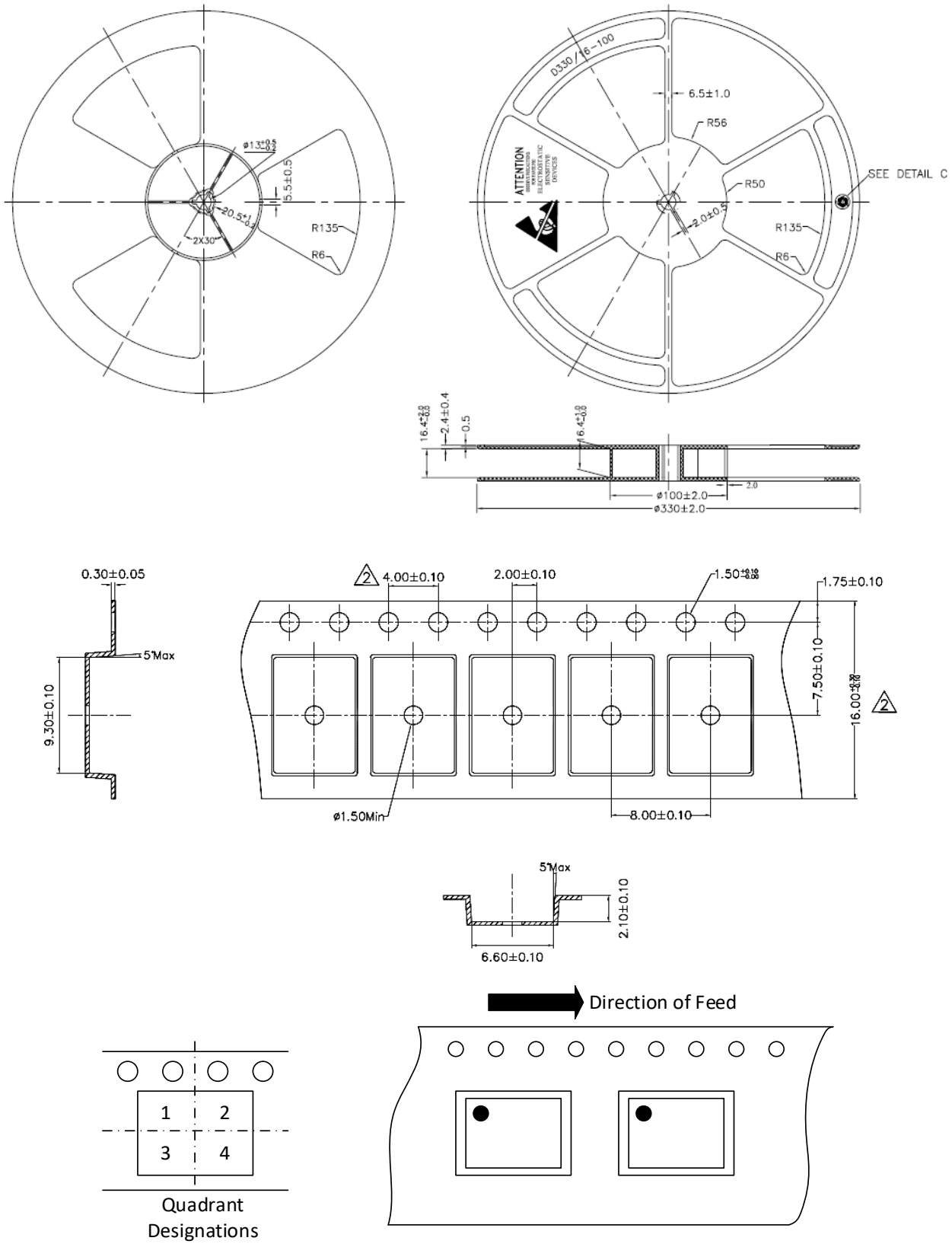


Figure 11.1 Tape and Reel Information of SOP14

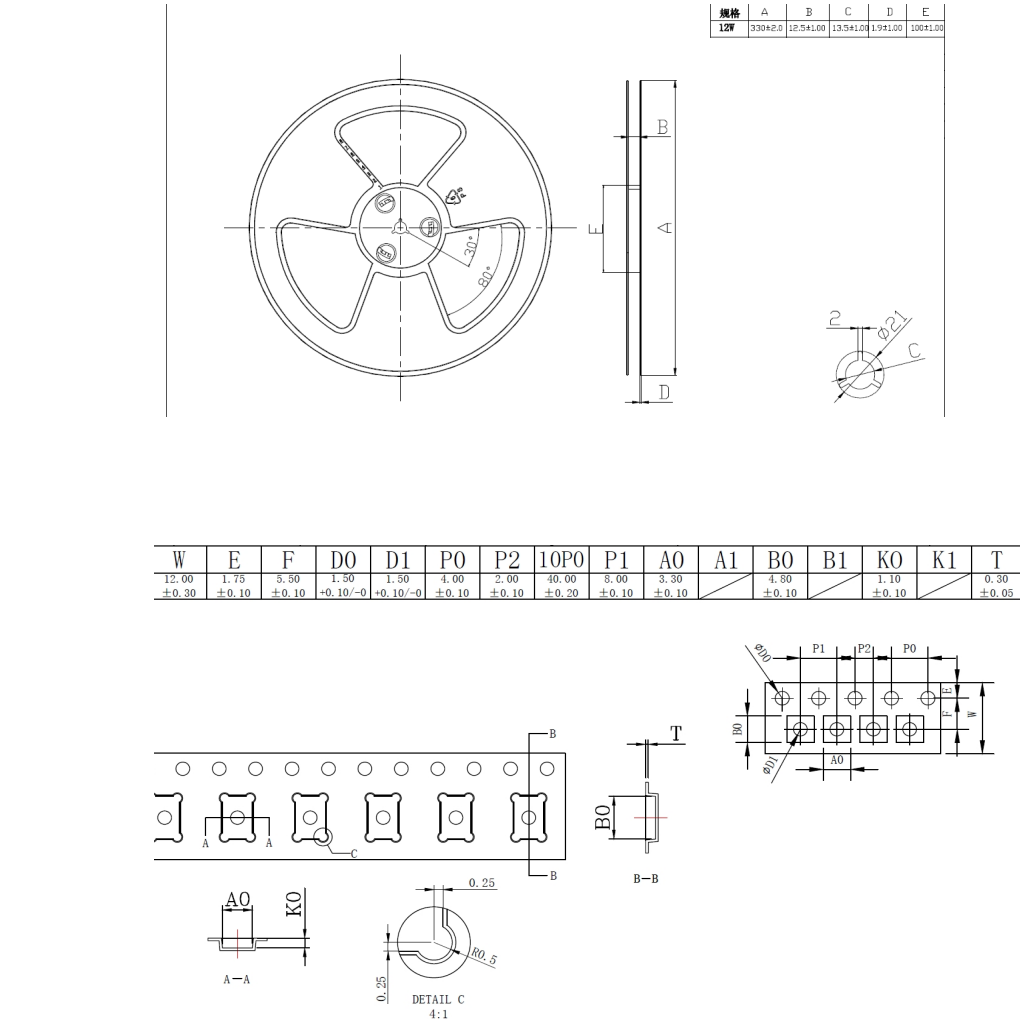


Figure 11.2 Tape and Reel Information of DFN14

12. Revision History

Revision	Description	Date
1.0	Initial Version.	2025/3/10

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